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Design & Implementation of Interface between FPGA & DSP Using High Speed Communication with SDR Technique.

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Abstract: *Software Defined Radio (SDR) is a concept of wireless communication. SDR technology is used to establish a flexible wireless communication system. It supports multiple frequency bands and multiple modes. It can be programmed to support new communication standards. Through the wireless load to achieve a dynamic upgrade, and even redefine the air interface in the air. With the rapid development of FPGA (Field Programming Gate Array) technology, ultra-large-scale, high-speed FPGA chip is emerging, to achieve high-speed digital signal processing possible .Based on FPGA and DSP, the embedded design supports a more flexible program for the realization of software-designed radio. Then how to make fast and efficient plan to achieve high-speed data communication between DSP and FPGA has become an urgent problem. For solving this problem, this paper introduces a program which realizes the high-speed communication between DSP and FPGA.*

I. Introduction

Here a high-speed data communication method between DSP and FPGA is implemented to meet the real-time requirements of data transmission and algorithm processing in software-defined radio system. The system uses AD9361 for data acquisition, high-performance FPGA for data pre-processing, low-power DSP processor to achieve complex algorithm and extract parameters, combined high-speed data processing of DSP with real-time response of FPGA to meet the performance optimization of the system. The software radio system to complete the rapid scanning of the spectrum (70 MHz–6 GHz), real-time analysis and early prediction. This Program is based on the TMS320 C6748 series of DSP chips and Xilinx Spartan6 FPGA chip, using a universal parallel interface connect FPGA and DSP, in which the interrupt signal and enable signal as judging bit and enable bit complete communication. The experimental results demonstrate that the scheme has high feasibility and stability.

The purpose of an SDR system is to implement as much as possible of the modulation/demodulation and data processing algorithms in software and reprogrammable logic so that the communication system can be easily reconfigured just by updating the software and the reprogrammable logic and not making any changes to the hardware platform. Software Defined Radio (SDR) is a concept of wireless communication. SDR technology is used to establish a flexible wireless communication system. It supports multiple frequency bands and multiple modes. It can be programmed to support new communication standards. Through the wireless load to achieve a dynamic upgrade, and even re-define the air interface in the air. This design concept in the early, usually by the DSP and programmable devices to complete. With the rapid development of FPGA (Field Programming Gate Array) technology, ultra-large-scale, high-speed FPGA chip is emerging, to achieve high-speed digital signal processing possible.

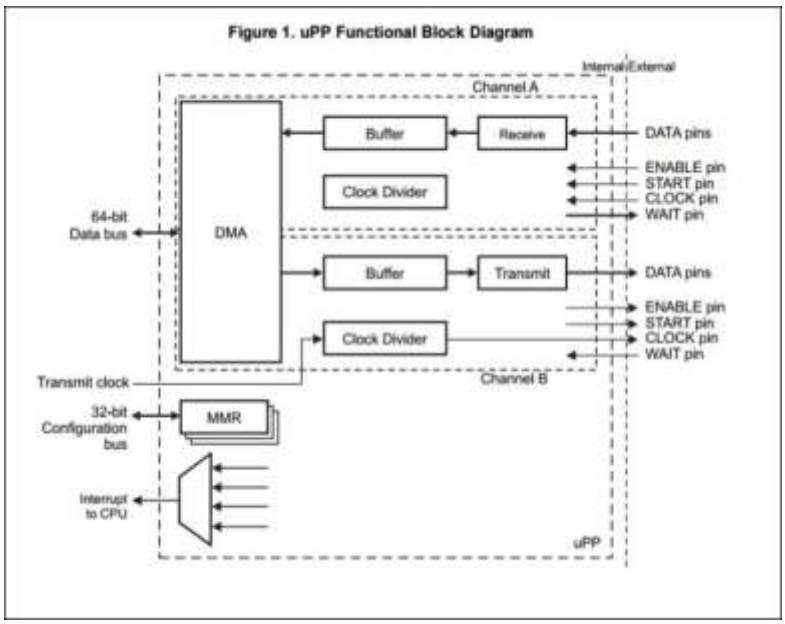
II. Study Area

Study area for the research includes:
1. FPGA Transmit Nodule
2. uPP Interface Initialization
3. DSP Read and Write Data Modules
4. Simulink model

The purpose of the peripheral the universal parallel port (uPP) peripheral is a multichannel, high-speed parallel interface with dedicated data lines and minimal control signals. It is designed to interface cleanly with high-speed analog-to-digital converters (ADCs) or digital-to-analog converters (DACs) with up to 8-bit data width (per channel). It may also be interconnected with field-programmable gate arrays (FPGAs) or other uPP devices to achieve high-speed digital data transfer. It can operate in receive mode, transmit mode, or duplex mode, in which its individual channels operate in opposite directions. The uPP peripheral includes an internal DMAcontroller to maximize throughput and minimize CPU overhead during high-speed data transmission. All

uPP transactions use the internal DMA to feed data to or retrieve data from the I/O channels. The DMA controller includes two DMA channels, which typically service separate I/O channels. The uPP peripheral also supports data interleave mode, in which all DMA resources service a single I/O channel. In this mode, only one I/O channel may be used.

Figure 1 provides a high-level view of the uPP peripheral internal logic. Note that this figure shows one particular configuration: Channel A receives and Channel B transmits. In general, each channel may operate in either direction.



The system is designed with a 16-bit transceiver uPP interface, due to hardware limitations, it only can be carried out transmit and receive experiment separately on the platform.

III. Methodology

The work will be carried out in the following steps.

1. Literature review of existing technologies.
2. Implementation of the FPGA through the uPP interface to send data to the DSP is the key of our system design.
3. The DSP will actually read the data. DSP will read data through the 16- bit bus from the uPP.
4. Due to hardware limitations, there is no way to carry out 16-bit loop test, so in the loop test of uPP interface, 8-bit transceiver is used to send data by DSP through the uPP interface to the FPGA, and FPGA receive data back to DSP.
5. Finally, the data received by DSP will be shown on PC through serial ports.
6. Serial ports will print the information and the data DSP received can be shown on terminal.
7. In the platform uPP experiment is carried out, it can be seen that DSP and FPGA direct communication channel is built and the communication method is stable and testing accuracy with many trials.
8. The system will use AD9361 for data acquisition, high-performance FPGA for data pre-processing, low-power DSP processor to achieve complex algorithm and extract parameters, combined high-speed data processing of DSP with real-time response of FPGA to meet the performance optimization of the system.
9. The software radio system to complete the rapid scanning of the spectrum (70 MHz–6 GHz), real-time analysis and early prediction. This Program will be based on the TMS320C6748 series of DSP chips and Xilinx Spartan6 FPGA chip, using a universal parallel interface connect FPGA and DSP, in which the interrupt signal and enable signal are judging bit and enable bit that will complete the communication.
10. The experimental results can demonstrate that the scheme has high feasibility and stability. Same system can be implemented in Simulink for simulation in case of issue in hardware implementation for testing for real-time. Simulink model give same system approach for the expected results proposed here.
11. With research and industrial application it can be proved the efficiency and accuracy of Simulink models of Dynamic systems utilized and tested in Engineering. The floating point design in MATLAB has been moved to fixed point values using Xilinx DSP system generator software a model based approach associated with assistance software from Math works.

IV. Conclusion

1. Here, according to the application requirement of software-defined radio in spectrum recognition system, a high-speed communication scheme between DSP and FPGA will be designed based on the uPP interface.
2. The system is designed with a 16-bit transceiver uPP interface, due to hardware limitations, it only can be carried out for transmit and receive experiments separately on the platform.
3. Simulation and testing of data transfer between FPGA through the uPP interface to the DSP. DSP read data through the 16-bit bus to the corresponding mapping area.
4. Compare simulation diagram and actual receive data, FPGA transmit data is the same with the data that DSP reads. Due to hardware limitations, there is no way to carry out16-bit loop test, so in the loop test of uPP interface, 8-bit the communication method is stable and accuracy from the test results.
5. In the scheme, the internal DMA controller directly will transfer data between the system memory and the peripheral device without occupying the CPU resources of the DSP, and greatly improve the efficiency and the throughput of the system.
6. In the FPGA the asynchronous cache module will be designed to speed data processing and increase the stability of data processing. Thus completing the data reception and transmission.
7. After the software simulation and board-level verification, the system can achieve accurate real-time high-speed data transmission between FPGA and DSP, the program has been applied to the platform.
8. The end results will be a prototype system that can used as a proof-of-concept for several applications. The performance of the system will be quite good, when compared to the theoretical performance of an ideal spread-spectrum radio. Off-loading processing from the DSP to the FPGA allows the system to be built using a low-cost, low-power processor, rather than requiring a GHz-class DSP to do the entire job. The uPP interface allows simple FPGA interfacing and boasts significant performance advantages over using other available interfaces on the DSP. Relieving the DSP of data movement by using the DMA in the uPP also helps keep DSP cycles available for more important work.

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