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Zero Volatage Switching Operation of a Boost Converter

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Abstract: *The power converters are known as one of the most widely used in any electrical applications. However, design of a power converter taking inductor current ripple into existence is one of the major concerns while designing a boost converter. A huge inductor ripple current may destroy the entire circuit resulting a huge amount of losses. Hence, a topology should be adopted to minimise the over current in a power converter circuit because of the inductive element.A gate switching drive in case of a boost converter results induction over current which cause excessive switching loss.In this paper a zero voltage switching topology is designed which allows the MOSFET to switch on whenever it senses a zero voltage.Thus the switching losses can be minimised.*

I. Introduction

The power converters are assumed to be in an ideal state during the mathematical analysis for simpler calculation. However, the practical converter circuits deals with different kind of losses. The losses may occur because of the resistance, continuous and discontinuous switching of the the semiconductor switches used in the circuit, passive element involved in the circuit operation etc. the losses that appear in the circuit during the converter operation affects the overall performance of the circuit and as a result of which the efficiency is affected. So there is n urgent need to minimize the circuit losses to achieve the minimum power loss and a better efficiency. The power converter are normally designed to operate in a very high operating switching frequency. High switching frequency results very low output ripple

II. An Overview Of Zero Vlotage Switching

Theoretically Zero voltage switching is defined as the square wave power conversion during the on-time of the switch with resonant switching transition. it can also be defined as the utilization of a constant off control that varies the conversion frequency, or to vary the output by controlling the on time of the switch. For a single switching cycle it can be expressed as the control of duty cycle keeping the switching frequency constant. In the circuit drawn below using ltSpice is the basic circuit of a boost converter. The time intervals and the other parameters are calculated and the final equations used for calculations are represented below.

III. Variable Ranges

The ranges are defined here which are used during the during the ltSpice simulations, programmings and matlab calculations.

$$350 < V_{IN} < 450 \qquad 1 < V_{LIN} < 150 \qquad 1e-9 < t_{ON} < 20e-6$$

V_{IN} : Input Voltage

V_L : Output Voltage

t_{ON} : on time of the mosfet

Equations Derived

$$t_1 = t_{ON} - t_{LIN}$$

$$t_2 = (\pi/2 - \Phi)/\omega$$

$$\phi = tan^{-1}(t_1\omega) - t_1\omega$$

$$t_3 = acos(V_{IN} * C_{OSS} * \omega/(-I_{Lpeak}) + cos(\omega * t_1 + \phi) - \phi)/\omega$$

$$t_4 = I_{Lpeak} * sin(\omega * t_3 + \phi) * L./(V_IN - V_L) + t_3$$

$$t_6 = acos(1 + (V_{IN}/(V_L - V_{IN})))/\omega + t_4$$

$$t_{LIN} = \sqrt{LC_{OSS}V_{IN}(V_{IN} - 2V_L)}/V_L$$

$$I_{t3} = I_{Lpeak} * sin(\omega * t_3 + \phi)$$

$$I_{out} = (V_L * t_1^2 - V_L * (t_{lin}).^2 + (V_{IN} - V_L) * (t_4 - t_3)^2)/(2 * L * t_{sw})$$

$$I_{L_Min} = \omega * C_{OSS} * (V_L - V_{IN})$$

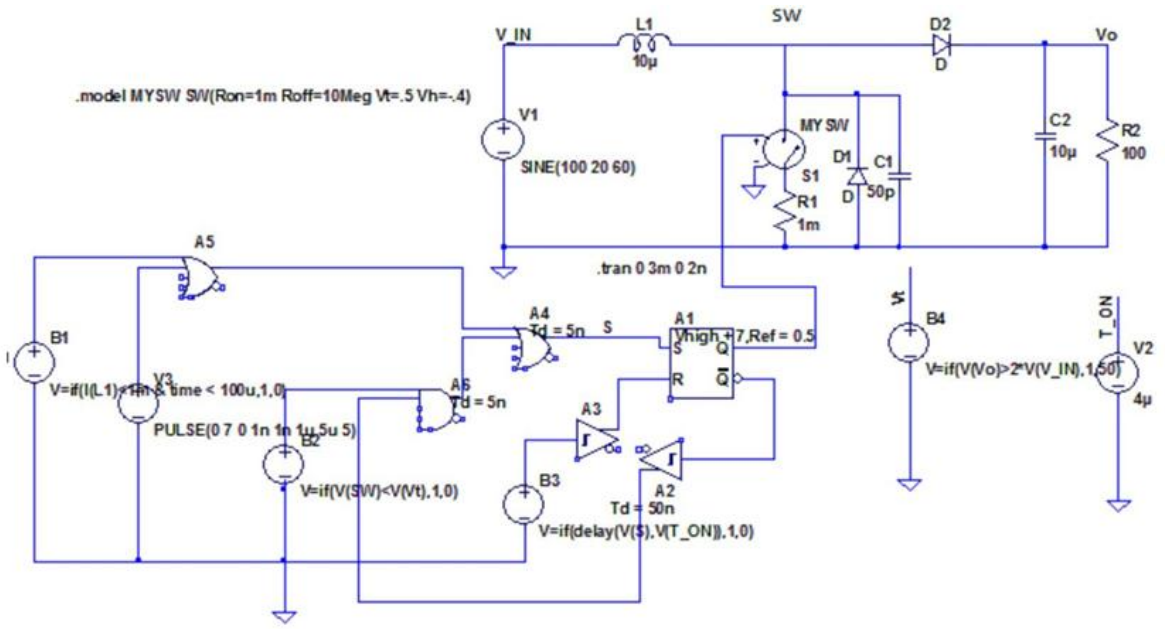
All the formulae derived for the calculation and circuit implementation are mentioned above. T0 to t1= switch is on and the diode is off
T1= V_{SW} is equal to V_{IN}

t1 to t2 = time when the inductor current follows a cosine curve

t2 = time when the inductor current approaches to the maximum value

t2 to t3 = the inductor current follows cosine curve till V_{SW} is equal to V_{IN} t3 to T5= the inductor starts discharging linearly and follows a linear curve t4 = the time when inductor current is zero
t5= time when the switch is again turned on and the diode is off

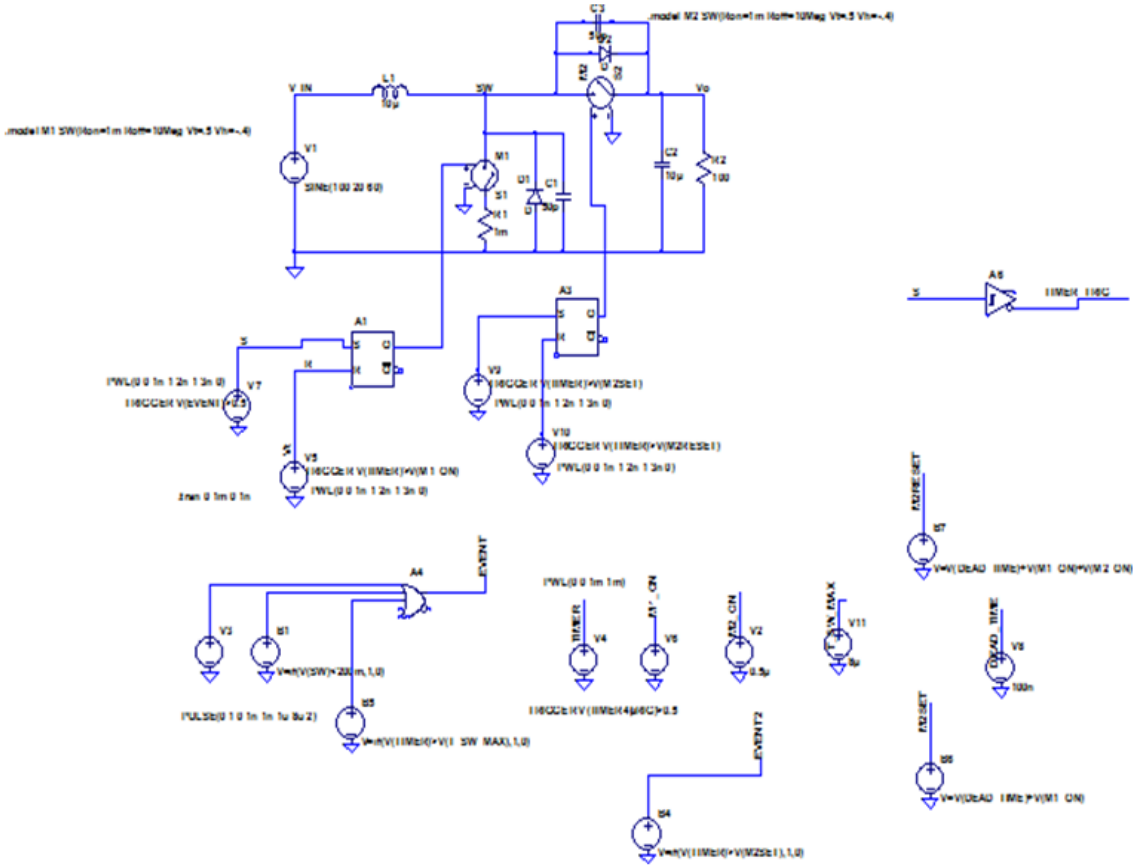
2.1 Initial circuit diagram of the boost converter designed during the period of internship is mentioned below.
The diagram drawn below is just the initial approach to the project.the developed and modified circuit diagram is mentioned in this report.



"MY SW" is the mosfet for the boost converter. The control circuit that connected to the gate terminal of the mosfet is the gate drive designed to achieve the zero voltage switching.

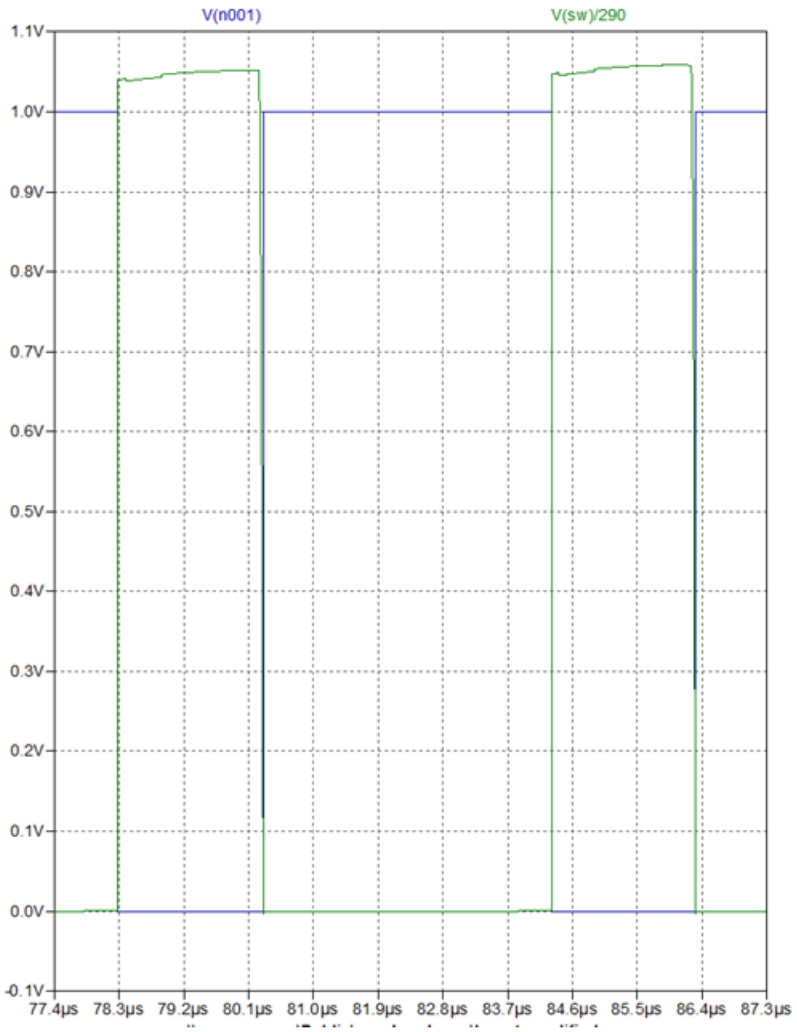
As the control system of the simulation using LTSPICE is not so effective in order to achieve the zero voltage switching and the microcontroller programming the control scheme was further developed to the circuit drawn below.

A graph is plotted using ltSpice

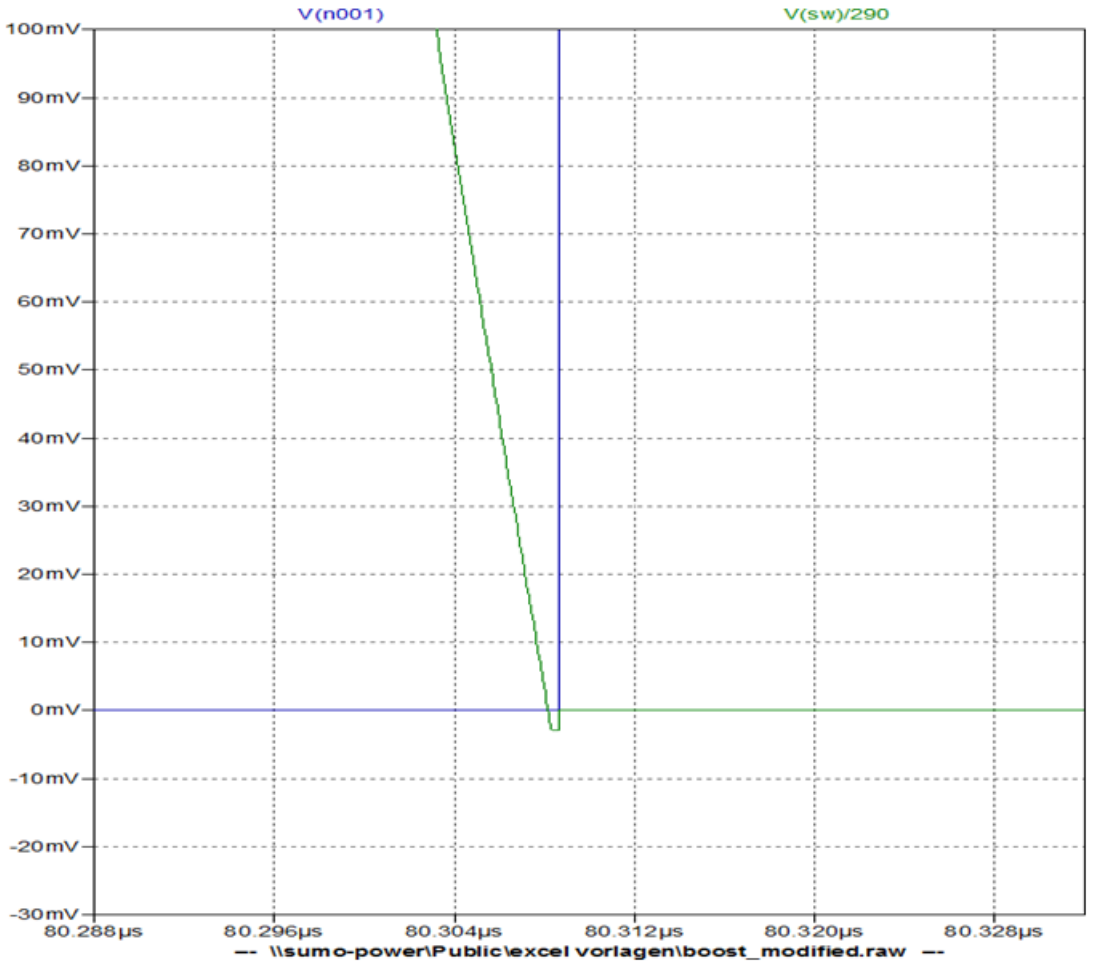


A graph is ploted using ltSPICE which represents the voltage across the switch and the voltage across the gate drive .the zero voltage switching can clearly be seen here in the graph.

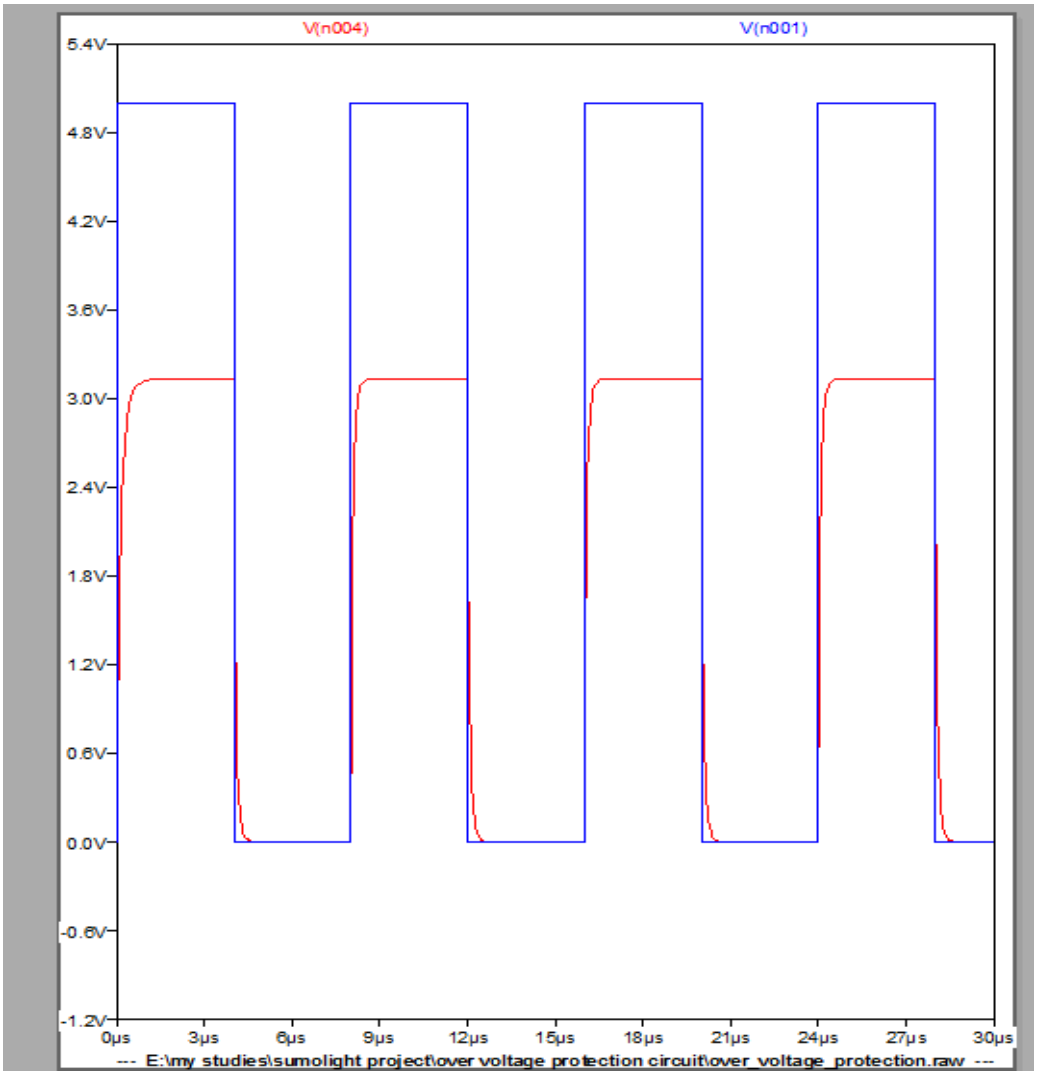
Here V_sw represents the switching voltage and V_001 represents the gate voltage.



The zero voltage can be seen here.

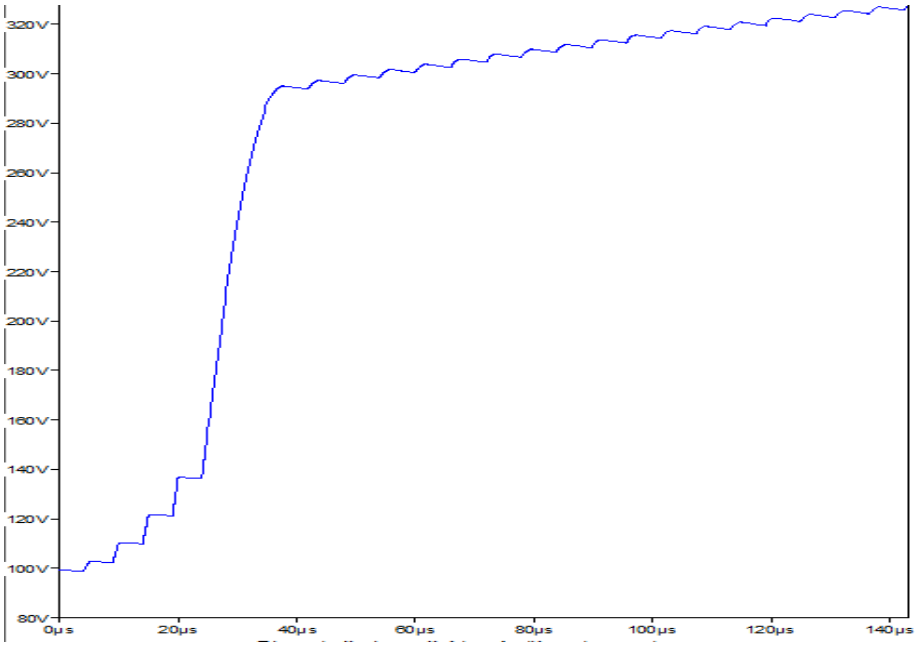


Here is a circuit drawn using ltspice to represent the circuit connection of TVS diode and TBU and the output at the load.
The output across the load is mentioned below .this represents the effect of TVS and TBU on the input wave form.

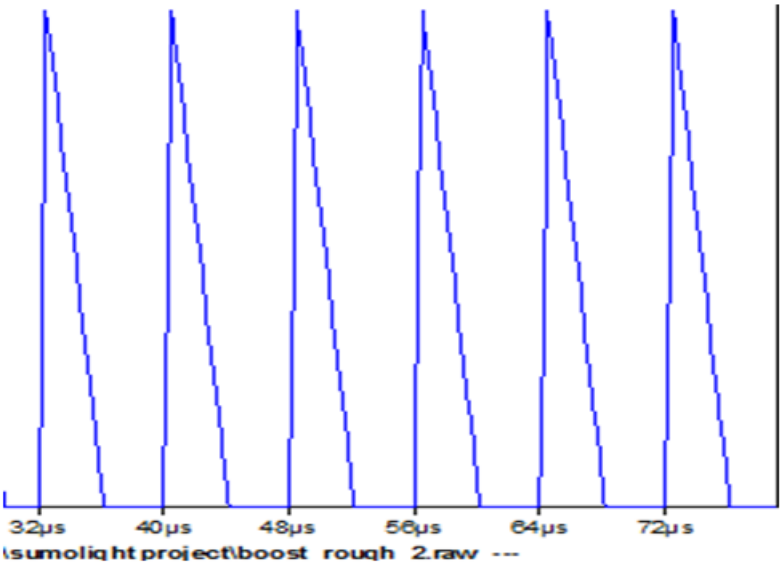


Here it is clearly visible that the voltage is dropped across the load .the tvs and tbu gives an over voltage protection to the circuit.

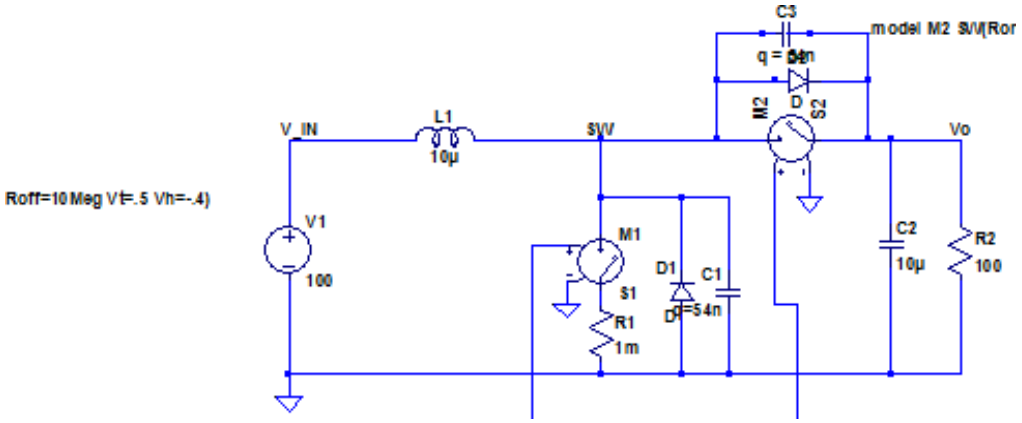
the output voltage is represented below which is extracted from the ltspice simulation with some approximation ..the out put increases until it reach the saturation and after that it maintains the value. the plot from ltspice is represented below for a 100 volt of dc input and other parameter remaining the same .



The plot for the current across the inductor is represented below for a dc input of 100 volt .



From the plot represented above it is clear that the current across the inductor goes to the peak and again comes down to zero and and the voltage across the source mosfet rises to approach the minimum switching loss. The complete circuit diagram is represented below (control loop excluded for clear visibility of the parameters)



IV. Conclusion

So here in this paper the detail about the zero voltage switching and the phase lock look is represented. so the basic idea of the zero voltage switching was to reduce the switching loss by waiting the current to react zero and then controlling the gate pulse. As a result of which the switching loss is completely reduced resulting a higher efficiency ..the two mosfet (switches) are controlled by the phase lock loop technique .where one switching puilse is treated as a masters pulse and the rest is treated as a slave pulse and the the slave pulse is generated after a delay of half of the switching period of the masters switching pulse.As a result of which the inductior current remains reasonable .without the phase lock loop techniquie the inductors current goes on increasing hence can destroy the entire circuit.

So the mat lab programming and simulation is represented above to calculate many parameters and to determine the relationship between them.

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