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A Review on Current-Mode CMOS Multiplier circuits with Improved Accuracy using Analog VLSI

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Abstract: *This paper is consisting on reviews of researches done on analog multipliers with better performances in many aspects. As there are two techniques exists in making analog circuits which are voltage mode approach and current mode approach, so taking the advantages of current mode techniques over voltage mode in mind in this paper we have reviewed only current mode analog multipliers. Analog multipliers since are useful in analog signal processing they have huge applications in our daily life devices and equipment, like watt meter, watt hour meter(power supply measurement), Densitometer, Acoustic Thermometer, oscillators and many more. These applications have their own interest as they are the part of the devices which Wegener all yuseinour daily life. The circuits made using current mode techniques are having better frequency response, low power consumption and also better temperature sustainability. We are also representing the working of two best current mode multipliers which we found, those are checked and implemented by 0.18um technology in Cadence Virtuoso and Hspice simulations of twares.*

Key wwords: *Current mode, Rectifier, Cadence Virtuoso, Hspice*

I. Introduction

A multiplier is a device that having three ports i.e. two is used for the as a input ports and one is used as a output port. The output of the multiplier is nothing but a multiplication of both inputs. If both input and output signals are voltages, the transfer characteristic is the product of the two voltages divided by a scaling factor, K, which has the dimension of voltage. Multipliers have many applications in analog systems and circuits. Modulator and mixer in communication systems are early applications of this block. Newer applications of this block are usage in implementing neural network and fuzzy logic systems. In a general point of view, we can classify multipliers in two categories of voltage and current.

In MOS voltage mode multipliers are classified in eight categories according to transist or region of operation, nonlinearity cancellation schemes, and signal injection method. But this classification doesnotinclude current mode multipliers. Current mode processing has more advantages than voltage mode. These advantages include wider band width, more linearity, lower power dissipation, simple rcircuitry etc. Most of current mode multipliers which are implemented intransist or level can be divided in two categories of strong in version and weak inversion. Although there are multipliers which are proposed based on blocks like OTA, CCII and different types of CDTAs and its derivatives. But most of these use BJT transistors and are notoptimized in the terms of power dissipation and areaconsumption.

Based on sub thres hold operated MOS transistors, the realization of multiplier/dividers requires simple architectures. So as to enhance the frequency response of the computational structures and to expand their 3 dB bandwidth, many analogsignal processing functions can be achieved by exploiting the squaring characteristic of MOStransistorsbiasedinsaturation.Inmultiplierstructureswerepresentedwithsingle-ended input voltages, the linearization of their characteristics being obtained using proper squaring relations between the input potentials. In order to implement the multiplication of two differential-input volt- ages, in multiplier circuits were described basedonmathematicalprinciples,similartothemethodsusedformultiplierswithsingleinputvoltages[1-5].

II. Literature Survey

The first research is based on the multiplier with low power consumption and lower linearity errors byusing current mode techniques in the CMOS multipliers. The result of this also shows the advantages ofcurrentmodeover voltage mode. The reasercher used the square law properties of the MOSFETs for designing the two new circuits which are able to multiply signals with better accuracy and low power consumption as well as simple architecture operates at low voltage input. There are two circuits presented and both perform well with current inputs. The circuits got improved in bandwidth due current mode where as it also get immuned to temperature variations. The two circuits with the combinations of current mirrors and current sources are proposed. Different W/Lratiosandcombinationsofbothnmosandpmosareused,circuitismadeon0.18umCMOStechnology[1]

The research presents a low power CMOS analog multiplier with better performance and simple design con- side rations. This design has low power utilization and having good linearity due to this design is very effective to use in analog circuits. The experiment is done in the SPICE simulation. The proposed circuitis working on voltage mode with low linearity error of almost 0.71.09 percentage and with huge band width performance of up to 1.98 1.02 Ghz. Circuit is also immune to noise effects, it is made on cadencetool.[2]

A CMOS analogue current-mode multiplier/divider circuit is presented, which is based on a dynamicbiasing applied at the body terminal of MOS transistors operating in both saturation and triode. Multiplier creates a feedback loop due to which enhance the accuracy and also enhance current swing . The multiplier has been fabricated using astandard0.18 um CMOS technology and it cosues almost 144 uWpower. The next circuit is based on the re-using of the same functional core for two circuit functions i.e. signal gain with theoretical null distortions and signal squaring.The most important circuit complexity is implementing the core of the structure, which is made easy in the circuits, both circuit area and power consumption per each realized function is strongly reduced in this method. The overall error of the transconductance amplifier is 0.4 percent and the approximation error for the squaring circuit is 0.27 percent, in the condition of a low-voltage low-power operation (a supply voltage of 1.5V and a medium current consumption of 50uA for each implemented circuit function[3][4]

III. Comparative Study of The Papers

From all the references which we had studied we found that on every parameters such as low power consumption, chip area, maximum bandwidth, linearity errors and technology used to make them, the multiplier which was designed by Cosmin Radu Popa in sixth reference is better of all. We have given all studied values of multipliers on every parameters in the tabular form given below with their authors. As we had found that among all ConminPopa's multiplier was better we also had done the hand calculations and simulations of his proposed idea of making the multiplier, those simulations and hand calculations are also shown below, using which one can understand the working of the circuit.

TABLE: Comparative study of analog multipliers

References	Techno logy [μm]	Supply Voltage [V]	Linearity Error [%]	Power Consum-ption [μW]	Chip Area [μm2]	Bandwi dth [MHz]
1] C. Sawigun, A. Demosthenous, and D. Pal, "A low-voltage, low-power, high-linearity cmos four-quadrant analog multiplier," in *Proc. 18th Eur.Conf. Circuits Theory Design, Aug. 2007, pp. 751–754.*	0.35	1.2				
2] A. Naderi, H. Mojarrad, H. Ghasemzadeh, A. Khoei, and K. Hadidi,"Four-quadrant CMOS analog multiplier based on new current squarercircuit with high-speed," in *Proc. IEEE EUROCON Conf., May 2009,*pp. 282–287.	0.35	3.3	1.15	240		44.9
3] S. A. Mahmoud, "Low voltage low power wide range fully differential CMOS four-quadrant analog multiplier," in *Proc. 52nd IEEE Int. Midwest Symp. Circuits Syst., Aug. 2009, pp. 130–133.*	0.25	+1, -1		326		
4] C.A De La Cruz-Blas, G.Thomas-Erviti, J.M. Algueta-Miguel, A. Lopez-Martin, "CMOS Analog current mode multiplier/divider operating in triode-saturation with bulk driven technique*" ElseVier Integration the VLSI ,* 2017	0.18	1.8	1.5	144	4050	62
5]Aram Bahramast, Syed JawadAzhari, SiavashMowlavi, "A NEW CURRENT MODE HIGH SPEED FOUR QUADRANT CMOS ANALOG MULTIPLIER" *24th Iranian Conference on Electrical Engineering (ICEE), 2016*	0.18	1.8		89.2	200	840
6a]Cosminpopa, "Improved Accuracy Current-Mode Multiplier Circuits With Applications in Analog Signal Processing" *IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS*, 2014	0.18	1.2	0.75	79.6	600	60
6b]Cosminpopa, "Improved Accuracy Current-Mode Multiplier Circuits With Applications in Analog Signal Processing" *IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS*, 2014	0.18	1.2	0.9	59.7	800	75

IV. Simulation result and Hand calculations

As in the reference number 6 by Cosmin Popa there are two design methodologies used, we are here presenting both of them with hand calculations and simulation results.
Design Methodology :

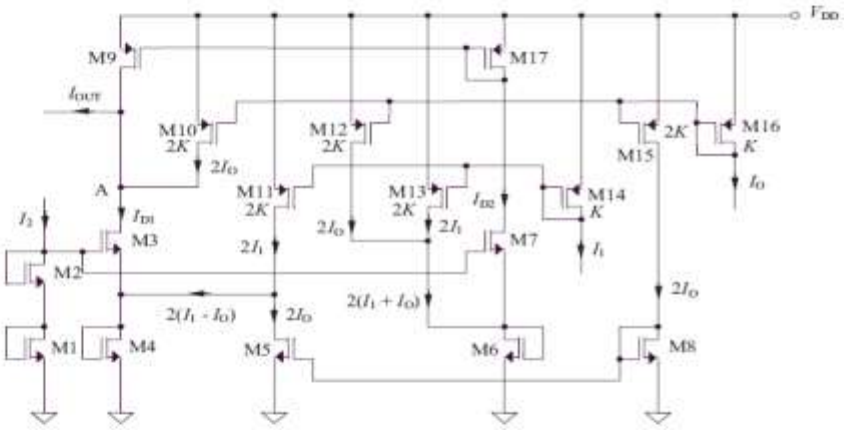

Fig. 4.1 First Design of multiplier

Expression of the output current in this design (in fig. 4.1) isIout $=ID_2 - ID_1 + 2I_O$ (by circuit analysis). Which gives the result of multiplier/divider circuit equation :Iout = $I_O\, I_1 / I_2$. For this circuit we first taken I0 = 40 µA (fixed) ,I1 = 0 to 10 µ A, I2 = 10 µa, 20 µA, 30 µa, 40 µA. And calculated the output current on simulation results as shown below in figure 4.2, as an example to understand for Io=40, I1=5, I2=10 we gorIout = 20 µA which can be verified with results also from fig. 4.2 also.

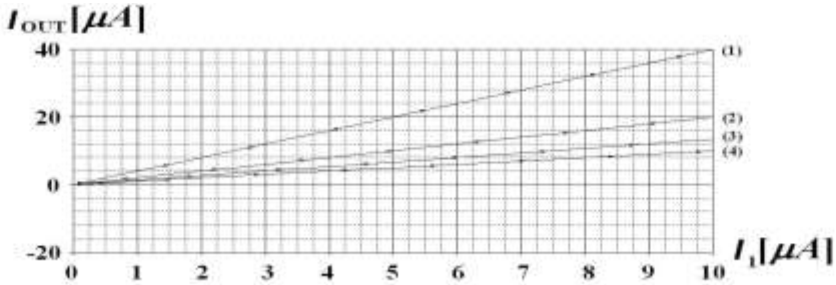

Fig. 4.2 Ioutvs I_1 current simulation graph

For current I2 we took I0 = 40 µA (fixed) ,I2 = 0 to 10 µ A, I1 = 10 µa, 20 µA, 30 µa, 40 µA
And found Iout, for example For Io=40, I1=5, I2=10 and gotIout = 20 µA. This also can be verified by fig. 4.3

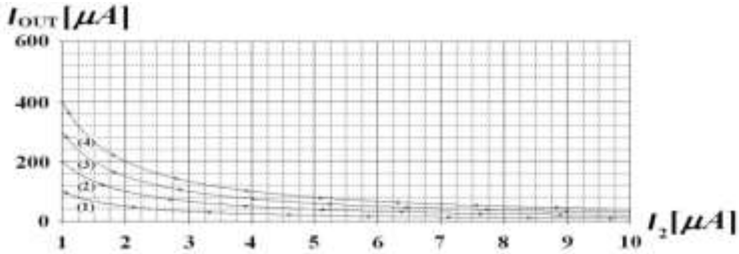

Fig. 4.3 Ioutvs I_2 current simulation graph

Author has also done transient analysis to get the frequency response of the circuit. In which he has taken I0 = 200µA/ 1MHz , and I2 = 300µA , I1 = 300µA / 60MHz and output shown in below fig 4.4. Found linearity error less tha 0.75%, can be observed in fig. 4.5

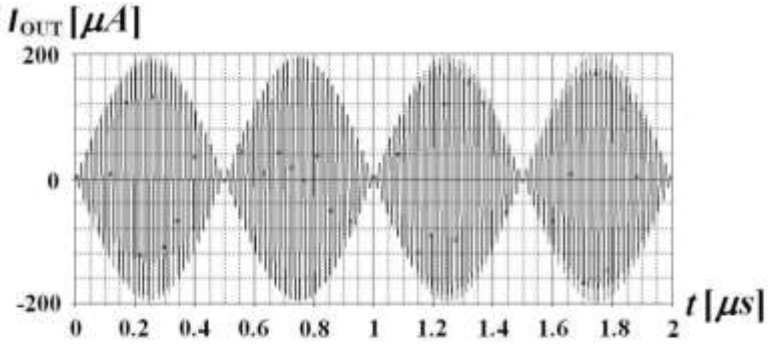

Fig. 4.4 Transient analysis of multiplier

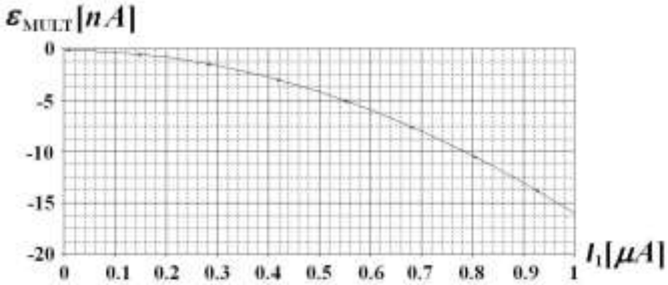

Fig. 4.5 Linearity error

Design Methodology 2:

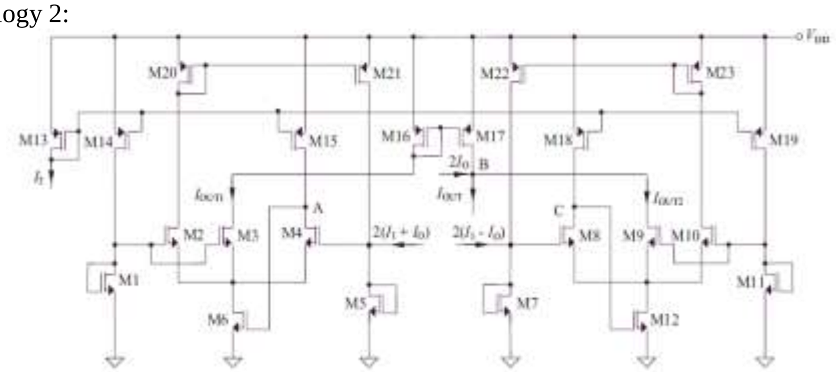

Fig. 4.6 Second Design of multiplier

Expression of the output current in this design (in fig. 4.6) isIout =Iout1 – Iout2 +2I0 (by circuit analysis)Which gives the result of multiplier/divider circuit equation : Iout = I_O I_1 / I_2. For this circuit we first taken I0 = 40 µA (fixed) ,I1 = 0 to 10 µ A, I2 = 10 µa, 20 µA, 30 µa, 40 µA And calculated the output current on simulation results as shown below in figure 4.7, as an example to understand for. For Io=40, I_1=6, I_2=10I_{out} = 24 µAwhich can be verified with results also from fig. 4.7 also.

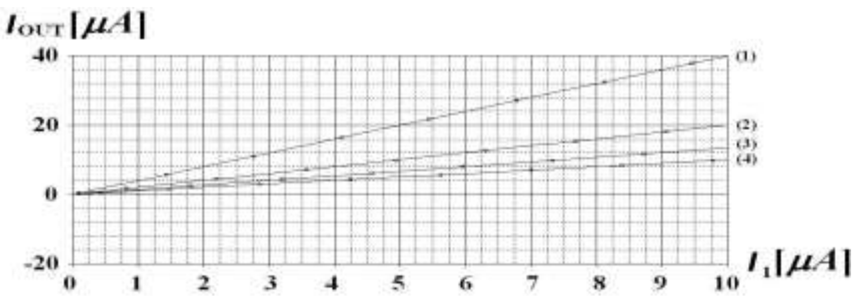

Fig. 4.7 Ioutvs I_1 current simulation graph

For current I2 we took I0 = 40 µA (fixed) ,I2 = 0 to 10 µ A, I1 = 10 µa, 20 µA, 30 µa, 40 µA
And found Iout, for example For Io=40, I_2=6, I_1=10. I_{out} = 24 µA. This also can be verified by fig. 4.8

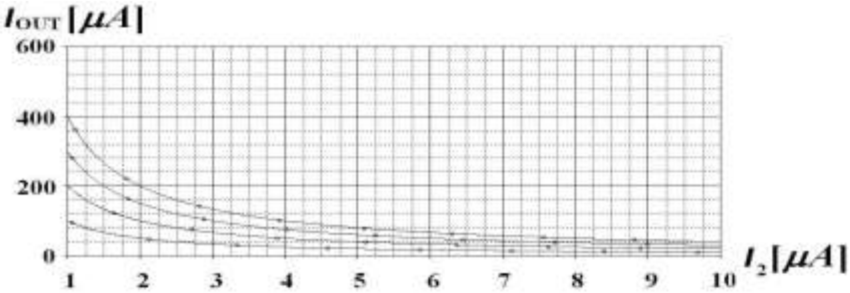

Fig. 4.8 Ioutvs I_2 current simulation graph

Author has also done transient analysis to get the frequency response of the circuit. In which he has taken I0 = 200µA/ 1MHz ,I2 = 300µA , I1 = 300µA / 45MHz and output shown in below fig 4.9. Found linearity error less tha 0.75%, can be observed in fig. 4.10

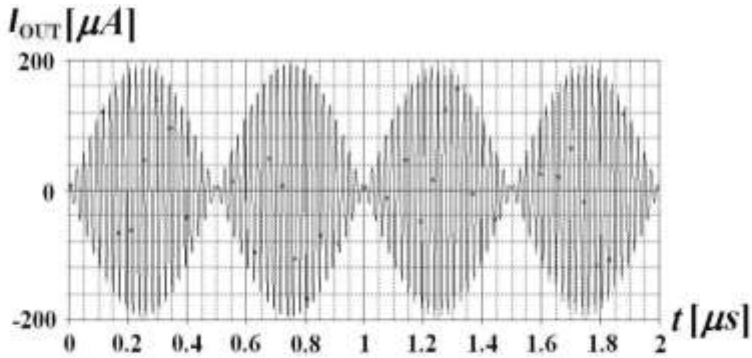

Fig. 4.9 Transient analysis of multiplier

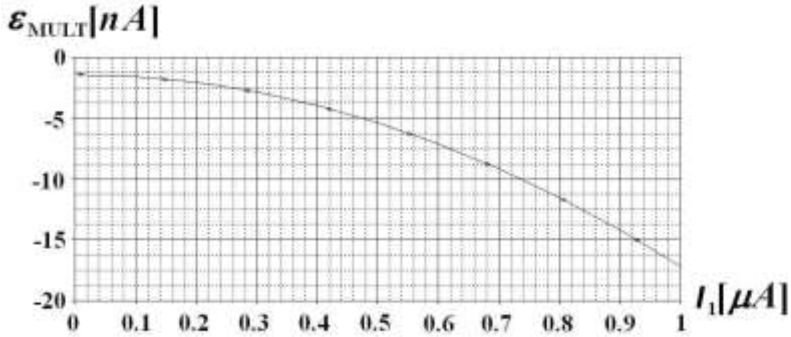

Fig. 4.10 Linearity error

V. Conclusion

After learning about the analog multiplier circuits and comparing the work of different authors on this topic it shows that the work which has presented is containing the most improved multiplier and divider circuits in context to the low power consumption and low linearity errors but it lags in bandwidth and chip area is more .

References

[1]. Cosminpopa, Improved Accuracy Current-Mode Multiplier Circuits With Applications in Analog Signal Processing,*IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS*, 2014

[2]. Cosmin Popa, CMOS Computational Circuits with Improved Performances,*IEEE EuroCon, Zagreb, Croatia, 1-4 July 2013*

[3]. C.A De La Cruz-Blas, G.Thomas-Erviti, J.M. Algueta-Miguel, A. Lopez-Martin, CMOS Analog current mode multiplier/divider operating in triode-saturation with bulk driven technique*" ElseVier Integration the VLSI ,* 2017

[4]. Aram Bahramast, Syed JawadAzhari, SiavashMowlavi, "A new current mode high speed four quadrant cmos analog multiplier" *24th Iranian Conference on Electrical Engineering (ICEE), 2016*

[5]. Cosmin Popa, Low-Power Low-Voltage CMOS Analog Signal Processing Circuits Using a Functional Core, *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2016

[6]. Bhushan D. Borkar, Ankita D.Tijare, VLSI Implementation Of Current Mode AnalogMultiplier, *IEEE ICCSP*, 2015

[7]. RobertM. Cuzner, GiriVenkataramanan, Current Source Rectifiers Con- duction Modes of operation, *IEEE Transactions on Industry Applications*, Vol. 51, No. 1, July 2014.

[8]. Mehmet Sagbas, ShahramMinaei, UmutEnginAyten, ”Component reduced current-mode full-wave rectifier circuits using single active component” *IET Circuits, Devices Systems*, Vol. 10, No. 1, January 2016

[9]. Zhenhua Wang, ”Full-Wave Performed Suitable Precision Rectification that is in Current Domain and Very for CMOS Implementation” *IEEE Transactions on circuits and systems-i: fundamental theory and applica- tions*, Vol. 39, No. 6, June 1992

[10]. SudhanshuMaheshwari, ”Current Controlled Precision Rectifier Circuits” *Journal of Circuits, Systems, and Computers*, Vol. 16, No. 1, 129138, 2007

[11]. Shahram MINAEI, Erkan YUCE, ”New Squarer Circuits and a Current- Mode Full-Wave Rectifier Topology Suitable for Integration” *Radio Engineering*, Vol. 19, No. 4, December 2010

[12]. Slobodan R. Djukic, ”Full-Wave Current Conveyor Precision Rectifier” *Serbian Journal of Electrical Engineering*, Vol. 5, No. 2, November 2008, 263-271

[13]. Cheng-Chieh Chang and Shen-Iuan Liu, ”Current mode full wave Rec- tifier and vector summation circuit” *Electronics Letters*, Vol. 36 No. 19, 14th September 2000

[14]. A.Faheem,N.Bhagat, U.P. Khot."CurrentModeFull Wave RectifierTopologyforIntegration".In:3rdIEEEInternationalConference on Recent Trends in Electronics, Information Communication Technology (RTEICT-2018); 2018..

[15]. A. Faheem, N. Bhagat, U.P. Khot. "Design of low voltage supply Current Feedback Operational Amplifier". In: 2nd International Conference on Inventive Communication and Computational Technologies (ICICCT 2018); 2018.