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A DSP Based Power Factor Correction Scheme for Switching Power Supplies

Shahzad Mobeen Ahmed[1], Faheem Ansari[2], Siddiqui Mohsin[3], Ashfaque Ahmad[4]

[12,3,4(]*Department of Electronics and Telecommunication Engineering, MMANTC, Abdul Latif Ali Al Shaya Faculty of Engineering, Mansoora, Pin.: 423203 Tal. Malegaon, Distt. Nashik Maharashtra. INDIA)*

Abstract: *Power factor correction (PFC) is necessary for ac-to-dc switched mode power supply in order to comply with the requirements of international standards, such as IEC-1000–3–2 and IEEE-519. Industry standard for the control of switch mode power supply (SMPS) systems has been analog control. Now with the advent of high speed, low cost Digital Signal Processors (DSPs) ICs, there has been an increased interest in digital control of SMPS. PFC can reduce the harmonics in the line current, increase the efficiency and capacity of power systems, and reduce customers' utility bills. An algorithm for digital control of power factor correction (PFC) is presented in this paper. Based on this algorithm, all of the duty cycles required to achieve unity power factor in one half line period are calculated by Digital Signal processor (DSP). A prototype of Boost PFC controlled by a DSP evaluation board was set up to implement the proposed control strategy. The experimental results show that the proposed strategy for PFC achieves near unity power factor.*

Keywords: *Digital control, power factor correction (PFC).*

I. Introduction

Power factor correction can reduce the harmonics in the line current, increase the efficiency and capacity of power systems, and reduce customer's utility bills. In order to achieve unity power factor in the switched mode power supply, many control methods are explored, including average current control [1], peak current control [2], hysteretic control [3], nonlinear carrier control [4], etc. All of these control methods have been implemented by the analog circuits. Several commercial integrated circuits (ICs) for current mode control, such as UC3854/3855 and ML4824 are available for the PFC applications. With the development of digital techniques, more and more control algorithms are implemented in power electronics circuits by the digital chips, such as microprocessors, microcontrollers or digital signal processors. One reason is that digital control can implement more complicated algorithms. Another reason is that digital control has many advantages over analog control, including programmability, adaptability, low part count and reduced susceptibility to environmental variations, etc. In addition, it is possible to achieve better performance in digital implementation than that in analog implementation with the same cost. As a result, it is prudent to explore digital control techniques for PFC application.

A digital control strategy of PFC using DSP is proposed in this paper to calculate the duty cycles required to achieve unity power factor in one half line period. A Boost converter controlled by these calculated duty cycles can achieve sinusoidal current waveform. One main advantage is that the digital control PFC implementation based on this control strategy can operate at a high switching frequency which is not directly dependent on the processing speed of DSP. The total computation time is less. This PFC control method can be implemented by a low cost DSP. The proposed PFC scheme has been implemented using a DSP (TMS320LF2407A) evaluation board from digital spectrum.

II. Principle of Digital PFC Control Strategy

The topology of Boost converter is shown in Figure 1. The proposed predictive PFC algorithm is derived based on the following assumptions.

1) Boost converter operates at continuous conduction mode.

2) The switching frequency is much higher than the line frequency, so the input voltage V_{in} can be assumed as a constant during one switching cycle. Based on these assumptions, when the switch S is on or off, the circuit of Figure 2(a). or 2(b). are obtained and the inductor current can be described as Equations (1) and (2), respectively.

$$L \frac{di_L}{dt} = V_{in} \qquad t_k \le t < t_k + d_k T_s \qquad (1)$$

$$L\frac{di_L}{dt} = V_{in} - V_o \qquad t_k + d_k T_s \le t < t_{k+1} \qquad (2)$$

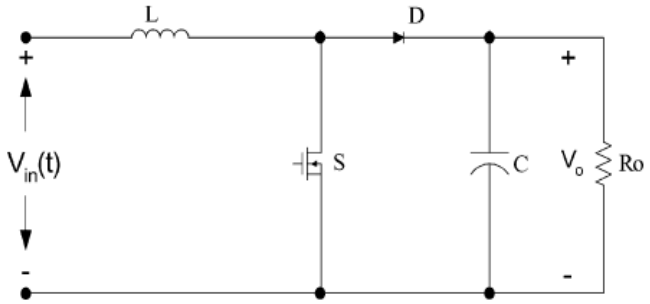

Fig. 1. Boost converter topology.

The discrete form for the inductor current at the beginning of $(k+1)^{th}$ switch cycle in terms of the inductor current at the beginning of K^{th} switching cycle can be derived from Equation (1) and Equation (2) as

$$i_L(k+1) = i_L(k) + \frac{V_{in}.T_s}{L} - \frac{V_o(k).(1-d(k)).T_s}{L} \qquad (3)$$

Where d(k) and T_s are the duty cycle and switching period. $V_{in}(k)$ is the input voltage in k^{th} switching cycle.

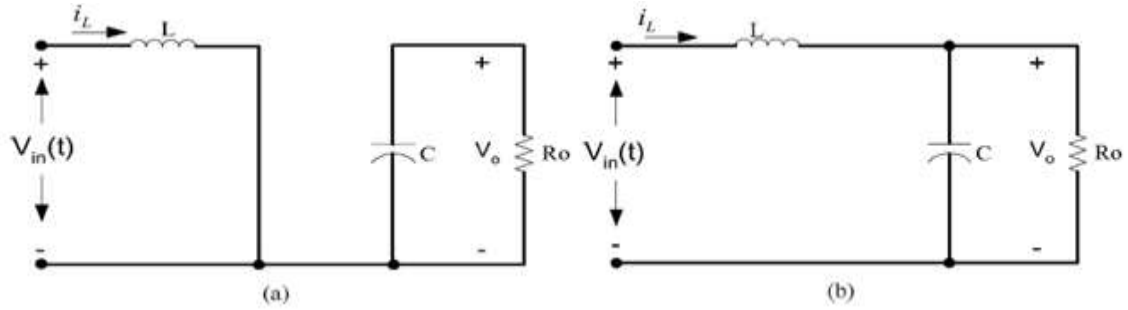

Fig. 2. Boost converter circuit. (a) switch is on and (b) switch is off.

$i_L(k)$, $i_L(k+1)$ are the inductor current at the beginning of k^{th} and $(k+1)^{th}$ switching cycles, respectively. When PFC is achieved, the inductor current should follow the reference current $i_{ref}(k)$, which is proportional to the rectified input voltage, as shown in Figure 3. At the same time, the output voltage should follow the reference voltage. That is

$$V_o(k) = V_{ref} \qquad (4)$$

$$i_L(k+1) = i_{ref}(k+1) \qquad (5)$$

$$i_L(k) = i_{ref}(k) \qquad (6)$$

Substituting Equations. (4) – (6) in Equation (3), we get

$$d(k+1) = \frac{V_{ref} - V_{in}(k)}{V_{ref}} + \frac{\left[i_{ref}(k+1) - i_{ref}(k)\right].\frac{L}{T_s}}{V_{ref}} \qquad (7)$$

Equation (7) gives the duty cycle in $(k+1)_{th}$ switching period i.e. d(k+1)
where,

$$i_{ref}(k) = v_{PID} \cdot \left|\sin(\omega_{line} \cdot t_k)\right| \qquad (8)$$

v_{PID} is the output of the PID regulator. It is determined by the closed voltage loop. $\left|\sin(\omega_{line} \cdot t_k)\right|$ is the rectified sinusoidal waveform with the line frequency. In DSP implementation, this sinusoidal waveform is

stored in a look up table. It should be noted from Equation (8) that has an exact physics meaning that is the peak value of the reference current. In DSP implementation, the limitation value of the PID regulator is easily determined based on the rated load according to this physics meaning. Equation (7) is used to implement power factor correction in this paper.

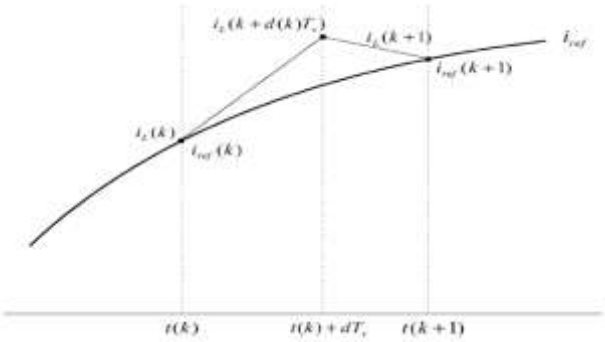

Fig. 3. Input current waveform and reference current in one T_s

The control block diagram for the Boost PFC converter is shown in Figure 4. The controller consists of output voltage controller (outer loop) and input current controller (inner loop). The slow response outer loop deals with maintaining the output voltage V_o within a tolerance band. The inner loop, which is much faster, synthesizes the output of the outer loop to correct the line current.

III. DSP Implementation

The software flowchart of the control strategy is shown in Figure 5. The main routine is described in Figure 5(a). The interruption routine, which is performed in every switching cycle, is shown in Figure 5(b). There are two main electrical values need to be sampled: rectified input voltage $V_{in}(t)$ and output voltage $V_o(t)$. The inner loop, which synthesizes the output of the outer loop to correct the line current, should be much faster than the slow response outer loop. The input voltage and output voltage could be sampled only once in about 100 switching periods.

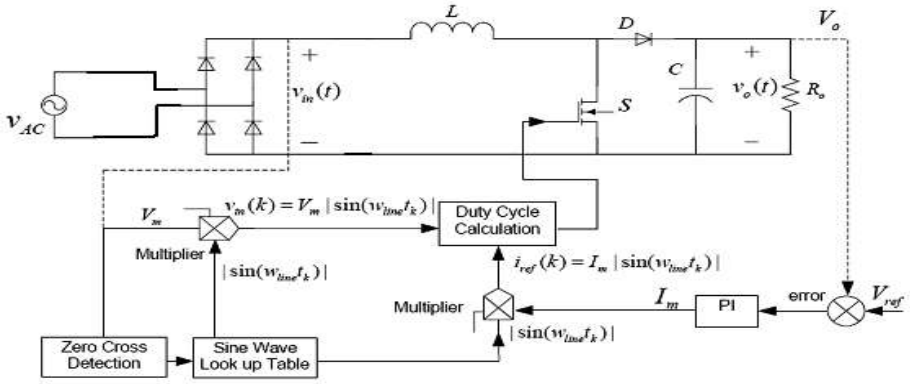

Fig. 4. Topology and control block scheme for Boost PFC

So the frequency of the main routine is 1kHz. Calculation of voltage PI controller, sampling of input voltage and output voltage, and part of the calculation about the differential equations could be done in the main routine.

By comparing the actual output voltage V_o with the desired output voltage V_{ref} and passing the error ($\Delta V = V_{ref} - V_o$) through a PI controller, the outer loop controller generates the amplitude of the reference current I_m. And it's easy to obtain the amplitude of the input voltage V_m by the sample data of the input voltage $V_{in}(t)$ in every 100 switching periods.

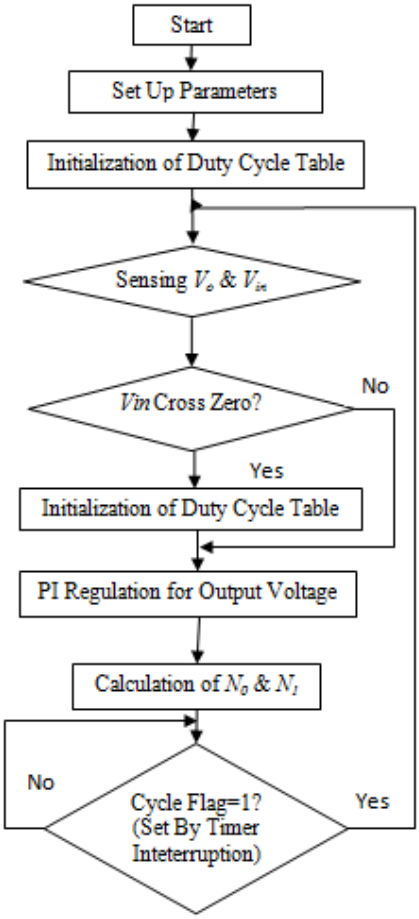

Fig. 5. (a) Main Routine

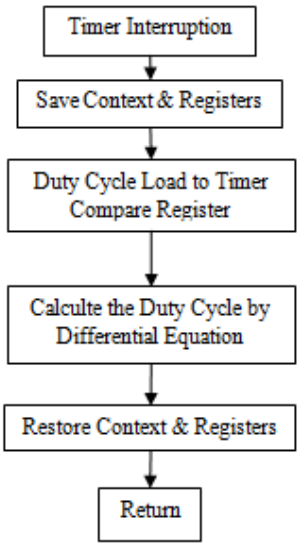

Fig. 5. (b) Interrupt Routine.

$|\sin(\omega_{line}\, t_{k+1})|$ is the rectified line frequency sinusoidal waveform, which is stored as a look up table. So the reference current $i_{ref}(k+1)$ in the $(k+1)^{th}$ switching period, which is proportional to the amplitude I_m and synchronous with the rectified input voltage, can be shown as in Equation (9). The advantage of using the look up table to generate $|\sin(\omega_{line}\, t_{k+1})|$ is that the sinusoidal input current waveform can be achieved under non-sinusoidal input voltage condition.

$$i_{ref}(k+1) = I_m\, |\sin(\omega_{line}\, t_{k+1})| \qquad (9)$$

And in every switching cycle, the input voltage also can be expressed as Equation (10).

$$Vin(k) = V_m\, |\sin(\omega_{line}\, t_{k+1})| \qquad (10)$$

Substituting Equation (9) and Equation (10) in Equation (7) and rearranging the duty cycle expressed as Equation (11)

$$d(k+1) = 1 - N_0 |\sin(\omega_{line}\, t_{k+1})| - N_1 i_{ref}(k) \qquad (11)$$

Where

$$N_0 = (V_m\, T_s - I_m\, L) / V_{ref}\, T_s$$
$$N_1 = L / V_{ref}\, T_s$$

The coefficients N_0 and N_1 can be obtained in the main routine, so in every switching period, besides loading the duty cycle from the memory to the timer compare register to generate the gate pulse, it only needs to calculate the duty cycle by the simple differential Equation (11) in the interruption service routine.

IV. Experimental Results

From the Table 1 and Figure 6, it can be observed that the supply power factor without power factor correction for a switching power supply for a load variation of 250Ω to 20Ω is from 0.2363 to 0.6941. The power factor with boost power factor correction for the same load variation is from 0.9691 to 0.9808. The power factor for different load currents is shown in Table 1 and Figure 6. It is shown that the power factor is

over 0.98 with the range from 25% to full load. The photographs of input voltage & input current and the harmonic components of input current without PFC are shown in Figure 7 and Figure 8 respectively.

Sr. No.	Load Current (Amps)	PF Without PFC	PF With PFC
1	0.2	0.2363	0.9691
2	0.4	0.2797	0.9724
3	0.6	0.2882	0.9727
4	0.8	0.3338	0.9745
5	1	0.3877	0.978
6	1.2	0.4395	0.9791
7	1.4	0.4954	0.9798
8	1.7	0.56	0.9801
9	2	0.6017	0.9805
10	2.5	0.6941	0.9808

Table 1. Comparison of **s**upply power factor with and without boost PFC by varying load

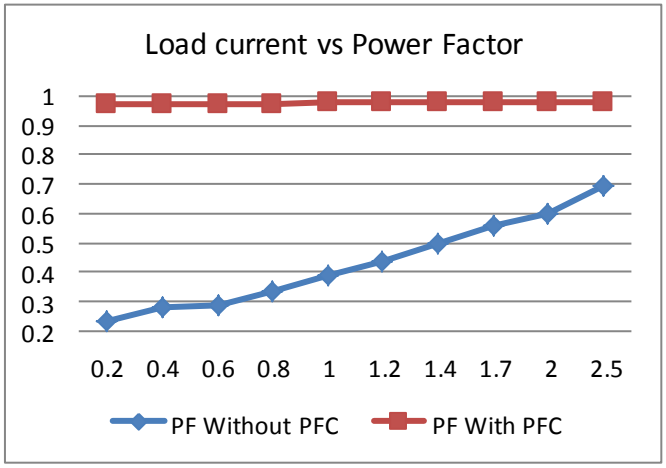

Fig. 6. Graph of Supply power factor with and without boost PFC by varying load.

The photographs of input voltage & input current and the harmonic components of input current with PFC are shown in Figure 9 and Figure 10 respectively.

The photograph in Figure 8. shows the supply voltage and the supply current waveforms without using the boost PFC circuit. It can observed from the waveforms that the supply voltage waveform is sinusoidal and the supply current wave form is non sinusoidal. The power factor and the total harmonic distortion (THD) under this condition are 0.6941 and 59.86% respectively. The photograph in Figure 9. shows the harmonic components of the supply current of Figure 8. It can be observed that the third harmonic component and other lower harmonic components amplitudes are large and comparable to the amplitude of the fundamental component.

Fig. 7. Input current & voltage waveforms without PFC.

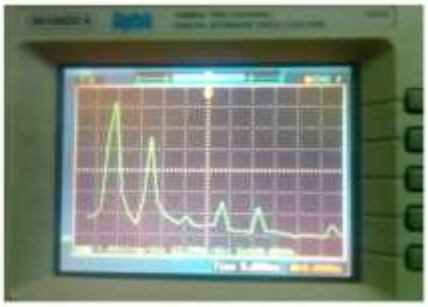

Fig. 8. Harmonic components of input current Without PFC

The photograph in Figure 10. shows the supply voltage and the supply current waveforms using the boost PFC circuit. It can observed from the waveforms that the supply voltage waveform is sinusoidal and the supply current wave form is also shaped nearly sinusoidal. The power factor and the total harmonic distortion (THD) under this condition are 0.9808 and 18.8% respectively. The photograph in Figure 11. shows the

harmonic components of the supply current of Figure 10. It can be observed that the third harmonic component and other lower harmonic components amplitudes are reduced to a large extent and are not comparable to the amplitude of the fundamental component.

Fig. 9. Input current & voltage waveforms with PFC

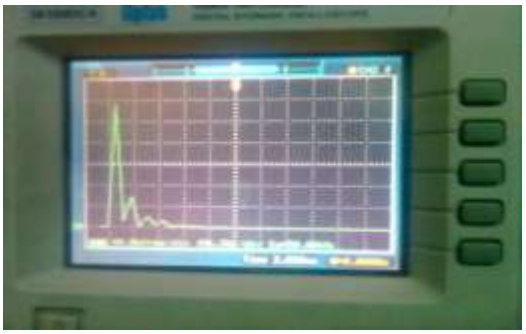

Fig. 10. Harmonic components of input current with PFC

V. Conclusion

In this paper, an algorithm is proposed for digital control PFC implementation. Based on the Boost topology, the algorithm is derived in detail. By using this control strategy, all the duty cycles required to achieve unity power factor in a half line period are generated by using a low cost DSP. Hence this scheme for PFC can be used instead of complicated analog control techniques.

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