IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
PP 47-51

32 bit DSP Processor for Communication System Application

Prasad Kulkarni[1], Dr.B.G.Hogade[2], Vidula Kulkarni[3]
[1]*HOD,Electronics and Telecommunication Department, MM Babasaheb Gawde Institute of Technology Mumbai, India.*
[2]*Professor,Electronics Department, Terna Engineering College Nerul ,Navi Mumbai, India.*
[3]*Assistant Professor, IT department, SCCT Sanpada , Navi Mumbai ,India.*

Abstract: *-.To design the computationally intensive functions available in Digital signal processor programmable logic devices offers an alternative solution. Programmable logic can provide increased DSP system performance at reduced system cost .Programmable logic combines the flexibility of a general purpose DSP plus the speed ,density and low cost of an ASIC implementation. This paper presents the challenges to design DSP processor and proposes architecture of Digital signal processors to compute FFT for communication system applications with special instruction set . The proposed design computes 8 point FFT in 46.95μs*

Keywords: - *FFT,DFT,DSP,ALU*

I. Introduction

The first efficient FFT algorithm was discovered by Gauss in the 18th century and rediscovered by Cooley and Tukey in 1960s. Later advances in the research of FFT algorithms include higher radix FFT, mixed radix FFT, split radix FFT etc. The FFT algorithms can be implemented on multiple platforms. The Architecture of DSP processors for FFT plays important role to compute FFT to fulfill the stringent requirement of high speed and power consumption. The FFT algorithm has been implemented on application specific integrated circuits (ASIC) as FFT processor. The Hardware design of FFT processor is tailored to fit high speed or low power specification but offers the less flexibility. The literatures were reviewed for different architectures where the FFT dissemination in time (DIT) computation affects the power (energy), throughput and area in the chip. These are the main constraints in VLSI implementation of architecture.

The multiprocessor architecture based on ring topology on single chip was used for power scalability. FFT size 8 to 4K provides the $0.1 * 10^{-2}$ μJ to 0.1 * 10 μJ normalised energy [1]. Chong *et al.* [2] have presented the energy efficient FFT/IFFT processor architecture for the applications (hearing aids) where the energy was the critical factor.. A. Anbarasan et *al.* [3] suggested ROM less FFT/IFFT processor to reduce the truncation error using fixed width modified booth multipliers. The PEs, delay line buffers and reconfigurable complex multipliers were used to compute FFT. Lin *et al.* [4] suggested pipelined FFT architecture for OFDM based UWB systems. This architecture reduces the number of complex multiplications. To increase the throughput in computation of real valued signal flow graph was modified to remove the redundant operations. Ayinala *et al.* [5] processed four inputs in parallel using processing element with conflict free memory address scheme. The throughput rate of radix-2 and radix-4 was increased by factor 2 to 4 times by using multipath delay commutator structure. This technique reduces the latency by the factor of 2 to 3.This type of architecture used for radix-2, requires $\log_2 N$-1 multiplexers, $2\log_2 N$ adders, N delay elements and 4log2N-4 multiplexers with 2/N throughput rate and N/2 latency [6].

In addition to power and throughput, area within chip is also an important parameter in VLSI design. Researcher presented architectures to reduce the area or gate count by reducing the numbers of component such as adders, multipliers etc. The review presented below gives the several methodologies in designing architectures of processor to reduce the area. The cost of complex multipliers and adders was saved by using distributed arithmetic in FFT architecture used for digital video broadcasting (DVB) [7]. The split radix FFT architecture without multipliers was implemented using distributed arithmetic which avoids the pre scaling on input data[8]. Salehi *et al.* [9] presented parallel pipelined architecture to compute real valued FFT along with hermitian symmetric IFFT. Yu and Yen [10-11] presented single path delay feedback (SDF) architecture was used to eliminate read only memory (ROM) which was used to store the twiddle factor. Xuan *et al.* [12] presented hierarchical design of an ASIP for FFT using scalable array structure with the 8 point butterfly unit (BU). The processors designed with Harvard architecture with special instructions also compute the FFT [13-16].

The objective of this paper to review the challenges in DSP designs and suggest the methodology to design DSP processor suitable to Compute FFT for UWB applications. This paper is organized in the six sections. Section II presents the challenges in FFT architectural design, section III describes the FFT

computations, section IV describes the architecture, and section V and section VI describes result and conclusion.

II. Challenges in Architectural Design

Mostly reviewed challenges in FFT architectural design are mentioned below but not limited to

1. The VLSI architectural design varies with the applications that decide the throughput, power dissipation and area occupied within chip.
2. The FFT input decides the computation time and latencies. Large numbers of inputs consumes more time, energy.
3. Different methodology is adopted to compute FFT in frequency and time domain.
4. The computation of real valued signal modifies the flow graph.
5. Reconfigurable architectures are the midway solutions within ASIC and software programmable general purpose DSPs and has very long instruction word.
6. Asynchronous approach in design reduces power consumption but increases the area as compared with synchronous approach.
7. The distributed arithmetic uses lookup table which is impractical for implementation using programmable logic devices.
8. The systolic approach was used for long length FFT in which throughput rate was decided by number of multiplexers used in design.

Processing elements, adders, delays and interconnections decides the throughput and complexity of the control.

III. FFT computation

In the design of a DSP system, two fundamental tasks are involved, viz (i) analysis of input signal and (ii) design of processing system to give the desired output. The DFT and FFT is very important tool to carry out these tasks. They can be used to analyses a two dimensional signal. The FFT algorithm eliminates the redundant calculation and enables to analyses the spectral properties of signal. They offer rapid frequency domain analysis and processing of digital signal, and investigation of digital systems. The FFT also allows time domain signal processing operations to be performed equivalently in frequency-domain. The fig.1 describes the flow graph to compute the 8 point FFT.

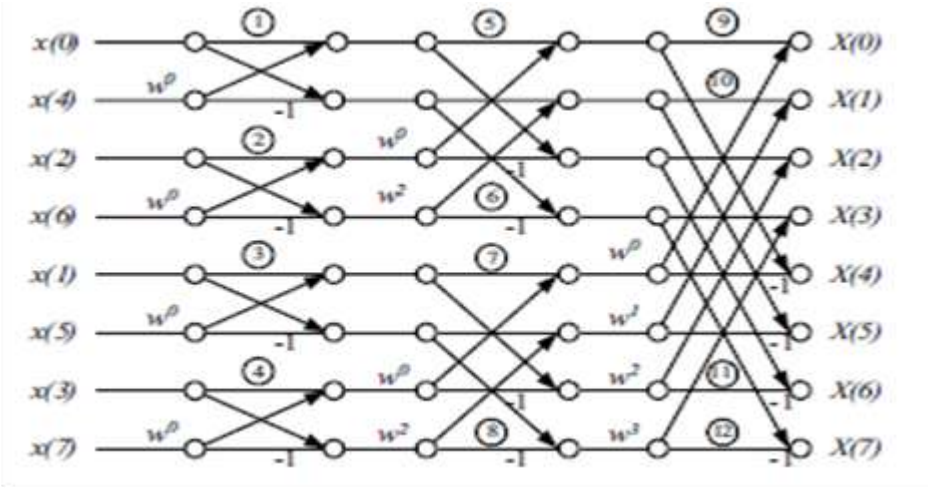

Fig. No. 1 Signal flow graph for 8 point FFT

IV. Architecture of DSP

The proposed architecture is based on Harvard architecture type .The program memory and dual port data memory is separately designed. The Program memory holds the instructions to compute the FFT .The IEEE 754 standard single precision floating-point format is used represents the samples. The register size is 32 bit and holds the samples or operand. The ALU performs floating point addition, subtraction and multiplication. The real and complex data are treated separately. The serial port is also included to import or export the data serially. The fig.2 shows the architecture of proposed DSP[13]. The same architecture is used for computation of FFT in frequency domain.

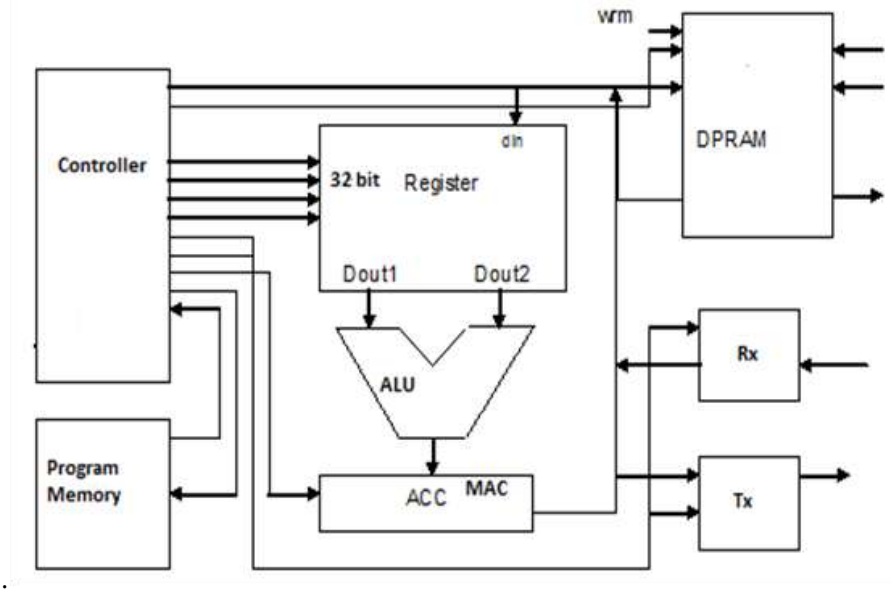

Fig. No 2 Proposed Architecture of DSP

V. Result

The given architecture is simulated for 8 point FFT computations using Active-HDL1.4. The computation time for floating point and addition and subtraction operations is also measured since they are the key performer in FFT computation. The addition takes 16.4 μs and multiplication takes 19.5μs.. Fig. 3 shows the simulation of addition where X=01400000h and Y=01400000h i.e. X=3d and Y=3d. The sum of X and Y is 6d i.e. Z= 02400000h. FOVF,FUNDF and FZERO overflow, underflow and zero flag and not active in this addition. Fig. 4 shows the computation of FFT. DFT of sequence x(n)={1,2,3,4,4,3,2,1} using DIT algorithm is used to compute the FFT.

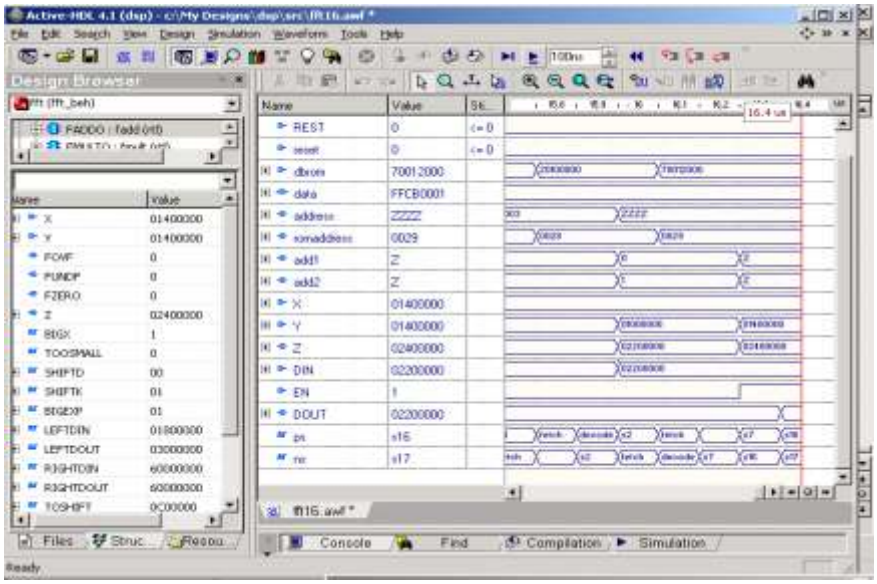

Fig. No.3 Simulation of addition

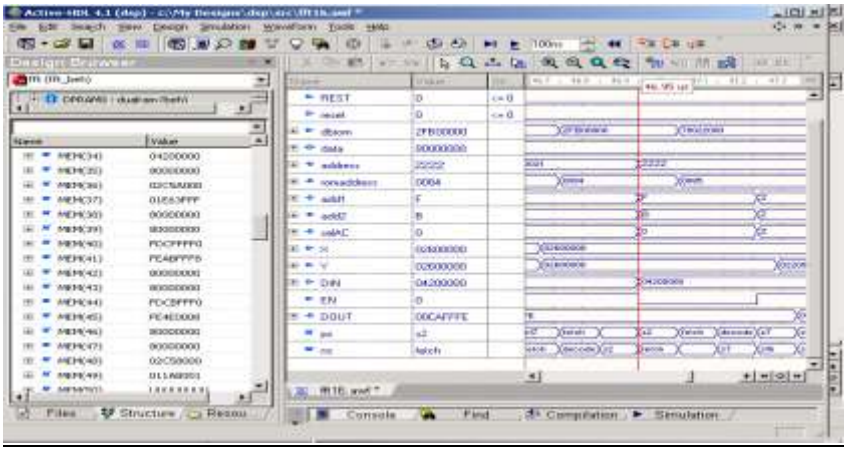

Fig.No.4 Simulation of FFT

The inputs *X(0)* to *X(7)* are initially moved in to DPRAM from location 0000H to 0007H. The twiddle factors are stored from location 0008H to 000FH.The twiddle factor is decomposed in real (Twr) and imaginary parts (Twi) .e.g. $W_8^3 = (e^{-j2\pi/8})^3 = -0.707 - j0.707$ is Twr(3) = - 0.707 is available at memory location 000Bh and Twi(3) = -j0.707 is available at memory location 000Fh. All the inputs and twiddle factors are represented in IEEE 754 single precision format. The inputs are moved to the general purpose registers and using arithmetic instructions FADD, FSUB, FMUL outputs of the stages are calculated. The real and imaginary parts are processed separately. The final output is also available from location 0022H to 0031H. The entire FFT algorithm is computed in 46.95µs with clock of period of 100ns.

VI. Conclusion

The proposed architecture is suitable to compute 8 point FFT in DIT as well as in DIF form. The input sequences are loaded in serial or parallel form and FFT out sequence is also read serially or in parallel form. The dual port ram is used in the design to interact with the external peripherals. The design is free from delay, feedback and commutator. The processor computes the sequence in 46.95µs to suit the communication applications.

.

References

[1]. Guichang Zhong, Fan Xu and Alan N. Willson,“ A Power-scalable reconfigurable FFT/IFFT IC based on a multi-processor ring”, IEEE Journal of solid-state circuits, vol. 41, no. 2, February 2006,p.p. 483-495 .

[2]. Kwen-Siong Chong, Bah-Hwee Gwee, and Joseph S. Chang, “Energy-Efficient Synchronous-Logic and Asynchronous-Logic FFT/IFFT Processors”, IEEE journal of solid-state circuits, vol. 42, no. 9,September 2007,p.p.2034-2045.

[3]. A.Anbarasan and K. Shankar, “Design and Implement of Low power FFT/IFFT Processor for wireless Communication”, Proceedings of the international Conference on pattern recognition, Informatics and Medical Engineering , March 2012.

[4]. Yu-Wei, Hsunan-Yu Liu and Chen-Yi Lee,“ A 1-GS/sFFT/IFFT Processor for UWB Applications”, IEEE Journal of solid-state circuits, vol. 40, no. 8, August 2005,p.p. 1726-1734.

[5]. Manohar Ayinala,Yingjie Lao and Keshab K. Parhi, “An In Real Place FFT Architecture For real valued Signal”, IEEE transactions on Circuits and systems-II, July 2013,p.p.1-5,.

[6]. Chao Cheng and Keshab K. Parhi,“High-Throughput VLSI Architecture For FFT Computation”, IEEE Transactions on Circuits and Systems-II, Vol. 54, No. 10 , October 2007, p.p. 863-867.

[7]. Richard M. Jiang, “An Area-Efficient FFT Architecture for OFDM Digital Video Broadcasting”, IEEE Transactions on Consumer Electronics, Vol. 53, no. 4, November 2007,p.p. 1322-1326.

[8]. Sunil P. Joshi and Roy Paily, “Distributed Arithmetic based Split-Radix FFT”, J Sign Process Syst. Springer Science, May 2013.

[9]. Sayed Ahmad Salehi,Rasoul Amirfattahi and Keshab K Parhi, “Pipelined Architecture for Real Valued FFT and Hermitian-Symmetric IFFT With Real Data Paths”, IEEE transactions on circuits and systems—II, vol. 60 , August 2013,p.p.507-511.

[10]. Chu Yu and Mao-Hsu Yen, “A Low power 64-point Pipeline FFT/IFFT processor for OFDM applications”, IEEE Transactions on Consumer Electronics, , vol. 57 , no. 1, February 2011,p.p.40-45.

[11]. Chu Yu and Mao-Hsu Yen, “An Area Efficient 128 to 2048/1536-Point Pipeline FFT Processor for LTE and Mobile WiMax System”, IEEE Transactions on Very Large Scale Integration (vlsi) Systems, vol. 23, no. 9, September 2015,p.p.1793-1800.

[12]. Xuan Guan, Yunsi Fei and Hai Lin , “Hierarchical Design of an Application Specific Instruction Set Processor for High-Throughput and Scalable FFT processing”, IEEE Transactions on Very Large Scale Integration (vlsi) Systems, vol. 20, no. 3, March 2012,p.p.551-563.

[13]. Prasad A. Kulkarni, Dr. Vijay Wadhai, D.R. Mehta and Vidula Kulkarni, “Reconfigurable DSP-FFT design for mobile communication”, International conference on “Contours of Computing Technology”, Springer Publication, March 2010.p.p.289-292.

[14]. Vidula Kulkarni, Dr. B.G. Hogade, Prasad Kulkarni, “Designing of Arithmetic Logical Unit for Digital Signal Processor” ,International Journal of Advance Foundation and Research in Science and Engineering ,Vol. 1,Special Issue -Vivruti , March 2015, p.p.1-4.

[15]. Vidula Kulkarni ,Dr. B.G. Hogade, Prasad Kulkarni, " Design and Simulation of Digital Signal Processor for ultra wide band communication system application" , Abhinav International Monthly Refereed Journal of Research in Management & Technology, Vol -5, Issue 5, May 2015, p.p 49-55.

[16]. Prasad Kulkarni, Dr. B.G. Hogade, Vidula Kulkarni, "Simulation of Digital Signal Processor – FFT for Communication System Applications" , ACM Digital Library, Proceeding ICTCS 16 Proceeding of the second International Conference on Information and Communication Technology for Competitive Strategies, Article No. 109, ACM. New York, NY, USA 2016, ISBN: 978-14503-3962-9 DOI 10.1145/2905055.2905325.