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FPGA Impementation of Series Harmonic Compensation For Single Phase Inverter

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Abstract: *An unconventional multiplexing technique applied harmonics extraction method is presented in this paper. single phase inverter programmed for the reduction of harmonics in output voltage. These harmonics components of the voltage are highly distorted current signals particularly when the inverter supplies the non linear loads. To obtain a very low harmonics large feedback around the noise signal has been employed. The multiple observers yield very pure in-phase and quadrature voltage signals for use in the outer loop and similar signals for stabilizing the inner current loop. The Inverter could be modeled as a feed back control system with the fundamental component of the voltage as the desired*
output while the voltage harmonics take the role of noise creeping into the output.To obtain a very low total harmonic distortion in the voltage waveform, the well-known control strategy of using a very large feed back around the noise signal has been employed
Keywords: *Harmonics, linear, quadrature, feedback, distortion.*

I. Introduction:

Stand-alone inverters are commonly used in the case of power failure, to deliver power for critical loads, which demand purely sinusoidal voltage at the specified magnitude frequency, and low total harmonic distortion (THD). The THD in industry should not exceed 5% as per Fixed may not perform well, particularly when the operating frequency drifts far away from the set resonance frequency .Alternatively, active filters can be employed. Many control methods have been proposed basically for obtaining pure sinusoidal output with good voltage regulation and fast dynamic response. Sinusoidal pulse width modulation (SPWM) schemes for stand-alone inverters have been shown to perform well with linear loads . However, with nonlinear loads the SPWM scheme does not guarantee low distortion in the output voltage.

The availability of low cost microprocessors has led to discrete-time methods, such as repetitive control sliding mode control, and deadbeat control are involved to improve the performance. To get zero steady-state error in the output voltage and fast response virtual inductor, capacitor and a resistor were used .while internal model control scheme (IMC) was employed. The control methods . employ twofeedbackcontrol loops. The inner loop is used for current control and the outer loop is used for voltage control.Many of these methods have not specifically considered thereduction in distortion due to nonlinear load .

The emergence of FPGAs has drawn much attention due to their shorter design cycle, lower cost, and higher\density. The simplicity and programmability of FPGAs make them a most favorable choice for prototyping digital systems. when comparing the dynamic performance and control capabilities in PWM-controlled Power converters FPGA based digital techniques are better than DSPs Basically a Luenberger observer (simple observer) can be used for obtaining the filtered fundamental component from the periodic output voltage and current waveforms,which leads to the indirect estimation of the total harmonicsin the output voltage due to the nonlinear loads, TheInverter can be modeled as a feed back control system with2 VLSIfeed back around the noise signal has been employed.

II. Block Diagram:

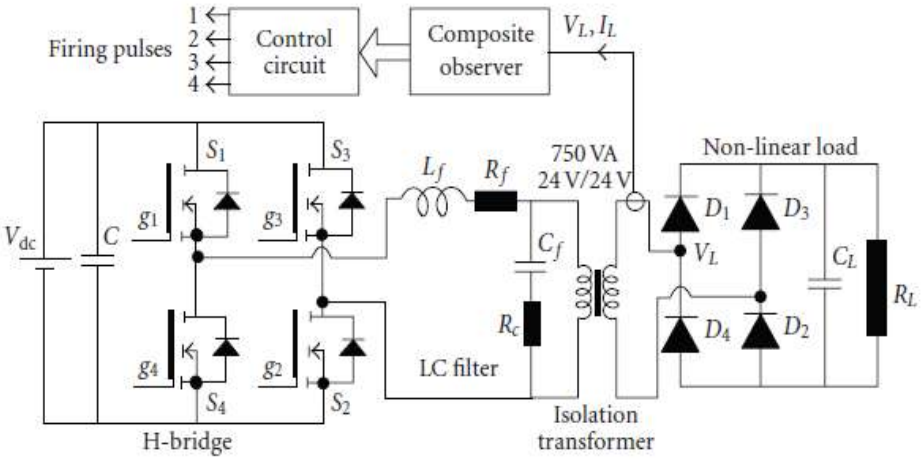


FIGURE 1: Single phase inverter circuit under rectifier load with RC filter.

Working:

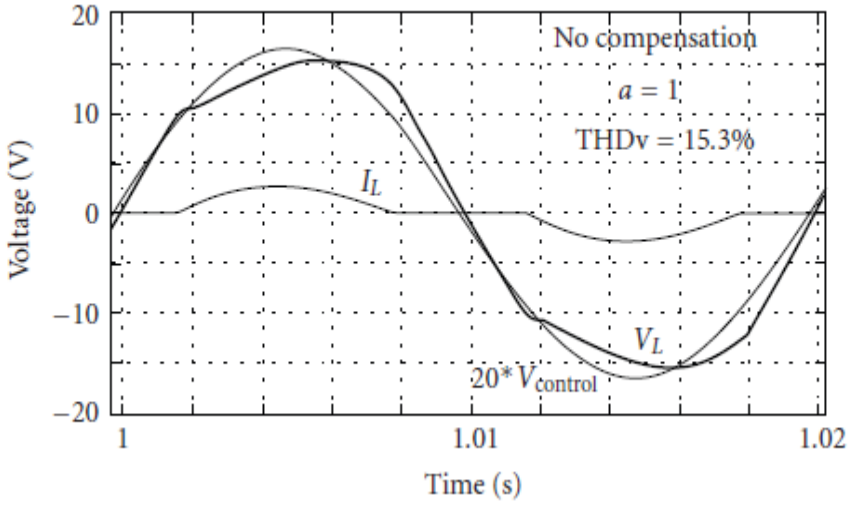
The control scheme for reducing harmonics in the inverter is shown . The steady-state error-vector[evd, evq] between the desired D-Q component values and theactual D-Q component values obtained from the voltage observer is processed through PI controllers to obtain D-Q current references. Similarly, using another simple observer ,the fundamental in-phase and fictitious quadrature current signals are estimated. This facilitates transformation of the current to the D-Q frame.

The current error-vector [eId, eIq]in the D-Q frame is processed by simple gain elements (k)even though PI or lead type compensators could have been used.The steady outputs of the two controllers in the current loop are converted into the in-phase and quadrature time signals, via the single-phase-inverse Park transform. The two time signals are added to get the sinusoidal reference signal for pulse width modulation as shown in Figure 8. Without any compensation for harmonics, the output voltage is heavily distorted for a "non liner load", consisting of a rectifier driving a RC load (10Ω_1mF). The THD v is about15.34% even though the control signal appears to be a pure sine wave. The distorted output voltage, pulsed load current ,and the control voltage are shown in Figure 9. The distortion is mainly due to the voltage drop caused by the harmonic currents in the series R-L filter of the inverter.

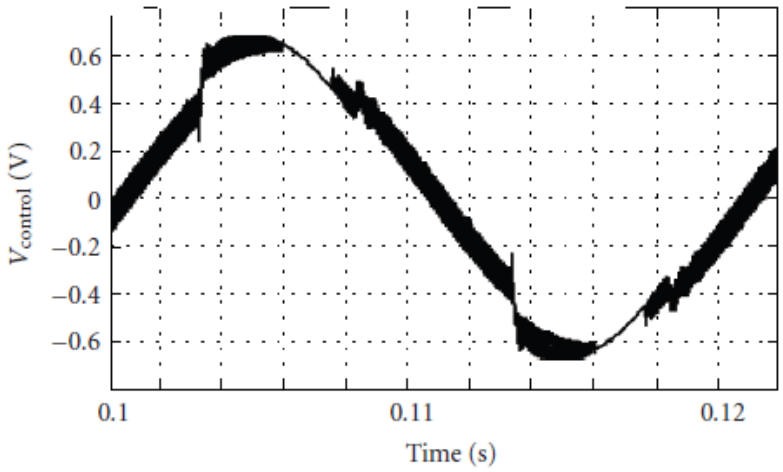
Fpga Schematic Controller:

The overall hardware implementation circuit of the singlephase inverter . The measured output voltage and current are normalized to unity using gv and gi,which include voltage divider as well as the analog amplifiergains. Inside the FPGA the maximum voltage and currentvariables are made equal to unity. Hence the same setupcould be easily extended to any voltage or current levels, bysuitably adjusting the external range setting devices.The implementation consists of two separate ADCs forfeeding in the load voltage and current into the control circuit A serial +5V, 12-bit, MSOP-8package analog-to-digital converter ADS7835 was interfacedwith Cyclone II FPGA. Handshaking between FPGA andADS7835 is through 3 signals named Convert, Clock, andData. The Convert and Clock are input signals to ADC fromFPGA, while the converted Data goes into the FPGA. Sincethe level of the digital I/O signals for the FPGA is at 3.3V andthe ADC operates at 5V, a digital buffer (16 pin 74HC366)has been provided for the two channels. The serial data fromADS7835 has been converted into 12-bit parallel data in the integer format in the FPGA, Since the integer signals are to be normalized to 18-bitsfloating point, that is, [3 : 15], further conversion to floatingpoint is necessary which is illustrated in Bit-bybitextraction and addition in the floating point has beencarried out for achieving this. These two procedures wereincorporated as subsystems.The measured current and the voltage variables available in the floating point format are fed to separate observers.

Software Output:



With no harmonics in using a controlling technique of fpga with feedback



Output 2. Control signals which yields a pure output waveform

III. Conclusion:

The reduction of distortion in the voltage waveform in single phase Inverters, caused by the currents drawn by non linear loads, can be easily done by feeding back the instantaneous harmonic content of the voltage signal. This harmoniccontent is computed on-line by a composite observer in the voltage loop, which incidentally can also be used for obtaining the fundamental voltage signal for keeping theoutput voltage at the desired level. A simple observer in the inner current loop serves the purpose of estimating the fundamental component of the load current.

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