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Reduction of Leakage Current using Self Controllable Voltage in 4x4 Dynamic RAM Cell

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Abstract: *With the rapid development in the technology to improve the semiconductor chip performance, system designers focused on the circuits for their reliability, low power dissipation, low power consumption, chip density and leakage current. The designers reduced each of these for improved performance, reduced cost and chip area. CMOS technology increased in level of importance to the point where it now clearly holds the center stage as the dominant VLSI technology. Along-with these improvements, the memories have provided with components of considerable capability and extensive application. The main memory is usually of the random access type. The random access memory is one in which the time required for storing (writing) information and for reading information is independent of the physical location (within the memory) in which the information is stored. The bulk of memory chip consists of the cells in which the bits are stored. In this paper we are implementing a low cost DRAM 4x4 (Dynamic Random Access Memory) with Self Controllable Voltage Level (SVL) technique used to reduce the leakage current in the design to 55%. Simulation is done by using DSCH and Microwind 3.5*

Keywords - *DRAM, Self Controllable Voltage, Low Leakage Current, Reduced Cost, Performance*

I. INTRODUCTION

The memories are designed to store large quantities of digital information. For reducing the density, pin counts can be reduced which will reduce the value at the expense of performance. The Word-Line (WL) is declared by raising variety of stroboscope signals. By raising the row access, stroboscope signal provides the mutual savings bank memory a part of the address line through which word decryption method can be initiated. A part of address (LSB) is then applied and also the column access stroboscope signals are declared.

A very careful temporary arrangement of the signal interval is required for proper operation of memory. Essentially, the signals square measures are used as clock input to the memory module. As DRAM (Dynamic Random Access Memory) is volatile in nature, it loses its memory once the power is turned off. Thus, it should be refreshed periodically with V_{DD}. DRAM needs additional peripheral electronic equipment [13].

1T DRAM basic memory cell consists of one access NMOS, storage electrical device, management input like word line (WL), data I/O and bit line. DRAM has little cell space compared to SRAM, extremely integrated, low cost and is widely used as main memory. But it also requires cyclic refresh and is of medium speed.

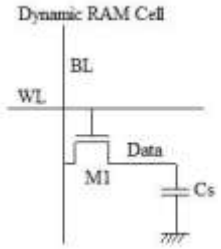

Fig. 1 Basic One Transistor Dynamic RAM Cell

Random access means that the processor will access any part of the memory at random instead of having to proceed serially from some foundation. DRAM is thus dynamic and not like static RAM (SRAM).

The capacitor in a DRAM memory cell leaks meanwhile. It needs to be refreshed periodically or it will discharge to 0. Dynamic RAM has to be dynamically refreshed all of the time or it forgets the information. The downside of all of this refreshing is that it is time consuming and slows down the memory. The storage cells must be refreshed or given an electronic replacement charge every few milliseconds.

The DRAM is far cheaper per cell; DRAM has larger storage capability per unit of surface than SRAM. In this paper, we are implementing the 4T DRAM with Self-controllable Voltage Level technique within the implementation of 3T DRAM. The design is using a four transistor DRAM to reduce the average dynamic power dissipation with respect to the frequency and the load capacitance to show the amount of power dissipated by the two logic families.

The word ADIABATIC originates from a Greek word used to describe the thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat.[1] In electronic computers, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in the circuit.

However, one can reduce the energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions. The signal energy is stored in the circuit capacitances are thus periodically recycled for being dissipated as heat. The adiabatic logic is also known as Energy Recovery CMOS. It is important to note that the fully adiabatic operation of the circuit is an ideal condition which may only be achieved approached asymptotically as the switching process is slowed down.

But in practical cases, the energy dissipation associated with a charge transfer event is usually composed of both adiabatic and non-adiabatic components. Therefore, reducing all the energy loss to zero may not be possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems.

This paper is organized in three main sections. Section I discusses the existing design and drawbacks of 3T-DRAM. Section II provides the proposed 4T DRAM design scheme. Section III discusses the results for Self Controllable Voltage Level memory design. Major points to consider in section III are low cost, low leakage current and improved performance.

II. DESIGN PROCEDURE

Most of the work in circuit current discharge analysis and reduction have stressed during a combinatorial circuits and successive circuit. Memory circuit element includes additional attention to style if discharge current is observed. Varied gate leak reduction methodologies are represented within the literature such as W. K. Luk et. al. offers a unique Dynamic Memory Cell with internal voltage gain[1]. H. J. Yooet. al. have developed an occasional voltage high speed self-timed CMOS logic for the multi giga-bit synchronous DRAM application [2].

John E. Leiss, Pallab K. Chatterjee and Thomas C. Hol-loway provide the concept of dram style victimisation the Taper-Isolated Dynamic RAM Cell [3]. G. W. Taylor et. al. have developed a punch-through isolated RAM cell [4]. The idea regarding leak model as well as source-drain partition [5].The font size for **heading is 11 points bold face** and **subsections with 10 points and not bold.** Do not underline any of the headings, or add dashes, colons, etc. Power Dissipation Analysis and improvement for Deep Sub-micron CMOS Digital Circuits shown in [6].

The important fundamentals of recent VLSI devices [7] and principles of CMOS VLSI style [8] have been developed. The device style pointers for floating channel kind encompassing gate electronic transistor (FCSGT) DRAM cells with high soft error immunity is represented during its design [9]. The 3 structure studied, solely the Sidewall Sealed MSL (SSMSL) may be a viable for the 0.6 m-pitch isolation of 256Mbit DRAM [10].

Two leak management electronic transistors (a p-type and a n-type) inside the computer circuit that the gate terminal of every Leak Management Transistor (LCT) is controlled by the supply of the opposite shown in [11]. Transient effects of the floating body should be thought about once planning for long information retention time [12]. The utilization of the minimum idle time parameter, as a metric for evaluating completely different leak management mechanisms, is shown in [13].

III. PROPOSED METHOD

V_{DD} used in this circuit design is 1.2V. Also, we have de-signed the DRAM memory at 0.25 m CMOS technology. The figure shows the schematic of four transistor dynamic memory cell in which the read and write operation is performed when M3 and M4 are in ON state. If M3 and M4 are in OFF state, read and write operation is not performed. The steady-state voltage is given as $V_{CC} = V_{DD} - V_{TH.}$

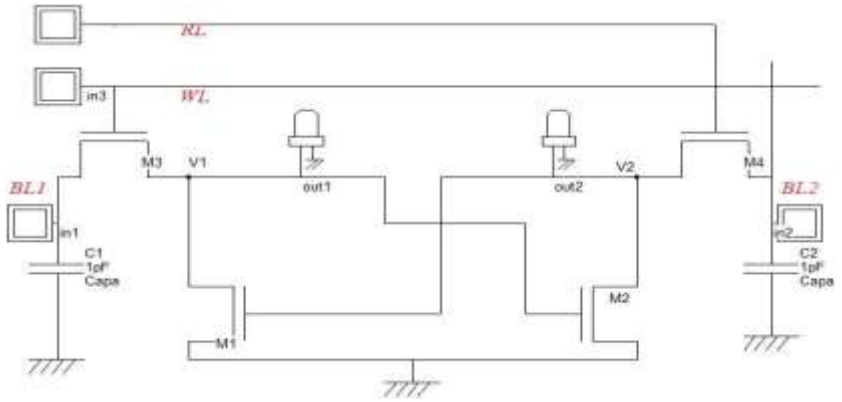

Fig. 2 Four Transistor DRAM Cell

IV. LAYOUT

The layout design of four transistor DRAM is shown in figure 4. This diagram shows a NMOS is implemented by using a n+ diffusion layer and gate is implemented by using a poly-silicon and interconnects are implemented by using metal-1 and metal-2. Waveform of 4T DRAM is shown below. The read and write operation are also shown. The read and write operations are activated when the word line is active in condition. If word line is not active condition circuit behaves as an open circuit.

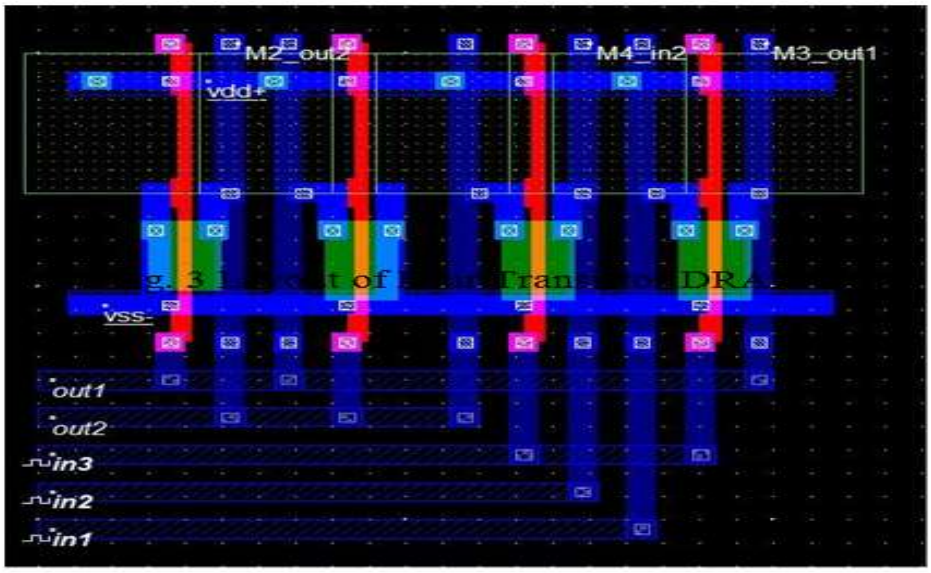

Fig. 3 Layout of Four Transistor DRAM Cell

In this paper, self controllable voltage level technique is used to implement the 4T DRAM and simulation is done by using a DSCH and Microwind 3.5. Here, the DRAM 4x4 was tested with different parameters like changing the voltage and current levels at the inverter and WL inputs.. This approach reduces the number of package pins and has survived through the subsequent memory generation. DRAMS are generally produced in higher volumes. Thus lowering the pin count reduces the cost and size at the expense of performance. The presence of new address word is asserted by raising a number of strobe signals. Raising the row access strobe signal assert the MSB part of the address is present on the address bus and that word decoding process can be initiated.

The LSB part of the address is applied next and the column access strobe signal is asserted. To ensure the correct memory operation, a careful timing of the signal interval is necessary. Basically the signals are used as a clock input to the memory module and are used to synchronize memory event such as decoding memory core access and sensing. DRAM (Dynamic Random Access Memory) must be refreshed periodically. The leakage current can be minimized up to 0.051mA using a 0.25 m 4T DRAM with SVL technique. In this work, we presented a 4x4 DRAM with self controllable voltage level provides with reduction up to 55% of leakage current. The layout of Simulation is done by using a Microwind 3.5.

V. CONCLUSION

4T DRAM with self controllable voltage level technique is implemented by using a DSCH and Microwind 3.5. It is a beneficial for reduction up to 55% of the leakage current To improve the performance and speed of the design. The power supply (V_{DD}) used is 1.2V and designed at 0.25 m CMOS technology. In this implementation, power dissipation is also reduced. The width to length ratio can be improved further.

REFERENCES

[1] Laxmi singh And Ajay Somkuwar,"Used self-controllable Voltage Level technique to reduce leakage current in DRAM 4x4 in VLSI", 978-1-4673-5758-6/13/2013 IEEE

[2] W. K. Luk And R. H. Dennard,"A Novel Dynamic Memory Cell With Internal Voltage Gain", IEEE Journal Of Solid-State Circuits, Vol. 40, No. 4, April 2005

[3] H. J. Yoo, "A Low Voltage High Speed Self Timed CMOS Logic For The Multi-Gigabit Synchronous Dram Application", Ieice Trans. Electron., Vol. E80-C, No. 8, Pp. 11261128, Aug. 1997.

[4] John E. Leiss, Pallab K. Chatterjee, And Thomas C. Holloway, "Dram Design Using The Taper-Isolated Dynamic Ram Cell", IEEE Transac-tions On Electron Devices, Vol. Ed-29, No. 4, April 1982

[5] G. W. Taylor, P. K. Chatterjee, H-S. Fu, And A. F. Tasch, Jr., "A Punch-Through Isolated Ram Cell", IEEE Iedm Tech. Dig., P. 352, 1978

[6] K. M. Cao, W. C. Lee, W. Liu, X. Jin, P. Su, S. K. Fung, J. X. An, B. Yu, C. Hu. "BSIM4 Gate Leakage Model Including Source-Drain Partition" Iedm Meeting 2000, Iedm Technical Digest, Pp. 815-818, December, 2000 and Fujio Masuoka, Fellow, IEEE, "Device Design Guidelines For Fc-Sgt Dram Cells With High Soft-Error Immunity", IEEE Transactions On Electron Devices, Vol. 52, No. 6, June 2005.