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Comparative Analysis of Fine Based 1 Bit Full Adder for Different Logic Styles

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Abstract: *Due to physical limitation on scaling and seriousness of the problem of SCE, leakage current the need of low supply voltage is increasing with the scaling of the transistor.There is need for some alternative to overcome the challenges. Multigate Devices are considered to be the most attractive to succeed the planar MOSFET. Due to its double gate structure it offers innovative circuit design styles. As addition is the most commonly used arithmetic operation in micro-electronic system and is one of the speed limiting elements. There are various full adder designs have been designed owing to its significance in many micro-electronic circuits. The development of adder in terms of efficient parameters such as speed and power consumption should be pursued. This paper concludes the impact of FinFET on design of 1-Bit full adder using different topologies. FinFET based 1-Bit full adder are developed, prototyped, simulated and analyzed using SPICE circuit simulator and comparative analysis is done based on use of lower supply voltage with better performance, low power usage and smaller area. A comprehensive comparison is carried out with 32nm nanoscaled technologies for 3 different topologies using TG, 9T, 14Tand as per the analysis topology using 9T provides better performance interms of average power, supply voltage, size and count of transistor.*

Keywords : *CMOS, Full Adder, FinFET,Multigate Device, Transmission gate (TG)*

I. Introduction

For portable application power consumption is the limiting factor, resulting heat dissipation, which limits feasible packaging and performance of VLSI chips [9]. Thus present technology needs to be scaled. One technique of scaling includes reducing the supply voltage. In synchronous digital integrated circuit, power dissipation can be reduced by reducing the supply voltage. But as supply voltage scales down with technology, many other issues like power supply noise, leakage current, low supply voltage are some of the challenges that are needed to be addressed in design of circuit (MSC) in SoC. The MOSFET logic styles cannot be used below 32nm technology as its performance highly degrades due to short channel effect (SCE). Having physical limitation on scaling of transistor there is a need of some alternative to overcome the challenges. Hence it was necessary to make transition from conventional planar transistor to a new device architecture [4]. International Technology Roadmap for Semiconductors predicts that from 32nm technology node onwards planar bulk device will not be able to meet requirements of technological challenges mentioned above[3]. Thus need of Multigate (MuG) device is considered to be most attractive to succeed the planar MOSFET. MuG MOSFET is one of the drawing device architecture for scaling CMOS to nanometer technology node and beyond on account of their potentially improved channel control using MuG. FinFET technology is one of the leading solutions to satisfy the need for excellent control of the gate over the potential over the body. FinFET is reported a novel double gate (DG) structure that offers advantages like reduced SCE, DIBL, leakage current, power supply voltage, power consumption, threshold voltage, higher speed of operation and current drive and better device scalability. Above features of FinFET are used in wide range of application like low power application. Considering the technological challenges in a way of designing circuit for different application and advantages of MuGFET, researchers are now on the way to combine the features of both aspects and design digital/analog circuit using MuGFET to overcome challenges. Analog circuits designed using FinFET to gain benefits in speed-accuracy-power tradeoff was reported by M.Fulde[4]. The new design have been proven to have significant improvement over conventional single gate CMOS design, thus the survey of different types of FinFET, various logic styles and their architecture are explore. The study of FinFET logic design styles, novel circuit designs and layout considerations were explored[1].

II. Finfet Technology

2.1 Introduction

In parallel transistor there are two transistors with their source and drain terminals tied together. FinFETs were first introduced by researchers at the University of California in 1999 [10]. Most chipmakers are currently developing technologies based on the FinFET. These include IBM, AMD and Motorola. It is

reasonable to assume that the first step away from planar transistors will be into the realm of FinFETs. FinFETs has reduced short channel effects (SCE), higher transconductance and ideal subthreshold voltage.

2.2 FinFET Structure

FinFET are non planar double gate transistor built on Silicon on Insulator (SOI) substrate. The important characteristics of the FinFET is that the conducting channel is enfolding by the thin silicon fin, which creates the gate device. The effective channel length of the device is determined by the thickness of the fin. It is called FinFET because the thin channel region stands vertically similar to the fin of a sandwich between the source and the drain regions. The gate covers around the body from three sides and therefore reduces the short channel effect (SCE).A parallel transistor pair consists of two transistors with their source and drain terminals tied together. The second gate which is added opposite to the traditional gate. Due to problems in aligning the front and back gates, as well as in buildings a low resistance to the back gate, DGFETs are difficult to fabricate. The FinFET has been developed to overcome the problem faced by DGFET. Double gates for FinFETs provide effective control of the short channel effects. It can also be exploited to reduce the number of transistors for implementing logic functions.

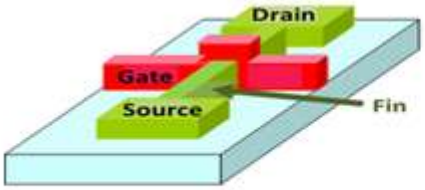

Fig 1: FinFET structure

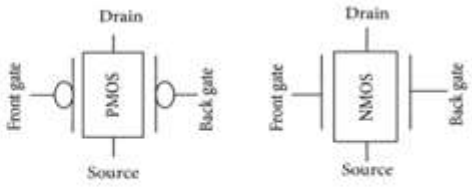

Fig 2: FinFET symbol

2.3 Modes of operation of FinFET

The four modes of FinFET operations are:

2.3.1 Shorted -gate (SG) mode: Both transistor gates are tied together, leading to a three terminal device. It serves as a direct replacement for the conventional bulk CMOS devices.

2.3.2 The independent-gate (IG) mode : Here independent digital signals are used to drive the device gates. The top part of the gate is etched out, giving way to two independent gates can be controlled separately. IG mode FinFETs offer more design options.

2.3.3 The low-power (LP) mode :In this case the back gate is tied to a reverse bias voltage to reduce leakage power.

2.3.4 The hybrid (IG/LP) mode : It employs a combination of LP and IG modes.

III. Overview of 1 Bit Full adder

3.1 Basic Full adder:

Table no. 1 Truth table of Full adder

INPUTS			**OUTPUTS**	
A	**B**	**C**	**SUM**	**COUT**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

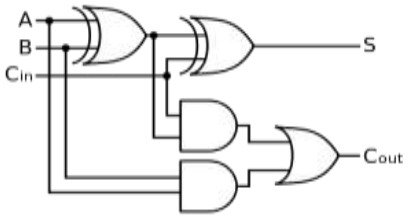

Fig 3: Full Adder

The first two inputs are A and B and the third input is an input carry designated as CIN. From the truth-table, the full adder logic can be implemented. We can see that the output S is an EXOR between the input A and the half-adder SUM output with B and CIN inputs. COUT will only be true if any of the two inputs out of the three are HIGH.

IV. 1Bit full adder circuit using Different Topologies

4.1 FinFET basesd 1-Bit Transmission Gate (TG) Full Adder:

Transmission gates full adder consists of 20 transistors which made up of transmission gates, PMOS and NMOS transistors as illustrated in Fig.5. Transmission gates are used in the design because it has high speed operation and low power dissipation. Apart from less transistor count, less intermediate nodes and lower input loading it has advantage of balanced generation of sum and Cout

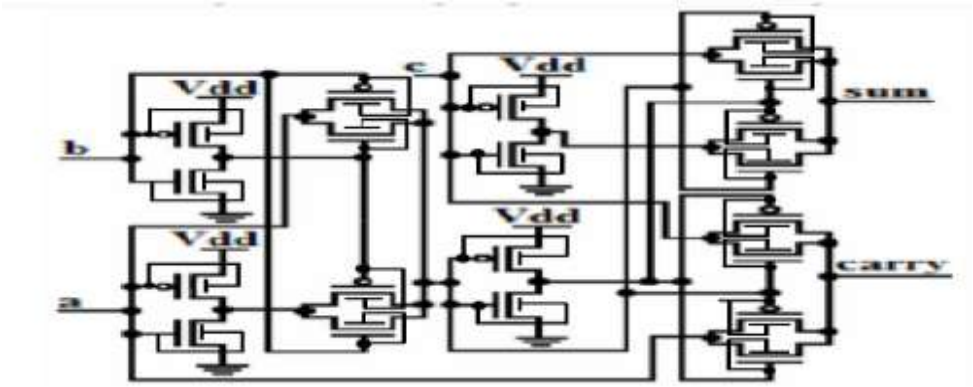

Fig. 4 FinFET Based 1-Bit Full Adder Using TG

4 .2 FinFET based 1 Bit 9A Adder:

Sum is generated by cascading XNOR gate with the new G-XNOR gate while the Cout is generated by simply multiplexing B and Cin They consume less power in high frequencies and have higher speed adder. However with same power consumption it performs faster.

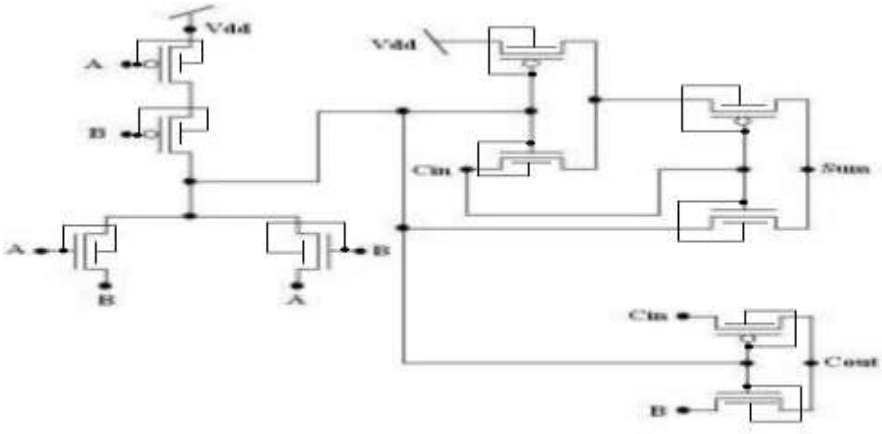

Fig 5: FinFET Based 1-Bit Full Adder Using 9A

4.3 FinFET based 1 Bit 14T Full Adder:

The 14T full adder contains a 4T PTL XOR gate, shown, an inverter and two transmission gates based multiplexer designs for sum and Cout signals.

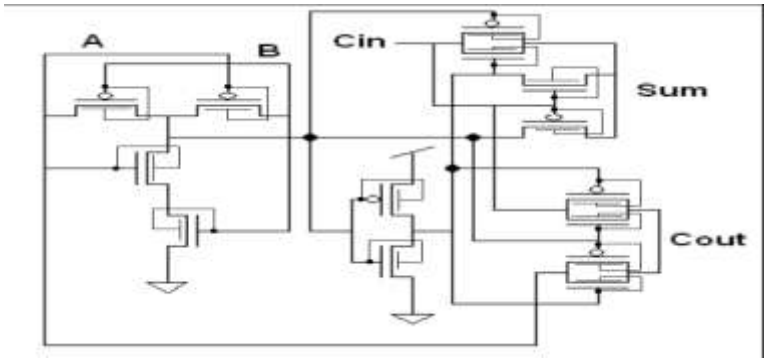

Fig 6: FinFET Based 1-Bit Full Adder Using 14T

V. Performance analysis and Simulation Results

The performance metrics of the full Adder measured are power supply, transistor count, average power, size area. The simulation analysis is done over HSPICE and waveforms are observed on CosmosScope. The simulation analysis is carried out with three inputs (A, B, C) and two outputs (Sum and Carry) of full Adder.

Table No. 2 Comparison of FinFET based 1-bit Full adder using different logic styles

Topology of FinFET based 1 Bit full adder		**TG**	**14T**	**9A**
Transistor count		20	14	9
Technology		32nm	32nm	32nm
Length of Transistor		32nm	32nm	32nm
Width of transistor	**PMOS**	216nm	216nm	216nm
	NMOS	72nm	72nm	72nm
Supply voltage (V)		0.8	0.8	0.8
Average power (uW)		1.5732	1.108	0.108
Tool used		Spice Simulator	Spice Simulator	Spice Simulator

It can be seen that the design of FinFET based 1 Bit Full adder using 9A requires lower average power and number of transistors when compared to remaining two circuits of FinFET based 1 Bit Full adder using TG and 14T while keeping the supply voltage, technology and size of transistor same for all the 3 different topologies

5.1 Simulation results 32 nm FinFET Based Full Adder Using TG:

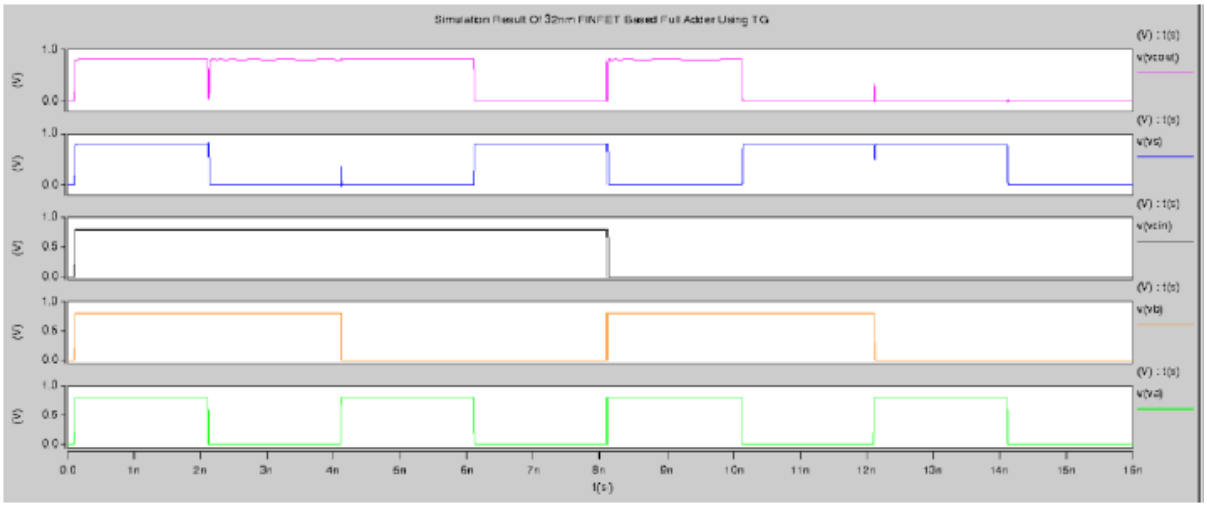

Fig 7: Simulation results of 32nm FinFET based full adder using TG

5.2 Simulation results of 32nm FinFET Based Full Adder Using 14T:

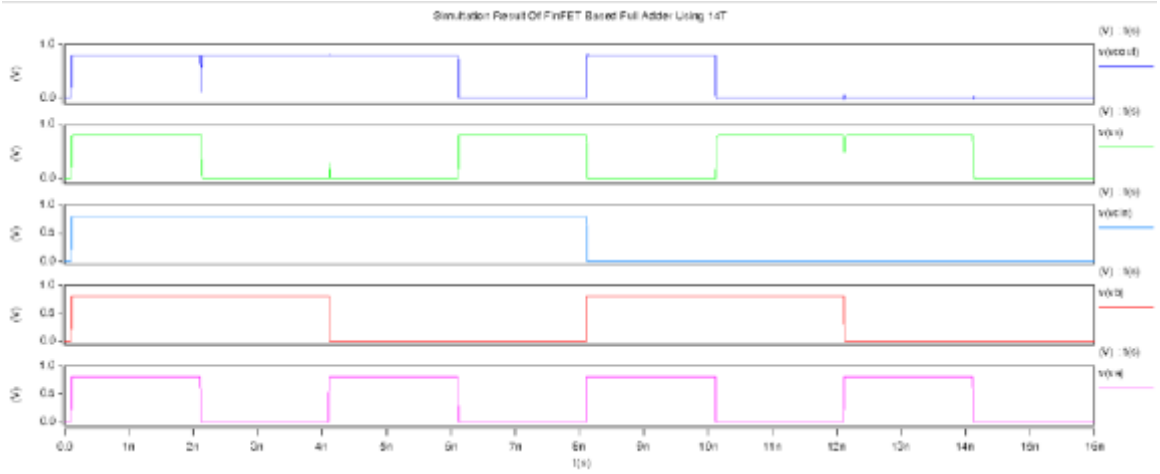

Fig 8: Simulation results of 32nm FinFET based full adder using 14T

5.3 Simulation results of 32nm FinFET Based Full Adder Using 9T:

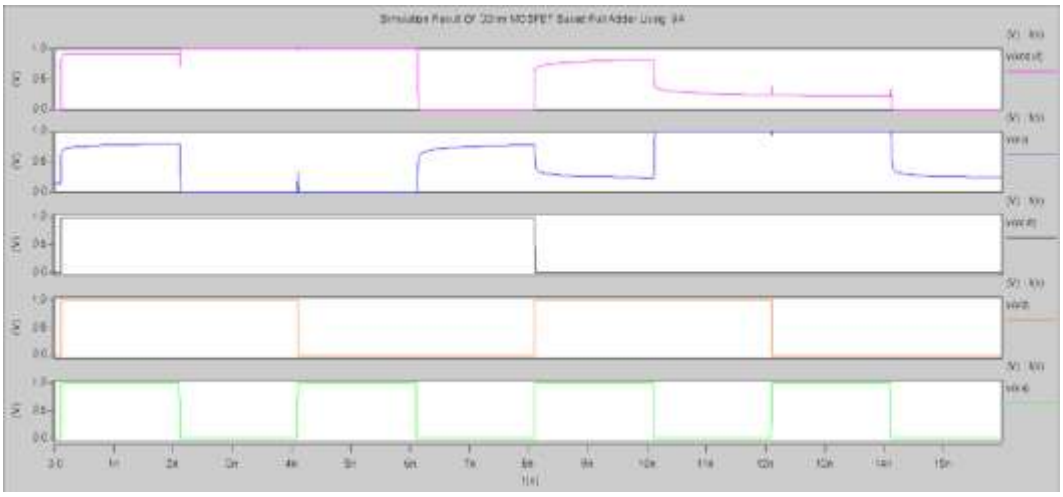

Fig 9 **:** Simulation results of 32nm FinFET based full adder using 9A

VI. Conclusion

The paper presents extensive simulation of implementation and analysis of VLSI circuits using the novel Multigate device (FinFET) is carried so that we could achieve better performance. The paper analyses the performance of Finfet Based 1bit full adder circuit using different topologied. To implement these new designs we replaced conventional MOSFET devices with the new novel DG MOSFET devices i.e. FinFET. It is showed through HSPICE simulations that they operate as expected with better performance parameters. It is found that the full adder cell with FinFET structure requirs lower supply voltage, number of transistors, average power , size as compared to the full adder cell with conventional MOSFET at the same supply voltage.Therefore, MOSFETs in full adder cell can be effectively replaced by the FinFET structure to optimize overall average power which will make the design more robust against process variation.

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