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Network-on-chip Architecture Latency Analysis of Odd-Even Routing Algorithm for 2D mesh topology

Prof. Anuradha A.Dakhane[1]
[1]*Assistant ProfessorRajiv Gandhi College of engineering,research and technology,Chandrapur*

Abstract: Network on chip is a scalable and flexible communication architecture for the design of core based System-on-Chip. Communication performance of a NOC heavily depends on routing algorithm.. Odd-Even (OE) routing algorithm is distributed adaptive routing algorithm with deadlock-free ability The purpose of NOC to solve communication and clock problem from architecture. Noc architecture includes number of routers to route the packets from sender to receiver. When network is in congestion, packet transmission will produce more time delay to get balance between time delay and throughput the appropriate routing algorithm is used. In this paper we used Odd Even routing algorithm for 2D mesh topology under bursty communication traffic and NIRGAM simulator for analysis of Latency and throughput .Packet size is vary along with network sizes 3×3,4×4,5×5,6×6,7×7,8×8,9×9.Consider all tiles as source, all tiles as destination. It is found that packet size along with network size increases then average latency/packet increases and average throughput (in Gbps) also increases but average latency/flit decreases.

***Keywords*:** 2D Mesh topology, ODD-EVEN routing algorithm, Network on Chip (NoC), NIRGAM simulator.

I. Introduction

Network on chip is a new paradigm for system on chip(Soc) design. Increasing integration produces a situation where bus structure which is commonly used in Soc becomes blocked and increased capacitances poses physical problems.In NOC architecture traditional bus structure is replaced with network which is lot similar to the internet .Network consists of wires and routers ,procesors,memories and IP- blocks(Intellectual property) are connected to routers.Information over the NoC is communicated in the form of packets. "Routes are packets,not wires"[2].The most important feature of NOC are network topology and routing algorithm.A routing algorithm plays important role on network operation and affects NOC network communication.

There are different routing algorithm such as XY, OE ,Source routing algorithms. Here OE routing algorithm[1] is used which gives limits on the possible shift position of packets to avoid the happening of deadlock. OE routing algorithm is a sort of distributed adaptive and shortest path routing algorithm based on odd even turn model[3]. It exerts some restrictions, for avoiding and preventing from deadlock appearance. Odd-even turn model facilitates deadlock-free routing in two-dimensional (2D) meshes with no virtual channels. Topology defines how nodes are placed and connected affecting bandwidth and latency of network.There are different types of topologies such as mesh, torus, folded torus, star, octagon, tree, etc. Among this topology, 2D Mesh topology was proposed to reduce the latency.figure 1:shows 4×4 2-Dimensional Mesh NoC.

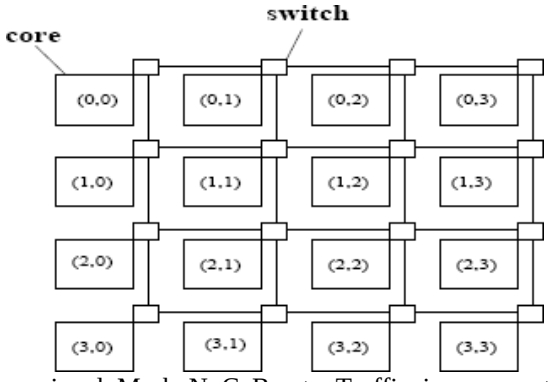

Figure 1: 4×4 2-Dimensional Mesh NoC Bursty Traffic is represented by alternating on and off periods. During ON period packets are generated in fixed intervals. During OFF period no packets are generated. Bursty Traffic is more better than constant bit rate(CBR) traffic.

The performance parameters are latency and throughput. Latency is defined as time taken to deliver a packet from source to destination. Throughput is defined as a fraction of packets delivered from sources to destinations in a given amount of time.

II. Related Work

Pan Hao,Hong QiI,Du Jiaqin,Pan Pan .In this paper author purposed NOC is to solve the choke point in communication and the clock problem from architecture. Each in NOC includes some routers, and it takes a few clock periods by passing a router. When the network is in congestion, the package transmission will produce much more time delay. So adopting a appropriate routing algorithm to get the balance between the time delay and throughput rate becomes the key problem. In this paper, researcher done some research on XY and OE algorithms based on the 4x4 mesh topology by using NIRGAM emulator. The result shows that the ratio of throughput rate and package time delay is 2.5358 in OE routing algorithm, which is larger than 2. 1126 in XY routing algorithm, and it proves that the OE routing algorithm is better to Mesh topology than XY routing algorithm[4].

Wang Zhang, Ligang Hou, Jinhui Wang, Shuqin Geng, Wuchen Wu, In this paper, researcher demonstrated the two routing algorithms in details at first. XY routing algorithm and OE routing algorithm are then simulated and compared based on a 3X3 mesh topology NoC with NIRGAM simulator.The simulation results show that OE routing algorithm, P= Average Throughput of Network/ Average Latency per packet of Network whose P parameter equals to 1.09, increases P parameter greatly as compared to XY routing algorithm, whose P parameter equals to 0.86, in a 2-dimension 3X3 mesh topology NoC, with Constant Bit Rate (CBR) traffic condition of each tail. If value of parameter P is larger, the performance will be better. P(XY)= 0.86 and P(OE)=1.09. Thus, OE routing algorithm better than XY routing algorithm[5].

Naveen Choudhary ,in this paper author analyzed the performance of standard 2D mesh NOC is for bursty communication traffic for various traffic or topology mapping patterns such as butterfly, transpose etc over a NOC simulation framework. The routing for the NoC is assumed to be XY and OE. It is observed that the communication performance of the 2D-mesh based NoC for bursty traffic is deeply affected by the varying traffic permutation for the used routing function Which basically helps us conclude that if appropriate traffic permutation are chosen for the bursty traffic in accordance to the routing function may lead to major gain in communication performance of the NoC. [6]

Ge-Ming Chiu**,**The objective of this paper to present the odd-even turn model for designing partially adaptive wormhole routing algorithms without adding virtual channels.The model restricts the locations where some turns can be taken so that deadlock is avoided. Simulation carried for xy algorithm, west-first algorithm, negative-first algorithm, even odd algorithm. Performance of the algorithms measured for avg. communication Latency and Throughput[3].

Marjan Morvarid, Reza Berangi, Mahmood, In this paper,author present a multipath routing scheme which is called DPOE (Dual Path Odd-Even). Multipath routing allows the establishment of multiple paths between a single source and single destination node. It is typically proposed in order to provide load balancing.In this, using allowed defined rotations in Odd-Even adaptive algorithm.packets are sent through two different paths and by employing a new selection policy, which is specifically for multi-path methods,they provided load balancing and improve efficiency of the network. By comparing simulation results, it will be observed that this method, under different traffic patterns, will significantly perform better than other methods Performance measured in terms of Average Packet delay(cycles) and avg Throughput(flit/cycle) over Packet injection rate(packets/cycle)[7].

Wang Zhang**,**A Network on Chip Architecture and Performance Evaluation,in this paper Networks-on-chip (NoCs) have emerged as an alternative to ad- hoc wiring or bus-based global interconnection in Systems-on-Chip (SoCs). The architecture of network significantly determines system performance. This paper proposes a network on chip architecture with 2- demention mesh topology, odd-even routing algorithm, wormhole switching technique and only input buffers. The size of packet is 20 bytes and that of flit is 5 bytes. The performance of proposed architecture is evaluated based on metrics of latency and throughput per channel under Constant Bit Rate (CBR) and Bursty traffic. For the proposed architecture, the evaluation results reveal that the average latency of whole network channels is 1.97 cycles under CBR traffic and 1.92 cycles under Bursty traffic. The average throughput of whole network channels is 8.8555 Gbps under CBR traffic and 8.8212 Gbps under Bursty traffic[19]

Singh, J.K.,In this paper author compares result of two routing algorithms and they find,a better routing algorithm can enhance the performance of NoC. XY routing algorithm is a distributed deterministic algorithm. Odd-Even (OE) routing algorithm is distributed adaptive routing algorithm with deadlock-free ability. Every NoC should satisfy some performance requirements like low latency, high throughput and low network power. Here we demonstrated the impact of traffic load variations on average latency, average throughput and total network power for two routing algorithms XY and OE on a 3×3 2-dimensional mesh topology. The simulations have been performed on NIRGAM NoC simulator version 2.1 for constant bit rate (CBR) traffic condition. The simulation results contains overall average latency (clock cycles per packet), average throughput (in Gbps) and total network power (in mW). Performance metrics (P) is calculated for both routing algorithms and compared.

For XY Routing (50% Load) P = (8.198/13.5859) = 0.6034,For OE Routing (50% Load) P = (9.2098/12.3141) = 0.7479,

ThePerformance metrics shows that OE routing algorithm is better routing algorithm than XY routing algorithm in Network on Chip design. [20].

III. Problem Defination

We observed that in related work on design of NOC architecture maximum paper made comparison of simulation performance parameters between XY and Odd-Even routing algorithm of a 2-Dimension 4X4 Mesh topology network-on-Chip is obtained with constant Bit rate (CBR) traffic condition of each tail. From related work it was observed that researchers did not work using bursty communication traffic.

So In this paper we have proposed **bursty traffic** for performance and simulation of **Odd-Even Routing algorithm** for **2D mesh topology** of Network-on-chip architecture. Performance is measured in terms of **Latency** and **Throughput.**

IV. Architecture OF 2D 3×3 Mesh Topology NOC

The routing Algorithm is simulated based on a 2- Dimension 3X3 mesh topology NoC (Fig. 2). In the Fig. 1, each circle represents a tile in the network. Each tile consists of an IP core connected to a router by a bidirectional core channel (C). A tile is connected to neighbor tiles by four bidirectional channels (N, E, S and W). Each tile is identified by a unique integer ID.Also, each tile can be identified by a pair x-coordinate and y-coordinate.2-Dimesion 3X3 mesh topology NoC is designed using wormhole switching mechanism, in which packets are divided into flits. A packet consists of 3 types of flits, which are head flit, data flit and tail flit. OE routing algorithm is based on these characteristics.

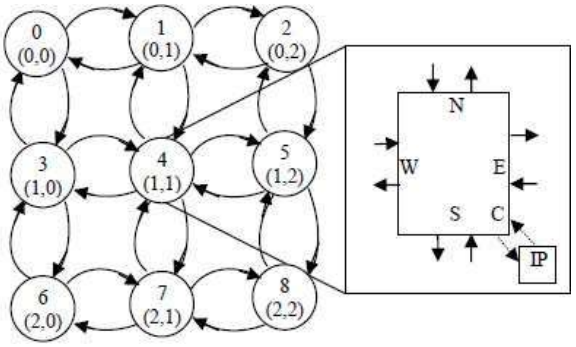

Figure. 2 Architecture of 2 dimensional 3×3 Mesh topology based NoC.

V. Odd-Even Routing Algorithm

OE routing algorithm is applied to NOC of Mesh structure. By making agreements to the position of possible occurrence turns, it can avoid the occurrence of deadlocks without using virtual channels. Explaining some definitions are necessary in order to represent this algorithm. In a two-dimension mesh with dimensions X×Y each node is identified by its coordinate (x, y). Take 2D-Mesh for example, if the X-dimensional coordinate of a node is odd , it is called the odd column. If the X-dimensional coordinate of a node is even, it is called the even column. Using S, W, N, E to represent the south west , north and east directions. The algorithm contains eight kinds of turns, respectively WS,WN, NS, NE, ES, EN, SE, SW. For example,WS identifies the turn from west to south. In the odd-even turn model, such turns are prohibited:(l)In even column nodes, EN, ES are prohibited;(2) in odd column nodes, NW, SW are prohibited; (3) 180°tum is prohibited. According to OE routing algorithm the following theorems are necessary to avoid deadlocks. Theorem1: If a node is present on an even column the packets can't take EN turns shown in Figure. 3.1 and if a node is present on an odd column the packets can't take NW turns shown in Figure 3.2 . Theorem 2: If a node is present on an even column the packets can't take ES turns• shown in Figure 3.3 and if a node is present on an odd column the packets can't take SW turns shown in Figure 3.4

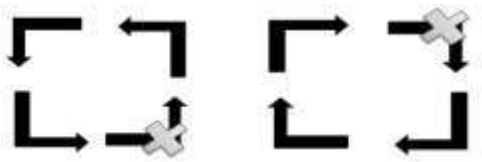

Figure 3.1 Allowed turns for even column in OE routing

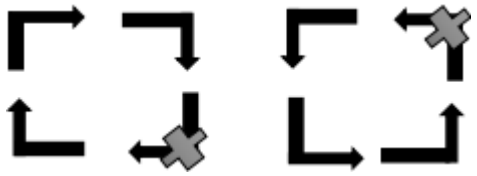

Figure 3.2 Allowed turns for odd column in OE routing

The following test is minimal OE routing algorithm in which avail_dimension_set contains dimensions that are available for forwarding the packet:

```
/* OE routing algorithm */
/*Source router: (Sx,Sy);destination router: (Dx,Dy); current router: (Cx,Cy).*/
begin
avail_dimension_set<-empty; Ex<-Dx-Cx;
Ey<-Dy-Cy;
if (Ex=0 && Ey=0) //current router is destination return C;
if (Ex=0){ //current router in same column as destination
if (Ey<0)
add S to avail_dimension_set; else
add N to avail_dimension_set;
}
else{
if (Ex>0){ //eastbound messages
if (Ey=0){ //current in same row as destination add E to avail_dimension_set;
}
else{
if(Cx % 2 != 0 or Cx=Sx) //N/S turn allowed only in odd column.
if(Ey < 0)
add S to avail_dimension_set; else
add N to avail_dimension_set; if(Dx% 2 != 0 or Ex != 1)
{           //allow to go E only if destination is odd column add E to avail_dimension_set;
//because N/S turn not allowed in even column
}
}
}
else { // westbound messages add W to avail_dimension_set;
if(Cx%2=0) //allow to go N/S only in even column, because N->W and S->W//not allowed in odd column
if(Ey<0)
add S to avail_dimension_set; else
add N to avail_dimension_set;
}
}
//Select a dimension from avail_dimension_set to forward the packet.
End
```

OE routing algorithm is a kind of adaptive routing algorithm. For a pair of source and destination, it can provide a group of routing paths and it can prevent from dead lock appearance.

VI. Simulation Result And Analysis

The simulation performed on NIRGAM simulator. NIRGAM is discrete event,cycle accurate simulator targeted at network on chip(Noc) research. NIRGAM works on LINUX operating system. Simulator for interconnect Routing and application modeling version 2.1. NIRGAM is an extensible and modular system C based simulator[8].

All tiles are used as a source and destination. All tiles send packets and all tiles received packets by using bursty traffic generator. The network size used is 3×3,4×4,5×5,6×6,7×7,8×8,9×9. The packet size is vary from 8 bytes to 128 bytes for network size 3×3 to 9×9 with a random destination mode. The load percentage is 100% which means that 100% of bandwidth is used. The simulation runs on 1000 clock cycles and clock frequency is 1GHz. The synthetic traffic generators generate traffic in 300 clock cycles with warm up period of 5 clock cycles. The flit interval between successive flits is 2 clock cycles. Average burst length (number of packets generated during ON time) is 4 and average off time is interval between two bursts is 15 clock cycles. Simulation performance of

routing algorithm is measured on a per-channel basis. We have simulated program for 10 times for each parameter and then taken average of 10 runs to get value of average latency (in clock cycles) per flit, average latency (in clock cycles) per packet and average throughput (in Gbps) for each channel.The performance metrics are average latency (in clock cycles) per flit, average latency (in clock cycles) per packet and average throughput (in Gbps) for each channel.

Fig. 3 shows the utilization of simulator for the proposed work elaborating the inputs given to the simulator and outputs taken from the simulator. There are three bets measures of Performance of routing algorithms namely, average latency per flit (in clock cycles), average latency per packet (in clock cycles) & average throughput(in Gbps) on a per channel basis is measured.

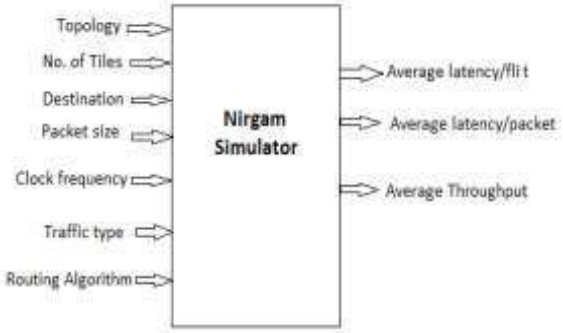

Figure 4: Inputs and Outputs to NIRGAM NoC Simulator

Table 1: Simulation Results For Packet Size Verses Average Latency Per Flit(In Clock Cycles) For Different Network Size

Pack et size(i n bytes)	Average latency per flit (in clock cycles)						
	3×3	4×4	5×5	6×6	7×7	8×8	9×9
8	3.70662	4.15124	4.63843	5.23427	5.79954	6.34145	6.5843
16	4.09953	3.71233	3.54479	2.39167	3.94185	4.12016	4.25394
32	3.14565	2.75947	2.29988	2.39167	2.4278	2.48057	2.48156
64	1.91961	1.64324	1.44908	1.37472	1.34984	1.40414	1.39498
128	1.32706	1.00571	0.907036	1.02046	0.95275	0.99598	1.00431

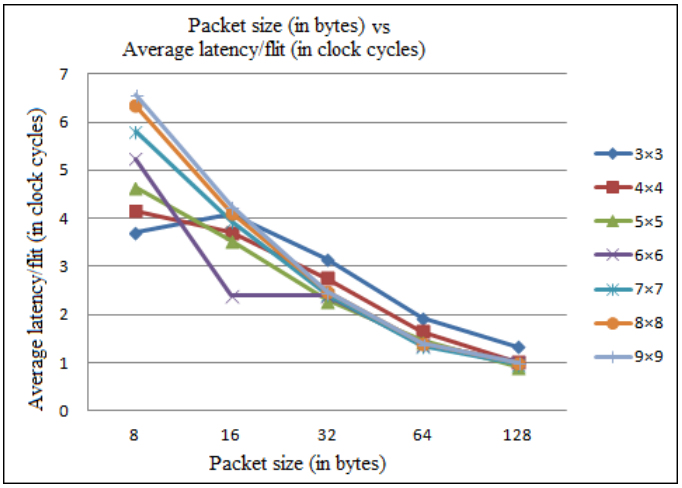

Figure 5: Graph of Packet size(in bytes) vs Average latency per flit (in clock cycles) for different Network size

Table 2: Simulation Results For Packet Size Verses Average Latency Per Packet (In Clock Cycles) For Different Network Size

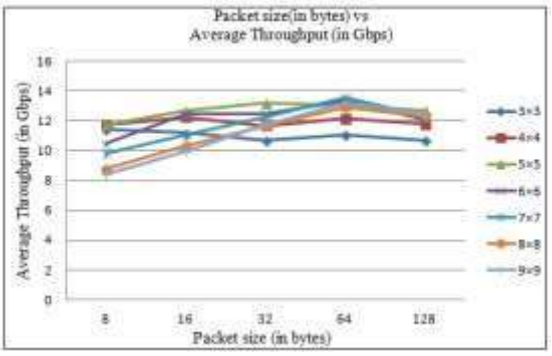

Figure 7: Graph of Packet size(in bytes) vs Average Throughput(in Gbps) for different Network size

Packet size(in bytes)	Average latency per packet (in clock cycles)						
	3×3	4×4	5×5	6×6	7×7	8×8	9×9
8	11.1214	12.4537	13.9153	15.7048	17.39823	19.0237	19.7041
16	20.4977	18.562	17.7236	21.51246	19.4546	20.597	21.6309
32	28.31088	24.8353	20.6989	21.525	21.347	22.1075	22.4069
64	32.6333	27.93508	23.57713	23.37027	22.9472	24.9365	23.8291
128	43.7931	33.18823	29.93215	34.06023	31.9941	34.1879	35.1186

Table 1 depicts simulation result for different Network size showing impact on varying Packet size on Average latency per flit(in clock cycles) for figure 5. shows the graphical representation for simulation data of Table 1 shows Packet size verses Average latency per flit(in clock cycles) for different Network size. Table 2 depicts simulation result for different Network size showing impact on varying Packet size on Average latency per packet (in clock cycles) for figure 6. shows the graphical representation for simulation data of Table 2 shows Packet size verses Average latency per packet (in clock cycles) for different Network size. Table 3 depicts simulation result for different Network size showing impact on varying Packet size

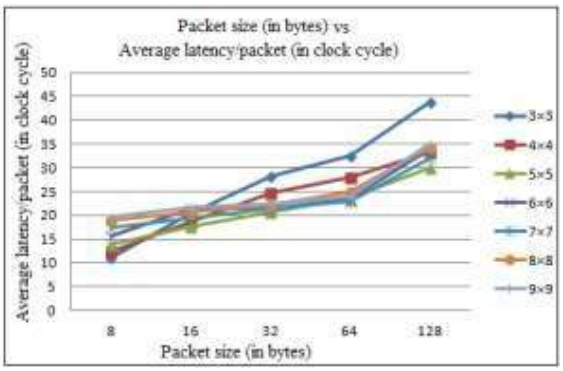

Figure 6: Graph of Packet size(in bytes) vs Average latency perpacket (in clock cycles) for different Network size

Table 3: Simulation Results For Packet Size Verses Average Throughput (In Gbps) For Different Network Size

Packet size (in bytes)	Average Throughput (in Gbps)						
	3×3	4×4	5×5	6×6	7×7	8×8	9×9
8	11.4088	11.74079	11.74201	10.44602	9.8414	8.75673	8.42466
16	11.1745	12.2673	12.65915	12.48111	11.0439	10.29997	9.95346
32	10.72633	11.68524	13.1677	12.4811	12.2173	11.67736	11.7363
64	11.06051	12.18655	13.08254	13.35119	13.53876	12.9086	13.2286
128	10.68405	11.78463	12.70637	12.09588	12.34657	12.32035	12.4347

on Average Throughput (in Gbps) for figure 4. shows the graphical representation for simulation data of Table 1 shows Packet size verses Average Throughput (in Gbps) for different Network size.

From figure 5 ,we can conclude that, If packet size increases along with network size then average latency per flit(in clock cycles) decreases. from figure 5,we can conclude that average latency per packet (in clock cycles)increases and from figure 7,we can conclude that, if packet size (in bytes) increases along with network size then average throughput (in Gbps) per channel has maximum value for packet size 64 bytes in 6×6 to 9×9 network size. In 3×3 network size throughput value is maximum for packet size 8 bytes. In 4×4 network size throughput value is maximum for packet size 16 bytes. In 5×5 network size throughput value is maximum for packet size 32 bytes.

VII. Conclusion

In this paper, we have used OE routing algorithm on regular 2D mesh topology of NoC architecture. NIRGAM simulator is used for analyze the performance of 3x3 to 9×9 network size. Parameters are to be considered, all tiles as source and all tiles as destination, that means all tiles send packets and all tiles receive packets by using bursty traffic generator.

The packet sizes vary from 8 bytes to 128 bytes with 100% load for 3×3 to 9×9 network size and all other parameters are constant. The performance parameters are latency and Throughput. Simulation performance of routing algorithm is measured on a per-channel basis. It has been observed that, If packet size increases along with network size then average latency per flit(in clock cycles) decreases and average latency per packet increases. If packet size (in bytes) increases along with network size then average throughput (in Gbps) per channel has maximum value for packet size 64 bytes in 7×7.

VIII. Future Scope

In NoC architecture mesh topology is dominant for physical structure and implementation. Therefore researcher used this topology. We had also used mesh topology to analyzed the performance and simulation of odd-even routing algorithm of NoC architecture under bursty traffic condition. Futurescope is that other topologies and traffic condition available for analysis the performance and simulation of odd- even routing algorithm of NoC architecture to reduce latency and to improve Throughput.

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