IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
PP 01-03

Implementation And Analysis Of Partial Reconfiguration Based Xilinx Ise Design Of Processor Peripherals

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ABSTRACT: *In this paper authors designed an OPB to DCRBridge which can be dynamically reconfigurable using ICAP(Internal Configuration Access Port).The processor system is created using Xilinx platform studio and PlanAhead software which is used to design the floorplan.The design deals with construction of OPB2DCR Bridgefor which Virtex-4 ML401 Evaluation Board is used to verify the design in hardware using Compact Flash Memory card to initially configure the Field Programmable Gate Array (FPGA) and then partial reconfiguration using ICAP under software control. Here authors use specific regions of the FPGA to reconfigure with new functionality at run time while rest areas in the FPGA remain static during that specific period of time. Here the user interacts with Partial Reconfigurable Regions (PRRs) and reconfigurable modules (RMs) using HyperTerminal under application control.*
Keywords*:Field Programmable Gate Array,Partial Reconfigurable Region,Reconfigurable Module, Internal Configuration Access Port*

I. Introduction

In these days researchers choose between a number of FPGA devices for example Spartan-3,Viterx-4 ,Vietex-5 for Xilinx.These devices consists of millions of gates and operating frequencies approaching to 500MHz.Virtex-4 is a programmable device.These can be fabricated using 90nm technology which accelerates the operation and also decreases power consumption. The ML401 (XC4VLX25-FF68-10) is intended to Virtex-4 technology. The Virtex-4 FPGAs include improved advanced inputs/outputs, clock technology, DSP blocks, embedded MAC, embedded processor, Smart RAM blocks and more. Modular design flow is used in partial reconfiguration implementation work. The requirement which are added follows the range constraints for reconfigurable modules which is applied.The bus macros are required for set up communication between reconfigurable modules. The reconfigurable module and static module have to be combined and then assembled.The full and partial bit stream created for the device.The Xilinx PlanAheadsoftware is used to integrate the floor plan, Macro placement, module implementation and assembly into a single graphical user interface. In this paper the design shows the hierarchical of the top level design which consists of two PRRsi.e left and right PRRs[3][4][5].

II. Flow Of System Architeure In Processor Design

The intellectual property is utilized in the interfacing the modules to abstract On-Chip Peripheral Bus i.e OPB. In this implementation processor system consists of OPB to DCR i.e Device Control Register. OPB includes arbiter with dynamic or fixed priorities and bus parking and DCR supports a master and multi slaves, daisy chain connection for the DCR data bus[1][2][14][15]. The bridge provides a memory mapped interface. The MicroBlazei.e MB is a softcore microprocessor as shown in figure 1.the MicroBlaze is a virtual microprocessor which is designed by combining block of code called cores inside a FPGA. The EDK connects the processor system. Digital Clock Manager i.e DCM is also used in Xilinx ISE to design the top module.

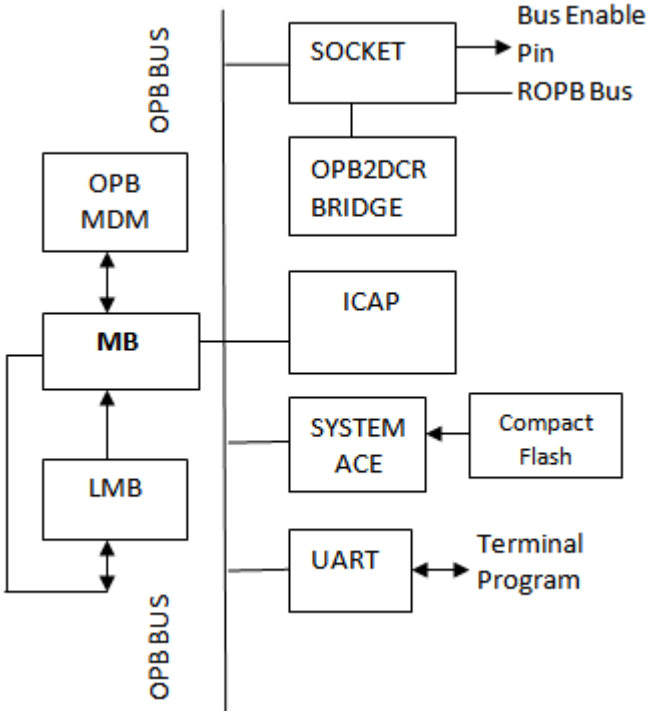

Figure1: Top Module of Processor Design

III. Experiment And Result

In the experiment when a hardware system was chosen in the Xilinx EDK[13][14][15] and after that hardware was synthesized. The netlist was loaded into the PlanAhead where the partial reconfigurable module was defined and placed in the specified pblock. For communication between the reconfigurable module and static logic,BusMacro has been placed. Then after successful passage of the Design Rule Check[5][6][7], the floor plan has to be exported to a folder and PlanAhead partial reconfigurable flow is executed.

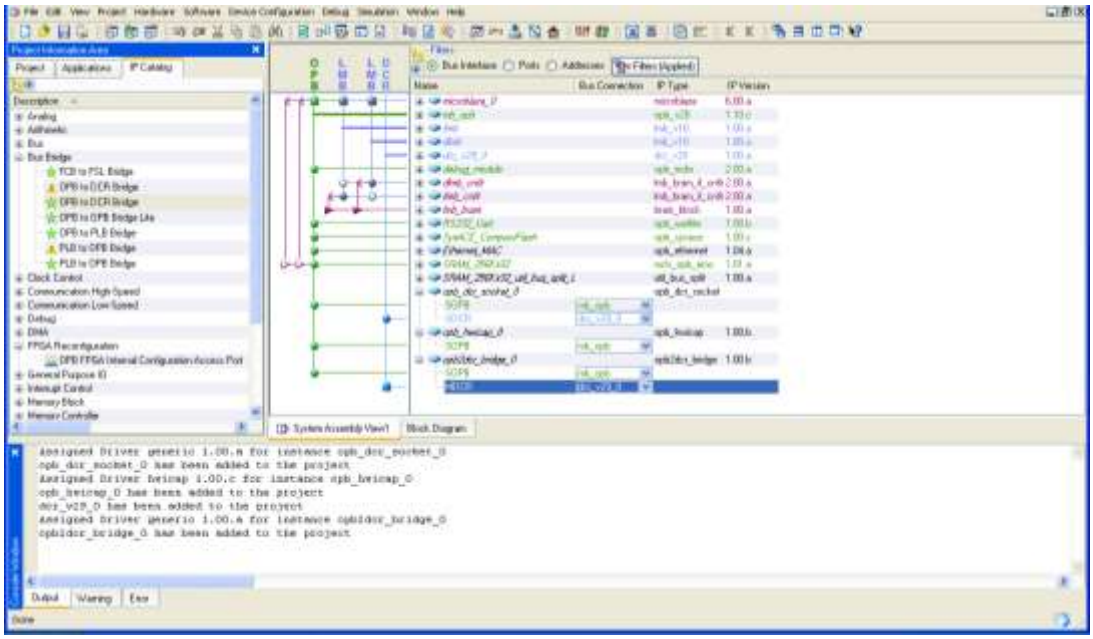

Figure 2: OPB to DCR Bridge using Xilinx Platform Studio

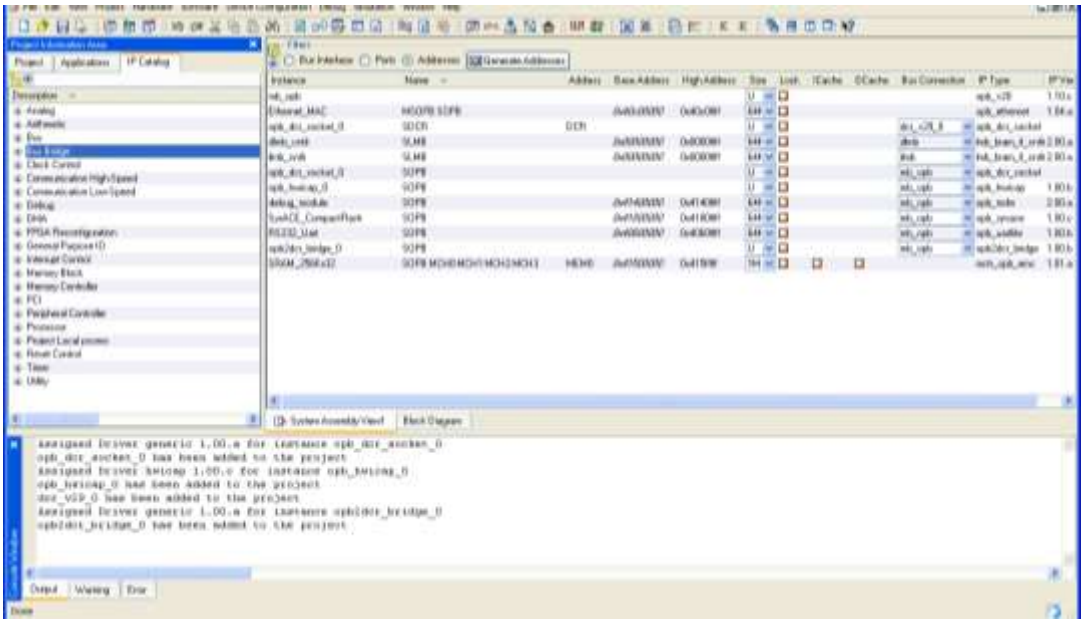

Figure 3: Bus Bridge using Xilinx Platform Studio

IV. Conclusion

An On-chip Peripheral bus to device control Register Bridge is designed using Xilinx Platform Studio which acts a main in designing the peripheral processor by Xilinx Platform Studio.Bus Macros are also used to set up a communication between the modules which is shown in figure 3 and also connectivity is shown in figure 4.EDK allows for the development and will be required for development related to self-reconfiguration.EDK is used to synthesize all peripherals required for the operation.

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