IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
PP 65-74

Design Alternatives For A 4-Bit Universal Shift Register Using Clock Pulse Sense Latch.

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Abstract: *This paper proposed the design of 4-bit universal shift register using a low power area reduced speed improved clock pulse generator and clock sense pulse latch. The proposed 4-bit universal shift register consists of two section of operation one section included pulse latch and another section for the control operation like right shift, left shift and parallel loading. These operations of the universal shift register executed by 4*1 MUX. All the MUX design using PTL logic and the clock pulse generator is designed using inverted inverter logic and pass transistor based AND gate circuit. The proposed 4-bit universal shift register increased the speed with low power consumption. The 4-bit universal shift register is designed and tested by using cadence virtuoso simulation tool in 180nm technology at a supply voltage of 1.8v for pulse latch and 2.5v for 4*1 MUX.*

Keywords: *low power, clock pulse generator, 180nm, cadence virtuoso, pass transistor logic, area-efficiency, MUX design, shift register.*

I. Introduction

Due to the increment of portable system and rapide devllopment in electronic sectore a low power and less area and speed improved device is necessaryto archives this gole .a low power speedimproved 4-bit univarsal shift registerhas beeen designed for different electronics application like data processing ,data counter ,computer memory element[1].the latches and flipflop are the basic storage element of all digitl electronics circuits.but for operating a latch a clock pulse generator is required.Due to the the clock pulse generatorproduced squezied clock pulse ,the latcches are act as edge triggerd flipflop[1].

The advantages of the clock pulse latch over flipflop is it conssumes less area and low power and due to it operate with a shorter lengteh clock pulse it provide faster operation ratherthan flip-flop.so the univarsal-shift register are designed for load or retrive the data in any mode .like either (serial and parallel) by shifting it either towords right or towords left.a univasal shift register can conduct 3-mode of operation left shift,right shift and parallel load of operation with the help of two select line S1,S0,which is connected to the control module the control modul contain 4*1 MUX.

In order to operate the univalsal shift register in asppecific mode ,it must first select the mode.to accomplish mode selection the univalsal shift register uses a setof two selector switches S1,S0eatch permutation of the switches corresponds to a loading /input mode[2].

TABLE I

S0	S1	Function
0	0	Parallel load
0	1	Left Shift
1	0	Right Shift
1	1	No Change

II. Basic Concept

Clock Pulse Generator

Clock Pulse Generator (CPG) is the main consideration for operating a clock sense pulse latch .CPG is basically designed using clock pulse circuits which are connected through a metal path back to back serially, like first clock pulse generator output feed to next input of the clock pulse circuit. The CPG generate clock pulse having shorter in length due to this property of the CPG more data can shifted through corresponding clock sense pulse latch rather than other conventional model.so the produced timing signal of the CPG reduced the delay period between to back to back clock pulses. The CPG is use as a trigger circuit for different applications like shift register, ring counter, frequency divider and many synchronizing circuit operations.

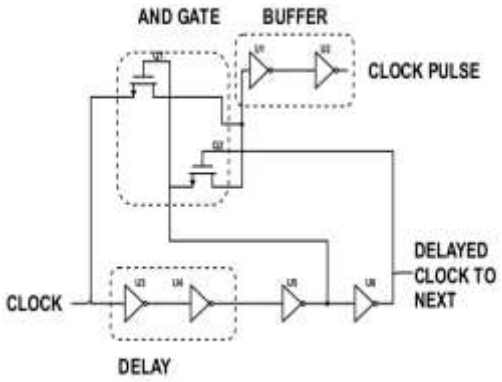

Fig. 1(a) Schematic daigram of single bit clock pulse generator [5]

Clock Sense *Pulse Latches*

Latches are generally used to store base-2 number data in an asynchronous sequential system. Clock pulse generator is the circuit which is used to build shift register and other electronic circuit through a clock sense pulse latch. When the time sensitivity determine by the width of the clock waveform then only the pulse latch can store data. For operating a pulse latch a clock pulse latch is required .the clock pulse is said to be set when the rising edge of the clock pulse towards the pulse latch and is to be in hold state during the falling edge is towards the pulse latch. A clock tree is requires for operating a higher bit and to triggering the latch.

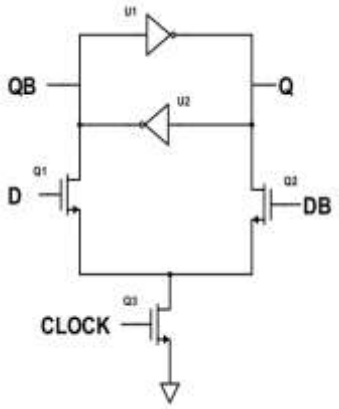

Fig.1(b) Schematic diagram of the SSASPL latch [1]

Universal Shift Register can be arranged to load and/or redeem the data in any mode (either serial or parallel) by shifting it either towards right or towards left. A universal shift register is an integrated logic circuit that can carry data in three different modes. Like a parallel register it can load and communicate data in parallel. Like shift registers it can load and carry data in serial fashions, through left shifts or right shifts. Moreover, the universal shift register can merge the potential of both parallel and shift registers to achieve tasks that neither basic type of register can perform on its own. For instance, on a particular job a universal register can loaddata in series (e.g. through a sequence of left shifts) and then transmit/output data in parallel. [3]

Universal shift registers, like other types of registers, are used in computers as memory elements. Although other types of memory devices are used for the logical storage of very large amount of data, from a digital system point of view when we say computer memory we understand registers. In reality, all the operations in a digital system are execute on registers such operations incorporate multiplication, division, and data transfer.

For the universal shift register to work in a particular mode, it must first select the mode. To realize mode selection the universal register uses a set of two selector switches, S1 and S0. As shown in Table 1, each permutation of the switches agree to a loading/input mode.

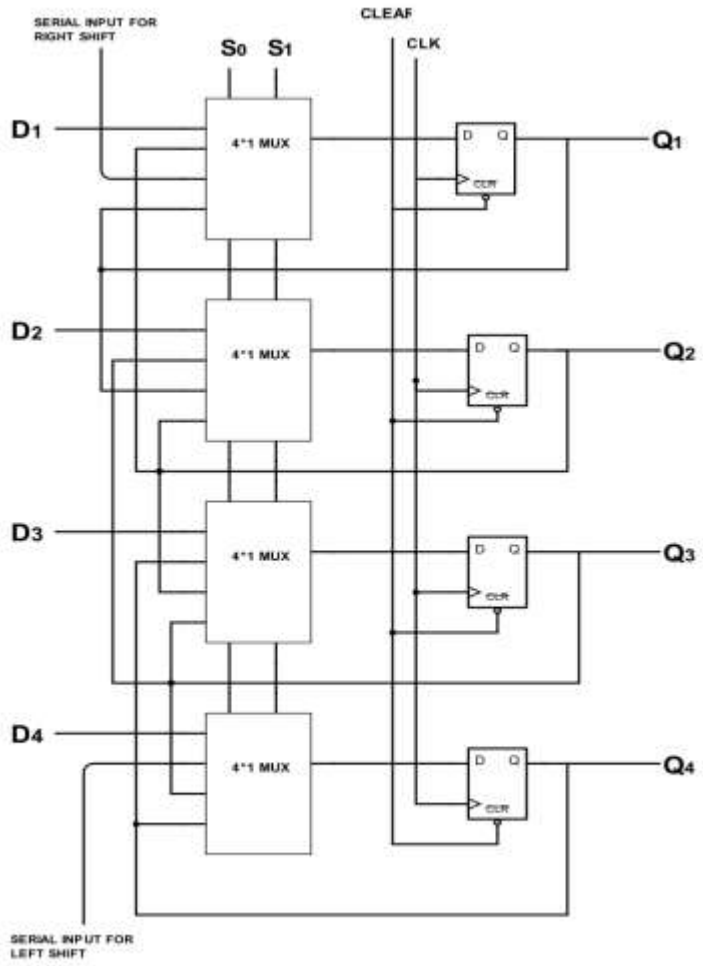

Fig.1(c) Architecture of universal shift registers[2]

III. Proposed System

A universal shift register can conduct 3-mode of operation like left shift, right shift, parallel loading with the help of two select line S1and S0 which is connected through control module .the control module contains 4*1 MUX.For constructing a 4-bit universal shift register required component are single clock pulse generator (SCPG), static sense amp shared pulse latch(SSASPL) and 4*1 MUX.

2*1 MUX design using PTL

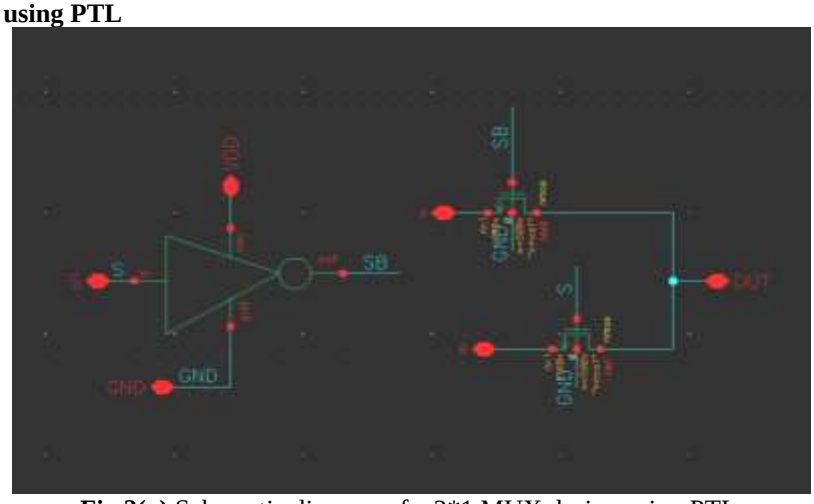

Fig.2(a) Schematic diagram of a 2*1 MUX design using PTL

The Fig.2 (a) shows the schematic diagram of a2*1 MUX design having 4 transistor, two NMOS and one inverter circuit using PTL (pass transistor logic).All the design done using labeling technique in cadence virtuoso tool.

Block diagram of 2*1 MUX design

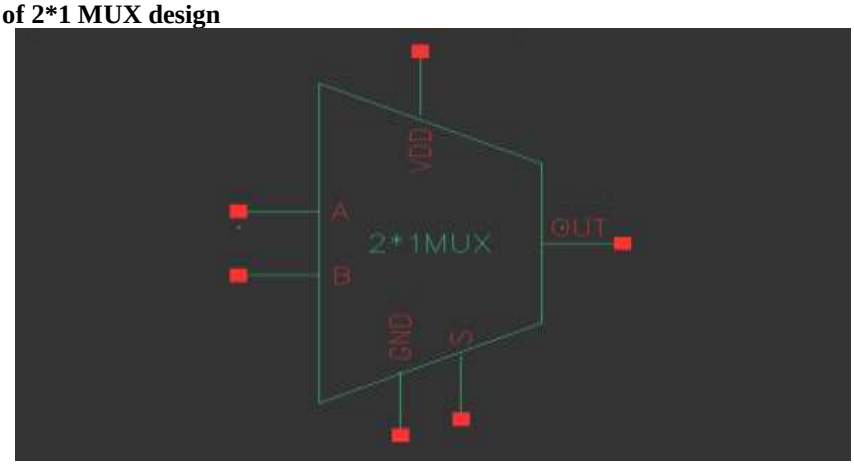

Fig.2(b) Block diagram of a 2*1 MUX design using PTL

The Fig.2 (b) shows the block diagram of a 2*1 MUX design having 4 transistor. Here A,B are the data input pin "S" pin is for the select line "OUT" pin is for the output pin, "GND" pin for ground and "VDD" pin is for biasing voltage supply.

4*1 Mux design using PTL

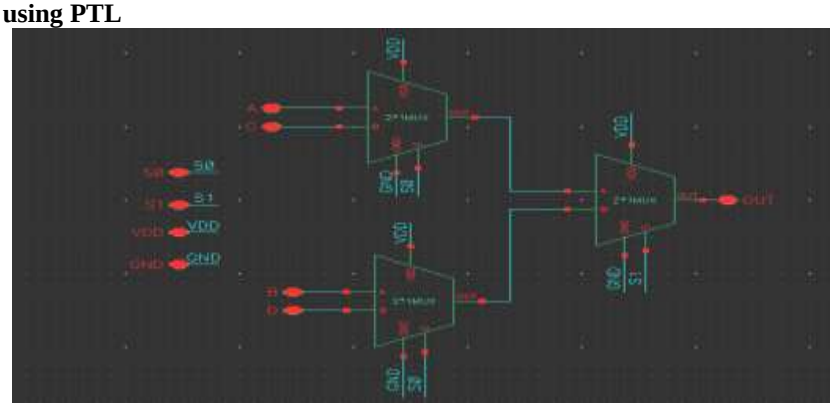

Fig.2(c) Schematic diagram of a 4*1 MUX design using PTL

The Fig.2(c) shows the schematic diagram of a 4*1 MUX design having 12 transistor. The 4*1 MUX design consist of three number of 2*1 MUX. Here the S0 and S1 are the select lineand all the design done using labeling technique in cadence virtuoso tool.

Block diagram of 4*1 MUX design

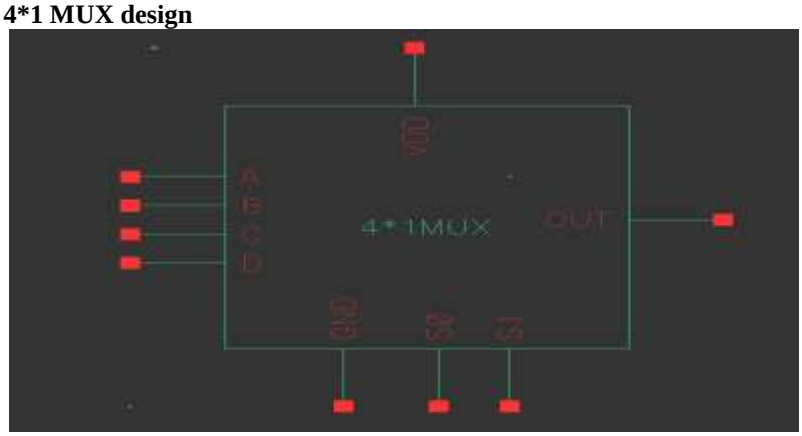

Fig.2(d) Block diagram of a 4*1 MUX design using PTL

The Fig.2 (d) shows the block diagram of a 4*1 MUX design having 12 transistor. Here A,B,C,D are the data input pin S1,S0 pin are for the select line "OUT" pin is for the output pin, "GND" pin for ground and "VDD" pin is for biasing voltage supply.

Design of a clear pin for Univarsal-Shiftregister

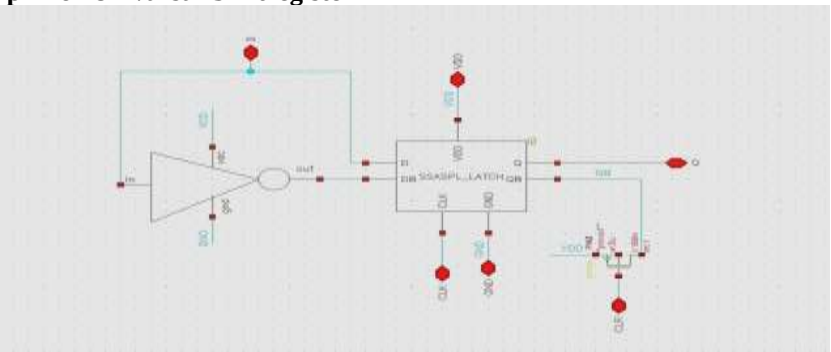

Fig.2(e) Schematic diagram of a SSASPL latch with clear pin

The Fig.2(e)shows the Schematic diagram of a SSASPL(static differential sense amp shared pulsed latch) with clear pin. Here a clear pin introduced when it activated it clear the previous data stored in the latch. A NMOS is connected to the "QB" output pin of the SSASPL latch all the design done using labeling technique in cadence virtuoso tool.

Proposed single clock pulse generator

The proposed single clock pulse generator (SCPG) is the combination of different circuits stage like complimentary pass transistor logic base AND gate circuit, inverted inverter base delay circuit and some buffer circuits. In inverted inverter circuit consists of two NMOS and two PMOS transistor the 2 NMOS transistor having the width of 500nm.and 2 PMOS transistor having the width of 500nm.and each inverter circuit consists of 1NMOS and 1PMOS transistor having width of 500nm. The input signal v-pulse is supplied to the inverted inverter circuit and the output was further feed to the inverter circuit. The single clock pulse circuit operates in two VDD supplies, one is connected to the inverted inverter delay circuit and other is connected to all inverter circuits. The VDD supply to the inverted inviter delay circuit is 2.5V and 1.8V DC supply is given to the inverter circuits. All the connection of the circuit element is designed using labelling technique in Cadence Virtuoso. The length of each transistor is 180nm.

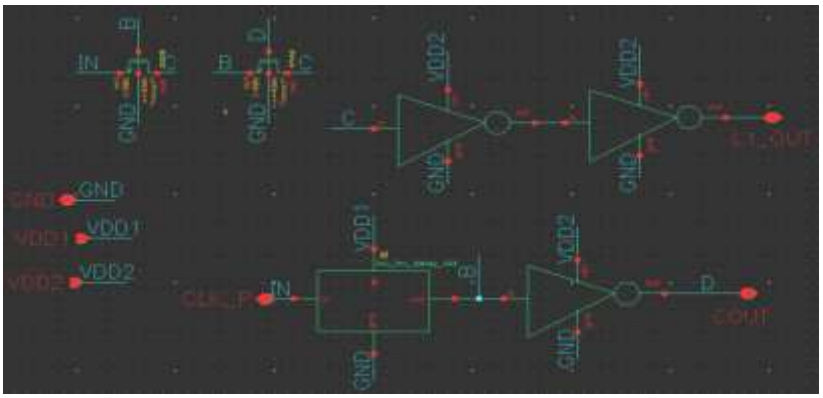

Fig. 2(f) Schematic diagram of the proposed single clock pulse circuit.

Delay circuit design

The principle of delay circuit is based on inverted inverter logic. Here the inverted inverter [14] delay circuit contains 2 NMOS and 2 PMOS transistors of 500nm width.

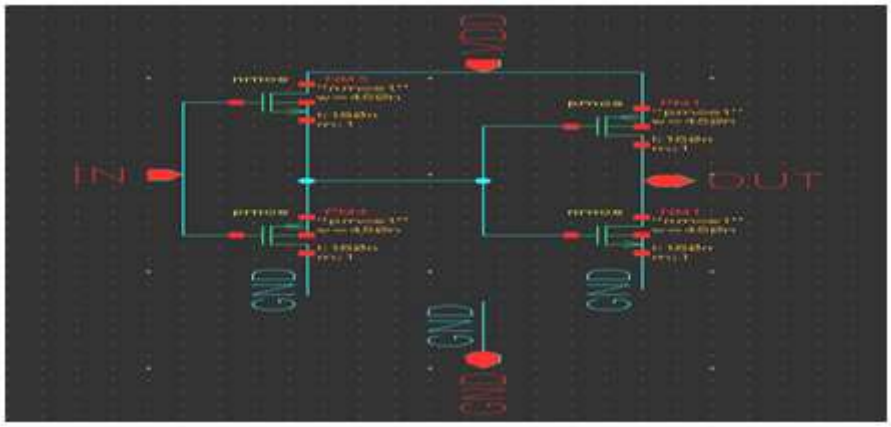

Fig.2 (g) Schematic diagram of inverted inverter delay circuit. [14]

Proposed 4-bit Univarsal-Shift register

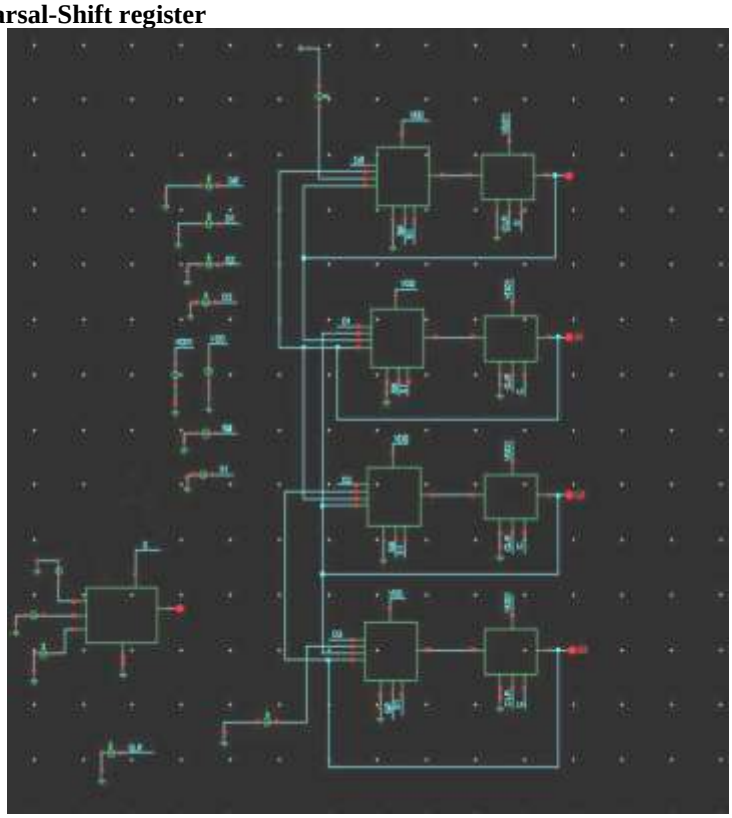

Fig.2(h) Testing diagram of Universal shift register

TheFig.2(h)shows the Testing diagram of a Proposed 4-bit universal shift register. Here the biasing voltage VDD for the 4*1 MUX is 2.5v and the biasing voltage VDD for the latch circuit is 1.8v.here a SCPG connected to 4 number of latches using labelling technique in Cadence Virtuoso. If the number of register increases then a clock pulse generator (CPG) will be required for overcome the timing miss match of the latches.

IV. Result Analysis

After designing the 4-bit universal shift register transient response has been analyzed and average power and area is calculated. For testing of the proposed 4-bituniversal shift register two different range of v-pulses are required, one for clock pulse generator and the other for the latch circuit. All connections of the latch and clock pulse generator circuit are done by labelling technique.

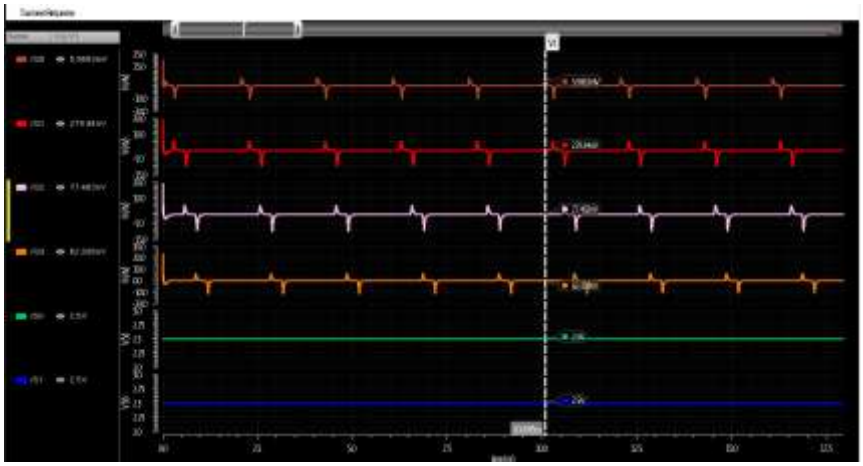

Fig.3(a) Transient response of the proposed 4-bit universal shift register in no change operation

The proposed 4-bit universal shift register is designed and tested using Cadence Virtuoso version (6.1.6-64b.500.4). The fig 3(a) shows the transient response of the proposed 4-bit universal shift register for no change operation. The clock pulse of 2ns and input of 40ns time period has been given as input.

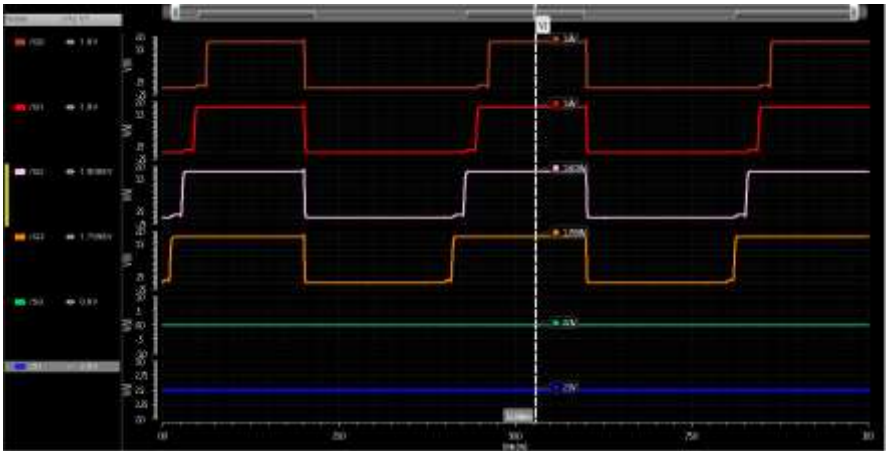

Fig.3(b) Transient response of the proposed 4-bit universal shift registers for left shift operation

The Fig.3(b)shows the transient response of the proposed 4-bit universal shift register for left shift operation. The clock pulse of 2ns and input of 40ns time period has been given as input.

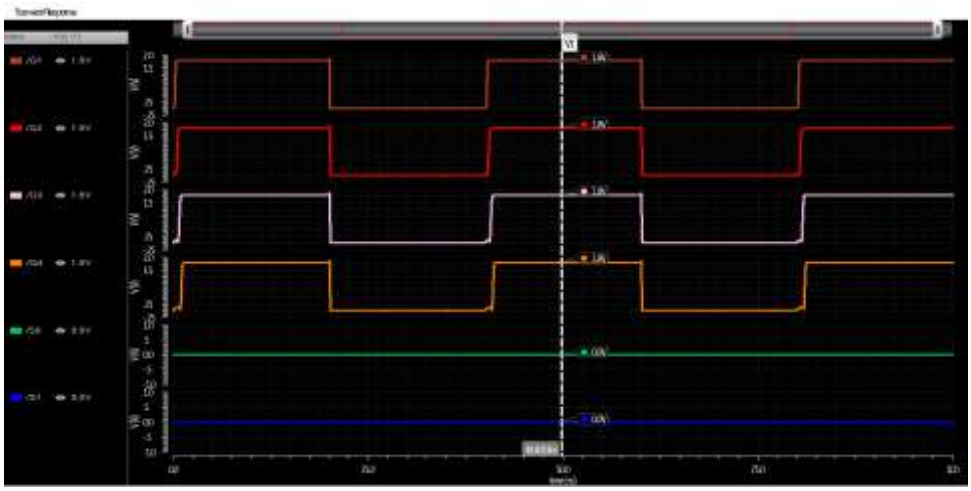

Fig.3(c) Transient response of the proposed 4-bit universal shift registers for parallel load operation

The Fig.3(c)shows the transient response of the proposed 4-bit universal shift register for parallel load operation. The clock pulse of 2ns and input of 40ns time period has been given as input.

Fig.3(d) Transient response of the proposed 4-bit universal shift register for right shift operation

The Fig.3(d)shows the transient response of the proposed 4-bit universal shift register for right shift operation. The clock pulse of 2ns and input of 40ns time period has been given as input.

Power measurement of the proposed design

The average power calculation is done in cadence virtuoso ADEL calculator window and measured for different frequencies like 500MHz and 100MHz for the proposed 4-bit universal shift register.

V. Noise Analysis

Due to noise in shift register many time some output data bit may be flip one to zero or zero to one .in this situation we cannot find out the desired output.to overcome this situation we need to calculate noise margin. The static noise margin (SNM) is found out by introducing DC noise at node Q (or Qb) [13].in fig 5(a) shows the butterfly plot of the latch design .here the two crossing point at the tips of the lobes are stable points and the center crossing is a Meta stable point. The SNM is interpreted as the length of the side of the largest square inside the butterfly lobe .if one lobe is smaller than other, then the cell is said to be imbalanced and the SNM is defined as the length of the largest square that fits inside the smaller of the two lobes .[13]

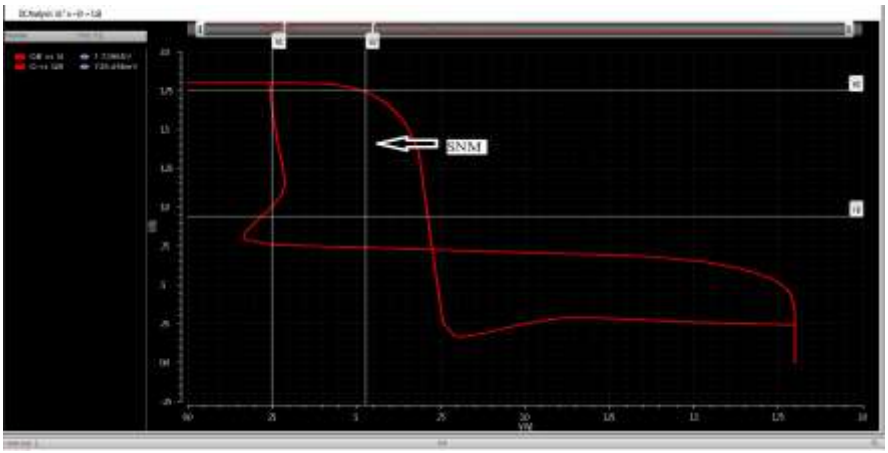

Fig.4 Butterfly plot of the SSASPL design

The fig.4 shows the SNM (static noise margin)of the SSASPL design and the measured SNM for the design is 850mv.

VI. Performance Analysis

The performance analysis of 4-bit universal shift register in 180nm technology has been provided in table number 2.

TABLE II

operation mode	Average power[mW]		Delay(ps)	Total transistor count in 4-bit universal shift register
	100MHz	500MHz		
parallel load	0.316	0.675	6140	92
Left shift	0.386	0.690	958	
Right shift	0.392	0.688	3140	
no change	0.291	0.649	-------	

VII. Comparison Analysis

Parameters	***CMOS***	**Proposed Design**
Power(mW)	67.2	0.678
Delay(pS)	532.51	3240
No of Transistors	216	92

VIII. Conclusion

In this paper a new clock pulse generator (CPG) and a 4-bit universal shift register has been proposed. The proposed 1-bit CPG consist of 12 transistors. And the proposed 4-bit universal shift register design consists of 92 transistors. The power and speed of 4-bit universal shift register has been calculated. The speed and the power consumption is better than other conventional flip-flop based universal shift register.

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