

Fpga Implementation of Anti-Wear Levelling Design of Ssd with Hybrid Ecc Capability Using Codes

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Abstract— The Joint Analysis Of Performance And Reliability, In Solid State Drive Design The Hybrid Error Correction Code Is The Alternative Choice. In Ssds Wear Leveling Leads In Early Performance Of Degradation. In That P/E Cycle Are Limited In Number Because Of Delay In Bit Error Rate Growth. The Proposed Anti-Wear Level Design Is To Avoid Performance Problem. Then The Performance Of Ssd With Hybrid Ecc Can Be Upgraded Without Offering Their Reliability. The Ability Of Proposed System Was Analysis By The Series Of Experiment. In Which The Proposed System Of Ldpc, Bch And Hamming Codes Enhanced To 55% Of Read And Write Performance In Ssds Without Disturbing The Investigated Ssd While Compared With Conventional Approaches.

Key Terms : Anti-Wear Levelling ,Bose - Chaudhuri-Hocquenghem (Bch), Low Density Parity Check (Ldpc), Bit Error Rate, Error Correction Code (Ecc), Solid State Drives (Ssd).

I. Introduction

The Flash Memory Chips In The Multilevel Cells Are Succeed In The Storage Market. The Data Can Be Last By The Growing Of Bit Error Rate Mnc Cells Problem Is Because Of Data Encoding And Programming Scheme.To Improve The Reliability And Performance Solid State Drive Is The Best Option Because It Gives Low Error Correction Codes By Using The Error Correction Code Hardware Wear Leveling Is Commonly Used For The Delay Time With Capability In Correction Because Of Decoding Delay It Not Only Inceaser The Performance And Also A Reliability. The Life Time Of Flash Memory Is Harmed Is Due To Negative Impacts Of Wear Leveling The Proposed Observation Is Anti - Wear Leveling Design For The Performance Of Ssds. If Flash Memory Chips (Nand) Is Divided Into Blocks And The Blocks Contains Number Of Spaces. The Page Consists Of A Spare Area (Stores Normal Data), Data Area (Stores User Data) These Are Used For Read And Write Operation.

In Modern Flash Devices Data Area And Spare Area Are Joined Together. The Blocks Residing Pages Are A Raced And Then Data Are Updated Now The Upto Data Are Able To Read The Out Of Date Data Are Known As Invalid Pages. These Are To Be Free Up Or

Recycled For New Data Upgradation. Due To Limited Number Of Programme/Erase Operation. There Is Only One Block Wear Leveling Is Used To Distribute Commonly For Programme And Erase Operation. This Increases The Life Time Of Flash Memory. The Upcoming Paper Of This Project Is Has Follows. Section Ii Discuss About The Prior Work And Motivation. Section Iii Discuss About Anti-Wear Level Design Based Hybrid Ecc. The Proposed System Of Garbage Collection And Executing Write. Section Iv Result Analysis And Comparison. Section V Hardware Implementation And Section Vi Is Concludes This Brief.

II. Prior Work And Motivation

The Storage Of Data By Controlling The Electrons Floating In Flash Cells That Utilizes Different Threshold Voltage Of Nand Flash Which Is Non -Volatile In Nature. To Represent A N-Bit Of Data $2n$ Voltage Of Programming Data In Nand Flash. Based On The Capacity Of Flashed Cells Each Nand Memory Is Classified Into Two Types. One Is Single Level Cells And Another Is Multi- Level Cells. One Bit Of Data Can Be Stored In Single Level Cells. When Compare To The Single Level Cell Flash Memory Multi- Level Flash Memory Cell Has Higher Priority Because Of Low Cost And Higher Cell Density. The Performance Of Read And Write Operation In Flash Memory Is Poor And Also Sensitive In Nature. It Has Smaller Number Of P/E Cycles And Higher In Bit Error Rate.

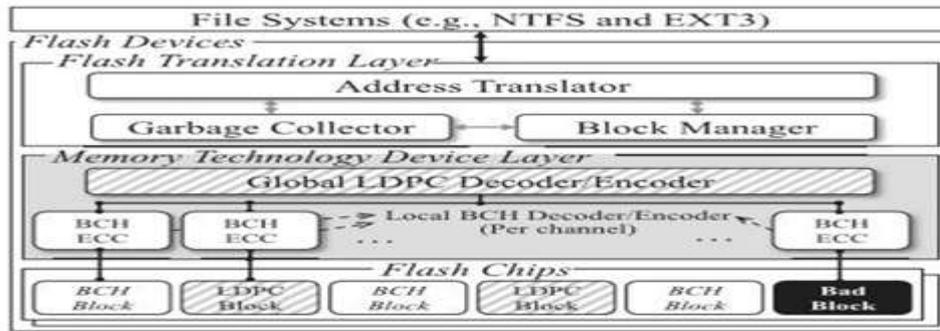


Fig.1. Hybrid Ecc Architecture

To Handle A Error In Data's Due To Electrical Noise And Read And Write Disturbance Ecc Is Commonly Used. To Increase The Reliability Of The Flash Memory Storage Devices Data Stored In Parity Bits. It Can Detect And Correct The Error With In It. Flash Storage Devices Has Easy To Implement Because Of Correction Strength And Simplicity. The Binary Bch Codes Of K-Bit Data And N-Bit Code Word And Distance To T+1. Bch Is For Error Solving And Parity Checking. Most Of The Error Detected Is Corrected Effectively. In Spite Of Locating In A Error Ldpc Is Used For Lightly Wood Ratio For Decoding Process. The Bit Receive One Or Zero Is The Probability Vector Of Ldpc. Ldpc Is More Flexible And It Require Complicated Hardware The Adopted Flash Memory Of Bch And Ldpc Has High Specification Of The Code In (N,K,T).

For A 512 Bit Of Data Minimum Of 12 Bit Error Correction Is Minimum. Bch Codes Has Atleast (8306,8192,12) Units As (N,K,T). In The Flash Page The Encoding And Decoding Data Is Shorter Than The Reading And Writing Of Data In A Flash Page. The Transferring A Data Between Ram Buffer And Flash Cells Takes More Time. Bch And Ldpc Of Flash Storage Devices Is Developed Here. The Complexity Of Hardware Bch Is Increases The Correction Strength At Higher Bit Error Rate. Ldpc Of Mlc Flash Memory Chip Has Default Error Correction Ssd.

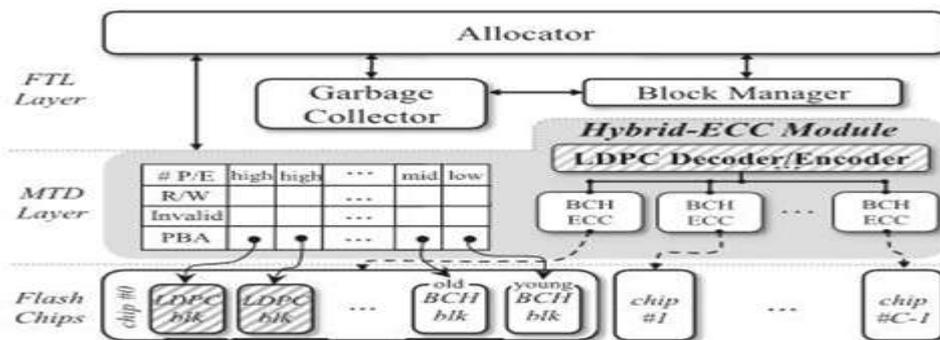


Fig.2. Existing Anti-WI Management System

These Above Motivation Used To Propose A Hybrid Ecc Design With Reliability And Input Output Performance. In The Bch Mode The Proposed Of Hybrid Error Correction Code Is Used. It Is Used For Better Read And Write Correction Performance. Further Adoption Of Bch With Low Detection Strength And Ldpc Has A High Correction Strength.

- 1) When The P/E Cycle Is Increases The Gradual Increase Of Rber Of Flash Cells. When Comparing With The Ldpc Bch Is Relatively Smaller And Has Low Strength.
- 2) In Prior Work By Adapting The Bch The Expected Reliability Not Affected. This Is Due To Data Encoding And Decoding When Rber Is Low. In The Hardware Design Ldpc Blocks Are Improved For Further Read And Write Performance In Gate Counts.

To Obtain These Drawbacks We Are Presenting The Anti-Wear Level Design To Overcome The Wear Leveling Design With Hybrid Ecc Characteristics. This Is Needed In The Accessing Performance And Reliability Of Data To Improve The Performance With Wear Leveling Due To Fast Increasing Of Bit Error Rate. The Combination Of Ldpc And Bch Is Used To Secure The Data In Hardware.

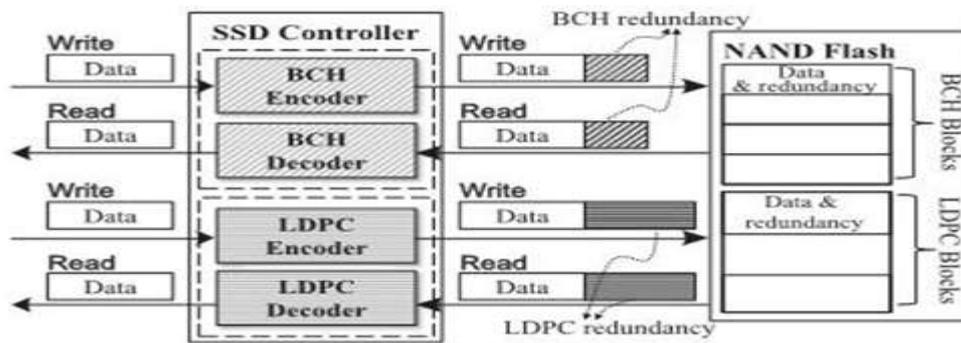


Fig.3. Comparison Between Ldpc And Bch

III. Anti-Wear Level Design Based Hybrid Ecc

3.1 Overview

A New Approach Of The Proposed Design Anti-Wear Leveling Design For Ssds With Hybrid Ecc Using Bch, Ldpc And Hamming Codes, Is Handover To Boost The Access Performance Of Ssds With Hybrid Ecc Capability Without Immolate The Reliability Of Ssds. With The Hybrid Ecc Capability, The Early Performance Degradation Problem Caused By Wear Leveling Can Evade In The Proposed Design, That Is To Let Flash Blocks Endure Different Levels Of Wear (Without The Activation Of Wl), And Then Exploit The Three Hybrid Ecc Properties To Have A Better Compromise Between Performance And Reliability. The Three Properties Are As Follows.

- 1) Flash Blocks Have A Relatively Low Bit Error Rate (Ber) At Their Early Usage Stage Such That A Weak Ecc (Eg. Hamming) With Better Encoding/Decoding Performance Is Enough.
- 2) Flash Block Have A Relatively Second Low Ber For Correction And Detection Of More Errors At Their Secondary Usage Stage That A Weak Ecc From First Early Usage (Eg. Bch) With Better Encoding/Decoding Performance Is Enough.
- 3) Flash Block Have A Relatively High Ber At Their Late Usage State That A Stronger Ecc (Eg.Ldpc) Is Required And Applied To Enhance Block Reliability.

The Aim Of The Proposed Design Is Doubled. The First To Obscure The Decoding (Read) Overheads Of Ldpc Blocks. This Means That We Should Efficiently Decrease The Access Rate Of Ldpc Blocks And The Advantage Of Three Module Of Ldpc And Bch And Hamming Blocks Is Cleverly Select The Data Saved In Ldpc And Bch And Hamming Blocks. The Second Is To Evade Doing Wl Might So As To Decrease The Performance Overhead, Since Wl Might Importune A Series Of Live Page Copies And Garbage Collection. Moreover, Equally Distributing The Wear Levels (Or Erase) To Each Block Will Be Baleful To The Lifespan Of Bch And Hamming Blocks. Consequently, Anti-Wl Write Strategy Is Proposed To Produce Uneven Wl Distribution Over Block To Take Benefits Of The Hybrid Ecc Module As Shown In Fig.4.

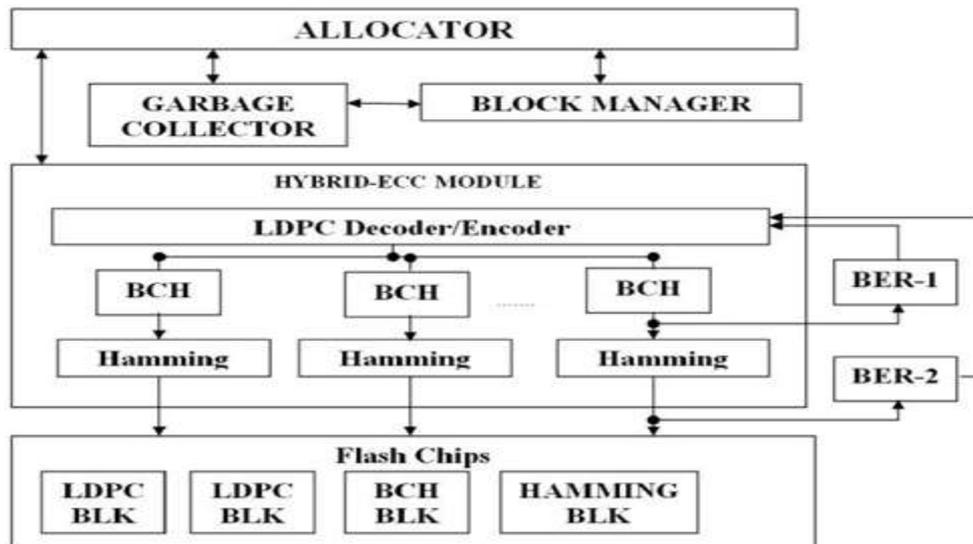


Fig.4. Overview Of Proposed Anti-WI Design With Ldpc, Bch And Hamming Codes

The Strong And Weak Units Of Ecc Capability Is Proposed In This Paper. The Combination Of Bch Ldpc And Hamming Are Used To Represent The Ber Each P/E Blocks In Number Higher The Ber Increases The P/E Cycles. When The Same Number Of P/E Cycles Is Applicable Then The Flash Memory Has Different Ber. So, The Proposed System Consider Of P/E Cycles.

In The Proposed System Of Anti-Wear Level Design Based On Hybrid Becc With And Flash Storage The Threshold Given At The Ber Is Higher Than That Of P/E Cycles In The Block. The Errors Are Corrected By The Data To Encode And Decode The Data In Bch. Whereas In The Ldpc, Given Threshold Is Lower Than The P/E Cycles. Then The Threshold Voltage Is Low It Can Be Corrected Only By Ldpc Not By A Bch. With Lowering The Bit Error Rate The P/E Cycles Of Flash Cells Are Adopted To Ldpc. The Bch Redundancy Of Data Has Only The Small Area Size With Means That Can Be Used In Spare Area. If The Bch Redundancy Of Data Is Directly Stores The Data It Needs Five Pages. Whereas, In The Ldpc Requires The Four Pages To Read Or Write A Data. In The Ldpc The Data And Redundancy Are Stored In Different Places When Compared To The Bch.

3.2 Garbage Collection In Anti-WI

The Proposed Anti-Wear Level Design Has The Garbage Collection Policy Is Literally Used For Collection Of Unused Data. Gc Uses In Uneven Leveling Of Distribution Over The Each Blocks. This Results In Blocks Containing Of Improper Data Which May Cause Degradation. The Accumulation Of P/E Cycles Is Very Fast. The Main Goal Of This Gc Is To Collect The Improper Data And To Arrange Them In Proper And It Is Delivered To The Required And Subsequent Request.

The Ldpc And Bch Contains Gc Is To Search And Calculate The Probability Of Data And Ratio Of Pages Taken. In This Case The Victims Are Ldpc Because It Has Smallest P/E Cycles. Similarly The Blocks Of Ldpc Are Required For Live Pages Between Dotted Lines The Last Request Can Be Executed In New Free Blocks And Hamming.

3.3 Ldpc, Bch And Hamming Codes

3.3.1 Hamming Code

Parallel Filter With The Same Response. A Discrete Time Filter Implements The Following Equation:

$$Y(N) = \sum_{I=0}^{\infty} X[N-I].H[1] \quad (1)$$

Where X[N] And Y[N] Is The Input And Output Signals, H[1] Is The Impulse Response Of The Filter. When The Impulse Response Is Non Zero, Only For A Finite Number Of Samples, This Filter Is Called Fir Filter, Else The Filter Is An Infinite Impulse Response (Iir). The Implementation Of Both Fir And Iir Filter Have Several Structure. The Interesting Property Of The Sum Of The Combination Of The Output Y[N] Can Also Be Obtained By Adding The Corresponding Inputs X[N] And Filtering The Results Signal With Same Filter H[1] Is Known As Parallel Filters. Fig.5 Shows The Parallel Filter With Same Response

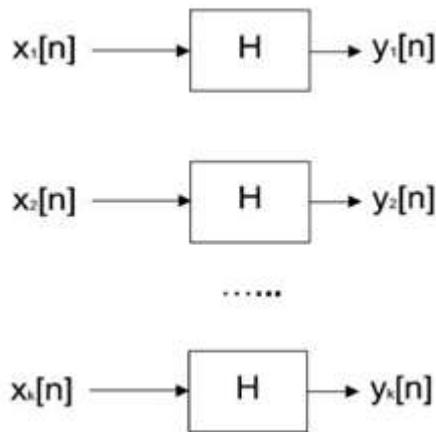


Fig.5. Parallel Filter With The Same Response

The New Technique Is Build On The Use Of Eccs. Adding N-K Parity Check Bits By Using The Simple Ecc Takes A Block Of K Bits And Generate A Block Of N Bits. K Data Bits Is Xor Combination Of The Parity Check Bits. This Combination Is Possible To Detect And Correct The Errors By Proper Designing.

The Data And Parity Check Bits Are Accumulated And Should Bits. This Is Done By Re-Calculating The Parity Check Bits And Comparing Accumulated Value Of Output Results.

Encoding Is Done By Caculating $Y = X \cdot G$ And Error Detection Is Done By Calculating $S = Y \cdot Ht$, Where The Operator \cdot Is Based On Module Two Addition (Xor) And Multiplication. Correction Is Done Using The Vector S, Known As Syndrome, To Identify The Bit In Error. The Similarity Of Values Of S To Error Position Is Gathered In Table 1.

Table 1 Error Location In The Hamming Code

$s_1 s_2 s_3$	Error Bit Position	Action
000	No error	None
111	d_1	correct d_1
110	d_2	correct d_2
101	d_3	correct d_3
011	d_4	correct d_4
100	p_1	correct p_1
010	p_2	correct p_2
001	p_3	correct p_3

3.3.2 Code Word Structure

The (31,21) Hamming Code Word With 32nd Bit Added To Provide An Overall Even Parity Check Is The Same Word As Defined For The Code. The Protocol Is Received All Hamming Codes Even Parity Bit Code Words And Processed Via 2 Bit Error Corrector. The 8 Word Intercalate Block Structure Produces The Received Data Stream Of 16 Consecutive Error Correction. Hence The Maximum Error Correction May In Some Cases (Low S/N And Extreme Cases Of Fading) Result Is Unacceptable Error Rate Out Of Decoder, The Data Stream Is Embedded Of The Protocol Utilizes Checksums. The Four Filter And Hamming Code Diagram Shown In Fig.6.

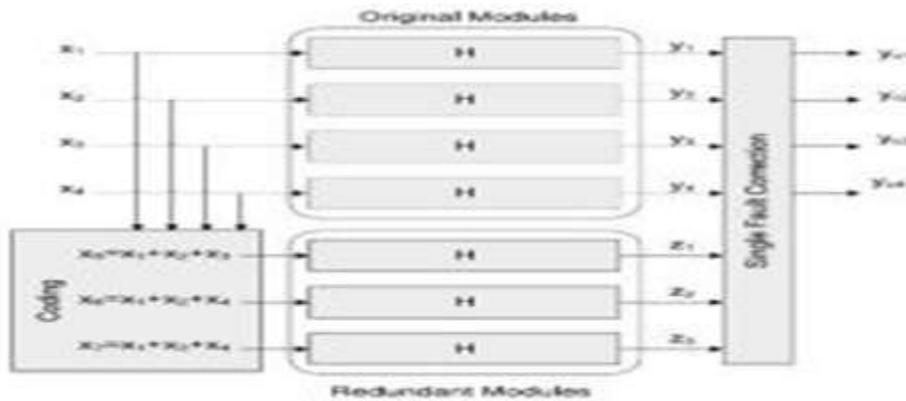


Fig.6. Proposed Scheme For Four Filter And Hamming Code

3.3.3 Ldpc And Bch

To Improve The Overall Performance Of Bch, Ldpc And Hamming Codes, Anti-Wear Leveling Design Of Wear Leveling

Over The Distribution Is Uneven. The Proposed Paper Shows The Addition Of Garbage Collector, It Uses The Separation Of Hot Data And Cold Data. Each Block Stores The Invalid Read/Write Data Flags And An Unused Content Of Data. Bch And Ldpc Contain The Corresponding Block That Has To Be Read In Order To Detect And Correction Of Noise. The Scheme Which Is Used To Ftl And Dftl Plays An Important Role In Adopting Of Mapping Information. The Fig.7 Shows The Ldpc Encoder And Decoder

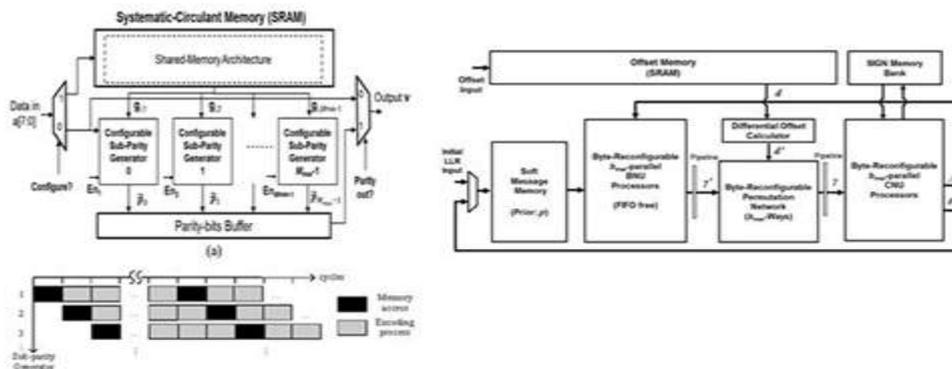


Fig.7. Ldpc Encoder And Decoder

In This Strategy, The Anti-Wear Leveling Of Distribution Blocks Over Read And Writes Performance In Increasing Of Security In Bch And Ldpc Codes. When Comparing To The Hamming, Bchold Blocks Erases The Centralized Operations In The Device. Further The Bchyoung Blocks Are Avoided In Order To Decrease The Possibility Of P/E Cycles. In The Most Of Applications Bch Takes Place The Better Read Write Characteristics Over Those Blocks.

IV. Comparison And Result Analysis

The Table 2 Shows The Comparison Of Anti-Wear Leveling Design For Ssds With Hybrid Ecc Using Multiple Codes. The Table Contains Slice Register, Lut, Number Of Iob, Fanout, Time Delay And Total Power Consumption.

Table 2 Comparison of proposed Anti-WL design using BCH, LDPC and Hamming.

	Hamming Code	BCH Code	LCPC Code	Anti - WL
Number of Slice Registers	0	0	168	68
Number of Slice LUT	136	790	141	2034
Number of Occupied Slice	61	482	41	857
Number of IOB	130	533	51	68
Total Power (mW)	36	98.16	88	37
Dynamic Power (mW)	0	0	52	1
Delay(ns)	16.923	24.265	2.088	4.648
Fanout effect	3.27	3.91	2.81	3.78

4.1 Energy Efficient Analysis

When Comparing The Multiple Codes Of Anti-Wear Leveling By Using The Number Of Slice Register Fig.8 Shows Below As Follows.

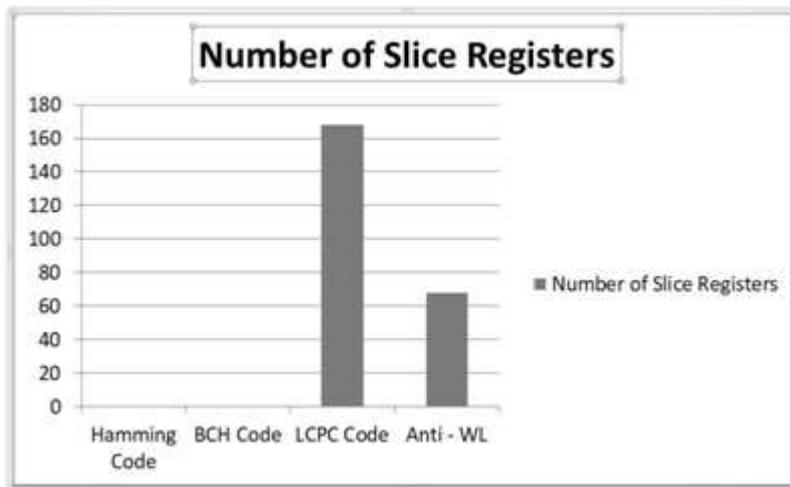


Fig.8. Analysis The Number Of Slice Register

4.2 Simulation Results

The Fig.9 Shows The Simulation Result Of Anti-Wl Design With Hybrid Ecc Using Codes.

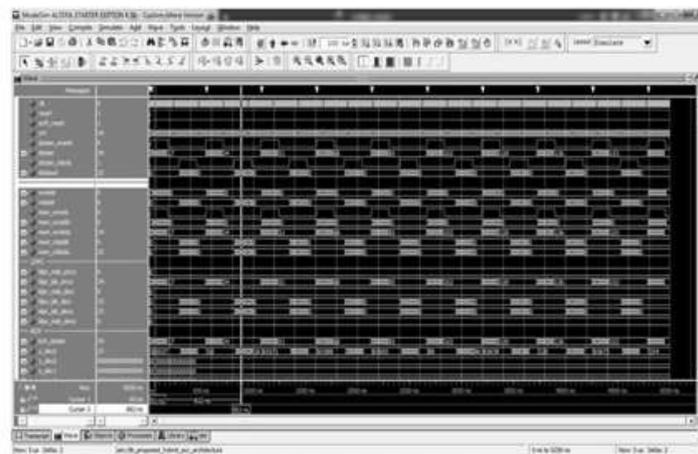


Fig.9. Simulation Result Of Proposed Design

4.3 Power Analysis

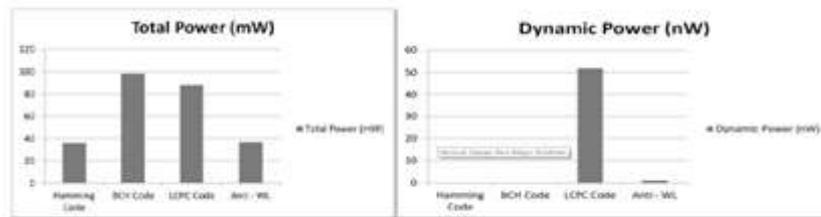


Fig.10. Power Report Of Anti-WL Design Using Codes



Fig.11. Power Report Of Hamming



Fig.12. Power Report Of Anti-WL

4.4 Area Analysis

The Total Power Consumption Results Of Four Approaches. The Power Report Of Each Codes Is Given As Follows: The Hamming Codes Consume The Power Of 0.36% And Bch Codes Consumed 3.15% And Ldpc Consumed 0.088% And The Total Power Consumption Of Anti-WL Consumed 0.37% And Dynamic Power Of Proposed System Is 0.001%. This Is The Power Analyzer Of Anti-WL Design. The Fig.9 Shows The Dynamic And Total Power Consumption Of Anti-WL Design.

The Fig.13 And 14 Shows The Area Report Of Anti Wear Leveling And Hamming Is Executed By Using The Xilinx Software.



Fig.13. Area Report Of Hamming



Fig.14. Area Report Of Anti-WI

4.5 Rtl View

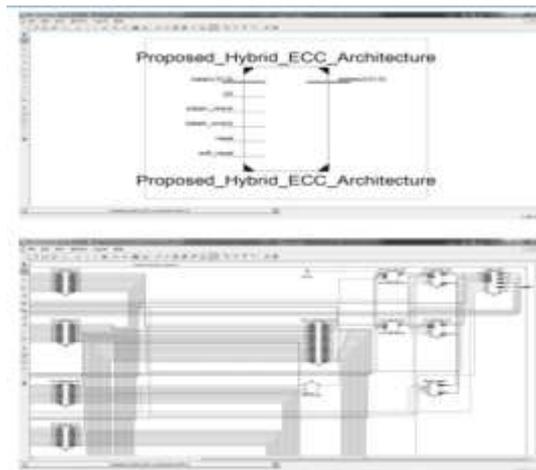


Fig.15. Rtl View Of Anti-WI Design With Codes

V. Hardware Implementation

Input Will Provided By Uart Interface Using Docklight Software From Personal Computer (Rx), And Also Test The Output From The Input Personal Computer (Tx). The Input Bit Size Is 8-Bit, It Will Provided To Rtl Vhdl Design Of Fpga Implementation Of Anti-Wear Leveling Design For Ssds With Hybrid Ecc Using Ldpc, Hamming And Bch Codes, And Test The Output On Same Docklight, The Memory Data Is Written Into Memory Or Not. The Rtl Design Is Synthesized In Fpga S6lx9 And Shown The Results Of Area, Power And Delay.

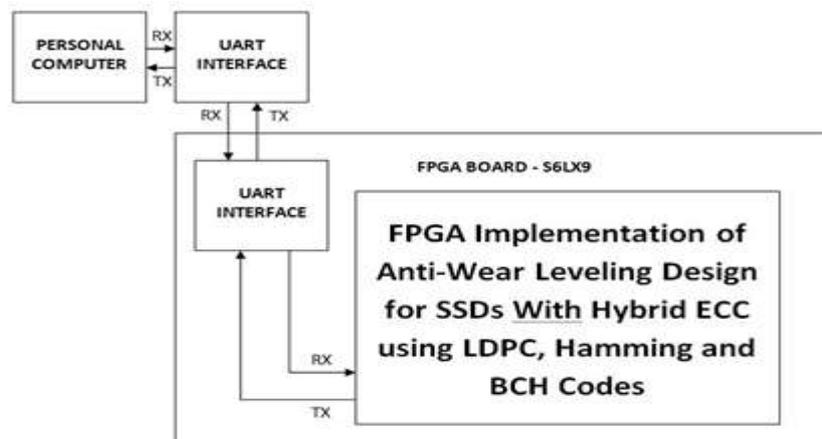


Fig.16. Hardware Implementation Architecture

VI. Conclusion

The Motivation Of Proposed Anti-WI Design Is A Series Of Experiments Was Conducted To Evaluate And Verify The Efficiency/Capability Of The Proposed Design. The Results Show That The Proposed Design Could Greatly Improve The Performance Of Ssds Without Affecting Their Endurance And Increase The Read/Write Performance Of Ssds. The Proposed Design Can Not Only Provide Better Performance By Hiding The Overheads Of Ldpc But Also Extend The Device Lifetime. The Anti-WI Design Of Ssds With Hybrid Ecc Using Multiple Codes Is Also Increasing The Security Performance Of Read/Write Performance.

In The Future Work, We Will Explore The Possibility To Further Utilize The Hybrid Ecc Architecture To Cooperate With Some Cost-Efficient Mapping Design Instead Of The Fine-Grained Level Mapping (I.E., Ftl) Considered In This Paper.

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