Fpga Implementation of Rounded Based Approximate Multiplier for Efficient Performance of Digital Signal Processing

D.Marimuthu¹, S.Bharath²
PG Student, M.E, VLSI Design, Surya Group Of Institution, Tamil Nadu, India
Assistant Professor , Communication System, Surya Group Of Institution, Tamil Nadu, India


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I. Introduction


The Rest Of This Paper Is Followed As. Section II Discuss About The Previous Work Of Approximate Multipliers. The Proposed Scheme Follows In Section III. ROBA Multiplier With FIR Filter With Its Hardware Work In Section IV. Accuracy Results Are Shown In Section V. In Section VI, Final Conclusion Was Drawn.

II. Prior Work

ROBA-Rounded Based Approximate Multiplier, Which Is Used To Determine The Accuracy Of The Multiplications In FPGA Processor. In Existing Comparison Separate Multiplier Design Is Used For Signed And Unsigned Operations. And It Require More Logic Size And It Consume More Power.

2.1 Signed Operation:

The Signed 2’s Complement Operation Is Used To Represent The Negative Operands As Well As Positive Operands In These Multiplications. When This Multiplier Is Negative Represented In Signed 2’s Complement. Each 1 Is Added, When It Requires The Addition Of The Multiplicand To The Partial Product.
2.2 **Unsigned Operation:**

The Positive Number Does Not Require An Arithmetic Sign. An M-Bit Unsigned Number Represent All Numbers Range From 0-255.

2.3 **Existing Implementation Of ROBA Multiplier:**

The ROBA Multiplier Is Modified By Conventional Multiplication Approach By Assuming The Rounded Values. Three Optimized Structure Was Followed For Both Signed And Unsigned Operations. Where The Inputs Was Represented In Two’s Complement Format. When The Sign Of The Inputs Was Determined, And Absolute Value Is Generated For Each Negative Value. Then Rounding Operation Was Made, Where Nearest Approximate Value Was Generated In The Form Of 2n. These Rounded Values Was Represented As Input A And B, Respectively. Then Shifting Operations Was Made. Shifter Register Can Have Both Parallel And Serial Inputs And Outputs. It Is Bidirectional Register Which Allow Shifting In Both Directions, (Left To Right Or Right To Left). Shift Register Are Used To Handle Data Processing.

\[ A \times B = (Ar - A) \times (Br - B) + Ar \times B + Br \times A - Ar \times Br. \]

\[ A \times B \sim = Ar \times B + Br \times A - Ar \times Br. \] (1)

When Two Numbers Are Added To Be Stored In Shift Register. It Converts The Data Between The Serial And Parallel Direction. It Is A Temporary Storage In A Processor. An Adder Is Digital Circuit That Performs Addition Of Numbers, It Is Used To Calculate The Addresses, Increment, And Decrement Operators Using Three Shift And Two Addition/Subtraction Method, The Value Of A And B Are Noted. This Is Equal To The Two Nearest Absolute Values 2p And 2p-1. Depending On The Magnitudes Of These Input Exact Multiplications Was Calculated In This Shifting Process. Finally, Absolute Value Of Both Inputs And Outputs Sign Of Multiplication Result Is Based On The Input Sign Be Determined And Then The Operations Be Performed For Unsigned Numbers.

![Fig. 1. ROBA Multiplier](image)

### III. Proposed System

3.1 **Proposed ROBA Multiplier:**

ROBA- Rounded Based Approximate Multiplier, Which Is Used To Determine The Approximate Rounded Values. In Previous Work ROBA Is Implemented By Multiple Constant Multiplication Technique (MCM) For Signed And Unsigned Multiplications, Which Is Followed By The Separate MCM Technique. Due To This Separate MCM Technique, There Will Be An Accumulation Of Large Area, Logic Size Was Increased, And Complexity Of Errors Was Obtained. To Overcome This Technique, Here Proposed To Implement The ROBA With FIR Filter. This Means Both Signed And Unsigned Operations In Single ROBA Multiplier. That Increases The Accuracy Of The Multiplications Technique In FPGA Processor. In This Multiplier, MCM Technique Will Propose To Design ROBA With FIR Filter. The Main Drawback Of MCM Technique Will Not Work Both Signed And Unsigned Operations. So To Overcome The Drawback, Here Proposed To Design With Rounded Based Approximate Multiplier.
3.2 FIR Filter


3.3 MCM Technique:

The MCM Technique Is Suitable For Implementation Of Large Order FIR Filter. Where MCM Technique Is Followed By Transpose Form Of FIR Filter. These Transpose Form Of Structure Has High Sampling Rate By Using Various Multipliers And Addition. For Each FIR Filter, It Increases The Linearity Function. MCM Technique Improves The Area-Delay Efficiency. In Existing Comparison, Separate Multiplier Design Is Used For Signed And Unsigned Operations In MCM Technique. And It Requires More Logic Size And It Consume Power. The Drawbacks Of MCM Technique Will Not Work Both Thing Of Signed And Un Signed Multiplication. So It Is Need To Design MCM With Rounded Based Approximate Multiplier That Includes Both Signed And Unsigned Operation In Single Multiplier.

3.4 Proposed Approximate Multiplier With FIR Filter:

FIR Filter Is Widely Used For Several Digital Signal Processing. The Frequency Specifications Require The Large Order FIR Filter. These Filter Support High Sampling Rate For High-Speed Digital Communications. A Real Time Implementation Of Large Order FIR Filter Increases The Linearity Function. Several Design For Efficient Realizations Of FIR Filters Uses The Multiple Constant Multiplication Methods. This MCM Technique Reduces The Different Complexity. The Realizations Of Multiplications Give The Input, Which Is Multiplied With Set Of Constants. This MCM Approach Mainly Implemented By Large Order FIR Filter. It Improves The Area-Delay Efficiency. Due To The High Sampling Rate, It Operates On Transpose Form Of Structure. The Filtering Coefficients Are Utilized To Reduce The Complexity Of The Realization Of Multiplications.

Fig. 2. FIR Filter

Fig. 3. ROBA Multiplier With FIR Filter

3.5 Proposed Adder Design:
3.5.1 HMPE Structure:
The HMPE Structure Consists Of Two Parts,
A Regular Prefix Adder
A Modified Excess-One Unit

![Parallel Prefix Adder](image)

**Fig. 4. HMPE Structure**
First, The Two Operands Are Added Using Prefix And The Result Is Conditionally Incremented Based On Control Signals Generated By The Prefix Structure.

3.5.2 Parallel Prefix Structure:
The Parallel-Prefix Structure Is Found To Be In High Performance Adders Because Of The Delay Is Logarithmically Proportional To The Adder.

![Parallel Prefix Adder](image)

**Fig. 5. Parallel Prefix Adder**
It Consist Of 3stages
3.5.2.1 Pre Computation:
In Pre Computation Stage, Here Two Inputs Are Generated And Computed.

\[ P_i = A_i \oplus B_i \]
\[ G_i = A_i \land B_i \]

3.5.2.2 Prefix Stage:
In The Prefix Stage, Generation And Computation Of The Signal Are Computed At Each Bit. The Black Cell Generates The Ordered Pair In The Gray Cell, Where It Generates Only The Left Signal.

![Prefix Stage Diagram]

3.5.2.3 Final Computation:

\[ S_i = P_i \land G_i - 1 \]
\[ C_{out} = G_{N-1} \]

IV. Analysis Of Experimental Results
Here, The Implementation Of Rounded Based Approximate Multiplier With FIR Filter Shown The Results Of Area, Power And Timing Report.

3.5.3 16 Bit Brent Kung Adder:
Brent Kung Adder Is A Very Well-Known Logarithmic Adders. It Has Different Intermediate Nodes. The Main Drawback Of This Adder Is, Thus The Rise Time And Fall Time Nodes Does Not Same. So, To Overcome This Drawback Buffer Stages Are Used With The Precomputation Process. Where It Generate The Inputs And Propagate The Outputs From This Adders

V. Hardware Implementation
The Input Will Provided Through UART Interface Communication Regarding The Input Frequency. It Undergoes For Testing. The Designing Of Low Pass Filter With ROBA Multiplier At Sampling Frequency (Fs) =5MHZ. So, Here Need To Test The Input Frequency Range Up To 1-10 MHZ, Where The NCO/VCO Will Help For Frequency Range Up To 1-10 MHZ, The Input Frequency Will Provided To FIR Filter With ROBA Multiplier, And The Output Frequency Will Provided Through DAC, And Test The DAC Output Using Oscilloscope. The Main Advantages Are Followed As Common Multiplier Design For Signed And Unsigned Operations, And Less Logic Size, Power, And Delay.

![Hardware Implementation Diagram]
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Fig. 8. Hardware implementation of ROBA with FIR filter

Fig. 9. RTL View Of ROBA Multiplier

Fig. 10. Simulation Results Of ROBA 1

Fig. 11. Simulation Results Of ROBA With FIR Filter 1
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Fig. 12. Simulation Results Of ROBA With FIR Filter 2

Fig. 13. Power Report

<table>
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<tr>
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<tr>
<td>Number of Slice Registers</td>
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<tr>
<td>Dynamic Power (mW)</td>
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<td>Fanout (ns)</td>
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Fig. 14. Graphical Representation Of Power Report
Finally, It Can Be Seen That The Implementation Of Rounded Based Approximate Multiplier With FIR Filter Shown The Frequency Coefficient Of FIR Filter. Usage Of Power Report = 14mw Delay Report = 17.980ns

VI. Conclusion

References
[1] Asant Kumar Mohanty, Senior Member, IEEE, And Pramod Kumar Meher, Senior Member. “A High-Performance FIR Filter Architecture For Fixed And Reconfigurable Application,” IEEE.