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SOI based Surface Potential Modelling for Semiconductor Memory Devices

B. Mohan Kumar Naik.
Dept. of ECE
New Horizon College of Engineering, Bengaluru- 560 103 Karnataka, India.
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Abstract
The study of the semiconductor construction and therefore the examination of physical look of the SOI-FinFET device has been industrial to approximation the standards of the surface potential by resources of rule. The model of the SOI-FinFET has surface potential that is to be investigated the options within the sub threshold region identical of the I-V characteristics, sub threshold swing and threshold voltage. the developed models and therefore the bestowed analysis exploitation TCAD tool development. by enhancing the dimensional structures, a sub threshold swing (STS) rate will from fifty five to sixty mV/decade and just about zero.35 to 0.40 V of threshold voltage of are often appreciated for SOI-FinFET.
Keywords-SOI-FET, Surface-Potential, TCAD, Drain-Current.

I. INTRODUCTION

Memory the stage a main title half and populates an excellent chip space in various of the VLSI circuit style. As memory devours an oversized fraction of assorted forthcoming styles, the memory density scaling will continue and track the logic for scaling trends [1-3]. As MOSFETs area unit scaled all the way down to millimicron scale, applied mathematics in would like of distinctions, variations in compound thickness, and upsurge in semiconductor unit threshold voltage (Vt) and consequently the regular and currents. In fringe of these static power rakishness in higher reminiscences, low offer voltages necessity to cast-off [4, 5].The Tri gate FinFET devices have currently substituted conservative coplanar MOSFETs for twenty nm [6, 7] and out of doors the channel management, and within the lower standards of sub threshold swing(SS) and drain inspired barrier lowering (DIBL). The gate brought drain discharge (GIDL) is institute to be a restrictive think about accomplishing ultralow ideals of OFF-state current (IOFF) [8, 9]. Few studies area unit investigated to condense GIDL current in FinFET devices. by increasing the edge voltage, the IOFF are often free for the semiconductor unit [10-13]. The multi-threshold voltage procedures area unit used, for example engineering drain and supply takes time beyond regulation regions, calibration gate work operate and by growing the gate length. lower discharge and moderates short channel effects (SCEs) are often achieved through Longer gate length.TheAnalytical modeling of semiconductor devices deliversvastlybeneficial insights into the underlying physics. The parameters like electrical parameters, electron density, Electric field surface potential, and etc.. to model the devices of semiconductors are inspected by using the semiconductor device channel.

There are totally different techniques arwont to measure the device Surface Potential. Parabolic-approximation, and super-position principle stay castoff to analyses the device. Analytically modelling of surface potential ar typically done practice super-position principal. A 2D(Two-Dimensional) analytically modelled for the potential of surface and field practice principle of superposition. meant for controls measured the encouragement of the mobile charges on the potential profile

II. SURFACE POTENTIAL MODEL

The two-dimensional(2D) read is employed to investigate and Poisson's-equation with the influence of the mobile charge [12]. The cross sectin read of the FinFET in x-y level is formed familiar within the Fig.1 2nd (two dimensional) Poisson's equation is as, $\frac{d^2\varphi}{dx^2} + \frac{d^2\varphi}{dy^2} = \frac{q}{\varepsilon_{Si}} n_i e^{\frac{\varphi - V}{V_t}}$ (1)

Where ψ(x,y) stands the surface potential static within the channel region, V_t= 0.0259 the thermal voltage V, Ni remains the essential carrier density, and V is that the similar Fermi potential. With principal of super position static potential [13] are often written as $\varphi(x, y) = \varphi_x + u_L(x, y) + u_R(x, y)$ (2)

Where ψ_x is solution- 1D Poisson's equation,

$$\frac{d^2\varphi}{dx^2} = \frac{q}{\varepsilon_{Si}} n_i e^{\frac{\varphi_x - V}{V_t}} \qquad (3)$$

ψ_x is obtained by twice integrating (3) and is obtained by

$$\varphi_x = V - 2V_t \ln\left(\frac{t_{Si}}{2\beta}\sqrt{\frac{qn_i}{2\varepsilon_{Si}V_t}}\cos\left(\frac{2\beta}{t_{Si}}x\right)\right) \quad (4)$$

Where βremains a constant (of x) differs from 0 to π/2, a function of *V*. For a given input voltage V_{gs}, β can be found from $\frac{V_{gs} - \Delta\phi - V}{2V_t} - \ln\left(\frac{2}{t_{Si}}\sqrt{\frac{2\varepsilon_{Si}V_t}{qn_i}}\right) = \ln\beta - \ln(\cos(\beta)) - \frac{2\varepsilon_{Si}t_i}{\varepsilon_i t_{Si}}\beta\tan(\beta)$ (5)

Where, Δϕ is that the distinction between gate effort of conductor and therefore the channel of semiconductor, The electrons movement within the device channel and between the supply close to the drain region, the negatron similar Fermi potential is constant in x-direction and disagrees within the y-directionThe similar Fermi potential is taken into account for DG-MOSFETs, until channel direction reaches to Vdsi.e. towards the shut of channel. and within the TFETs, the channel length remains constant (Vds) effort at the beginning purpose of the channel. this provides ψx a relentless worth in their direction of the supply junction neck

$u_L(x, y) + u_R(x,y)$is the solution to 2D Laplace equation,

$$\frac{d^2\varphi}{dx^2} + \frac{d^2\varphi}{dy^2} = 0 \qquad (6)$$

The solution to the Laplace equation can be given as,

where $u_L = \sum_{n=1}^{\infty} u_{Ln}(x,y)$ and$u_R = \sum_{n=1}^{\infty} u_{Rn}(x,y)$and $u_{Ln}(x, y) + u_{Rn}(x,y)$are mentioned as Eigen functions that can be attained as follows

$$u_{Ln}(x,y) = b_n \frac{\sinh(\pi(L-y)/\lambda_n)}{\sinh(\pi L/\lambda_n)}\sin\left(\frac{n\pi}{2} + \frac{\pi x}{\lambda_n}\right) \qquad (7)$$

$$u_{Rn}(x,y) = c_n \frac{\sinh(\pi y/\lambda_n)}{\sinh(\pi L/\lambda_n)}\sin\left(\frac{n\pi}{2} + \frac{\pi x}{\lambda_n}\right) \qquad (8)$$

Whereλ_n are Eigen values that are obtained from,

$$\varepsilon_{Si}\tan\left(\frac{\pi t_i}{\lambda_n}\right) = \varepsilon_i \tan\left(\frac{n\pi}{2} - \frac{\pi t_{Si}}{2\lambda_n}\right) \qquad (9)$$

The first order coefficients are obtained as explained in [15]

10)

$$b1 = \frac{2\lambda_1^2\tan(\pi t_i/\lambda_1)\sin(\pi t_{Si}/2\lambda_1)}{\pi^2 t_i\left(\frac{t_{Si}}{2} + \frac{\sin(\pi t_{Si}/\lambda_1)}{\sin(2\pi t_i/\lambda_1)}\right)t_i}(\phi_{SC} - V_{gs} - \Delta\phi)$$

11)

$$c_1 = \frac{\sin(\pi t_{Si}/2\lambda_1)}{\left(\frac{t_{Si}}{2} + \frac{\sin(\pi t_{Si}/\lambda_1)}{\sin(2\pi t_i/\lambda_1)}\right)t_i}\left(\frac{-4V_t\lambda_1}{\pi}\ln(\cos\beta_d) - \frac{2\lambda_1^2}{\pi^2}\frac{\varphi_x(t_{Si}/2) - \phi_{DC}}{t_i}\tan\left(\frac{\pi t_i}{\lambda_1}\right)\right)$$

Where φ_{SC} and φ_{DC} are source and drain junctions built in potentials respectively. $\beta_d$is calculated from (5). Even order quantities will be zero intended for symmetric structure **Error! Reference source not found.**. The expression for surface potential can be given as$\varphi(x,y) = \varphi_x + \cos(\pi x/\lambda_1)\left(\frac{b_1\sinh(\pi(L-y)/\lambda_1) + c_1\sinh(\pi y/\lambda_1)}{\sinh(\pi L/\lambda_1)}\right)$

(12)

III. DEVICE STRUCTURE

A 2D(Two-Dimensional) irritated opinion is shown in Fig one. where LFin, WFin, HFin, tox and tbox stay the peak,Length, and dimension of the channel, thickness of compound layer and suppressed compound layer matched. The FinFET is functioned within the sub threshold region where mobile devices ar abandoned and supply to channel & drain to channel region hurdles ar unforeseen. The device-limitations of Tri-gate FinFETs is as shown within the Table-1..

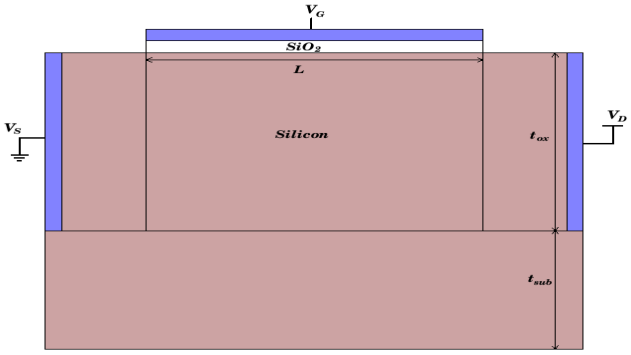


Fig 1-FinFET2 D view

Table 1- Parameter of FinFET device

Sl.No	Parameter	Symbol	Value
1	Fin Length	L_{Fin}	22 nm
2	Tox	t_{ox}	2 nm
2	Fin Width	W_{Fin}	20 nm
3	Fin Height	H_{Fin}	15 nm
4			
5	Buried Oxide Thickness	t_{box}	22 nm
6	Gate Work-function	φ_G	4.9 eV
7	Source/Drain Work-function	φ_{SD}	3.9 eV
8	Source/Drain Doping	$N_{S/D}$	10^{19} cm^3
9	Channel Doping	N_C	5×10^{17} cm^3

IV. RESULTS AND DISCUSSION

Based on the characteristics and therefore the analytical modeling the for Tri gate FinFET is valid with 2D(Two-Dimensional) numerical device simulation results that numerically solve poisons equation [14]. within the figures mentioned lines ar to be simulated knowledge|theinfo|the information} and symbols to the sculptural data.

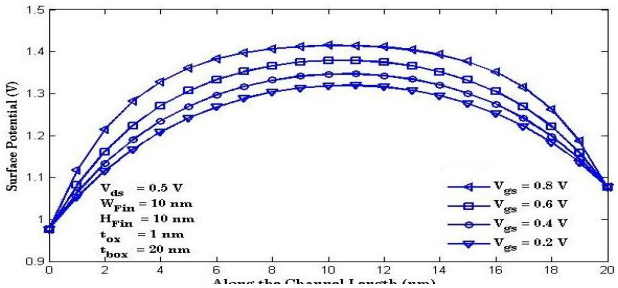


Fig.2. variation with gate Voltage for V_{DS} = *0.1 V.*

surface potential shown in Fig-2 shows the various input gate biases designed for Tri-gate FinFET through the direction of channel in variation with for a relentless drain bias VDS=0.1 V. from the higher than fig-2 that the expansion in input gate voltage potential of surface conjointly will increase on condition that a thicker layer of inversion charge for electrons to migrate from supply to empty finish to finish channel of the device.

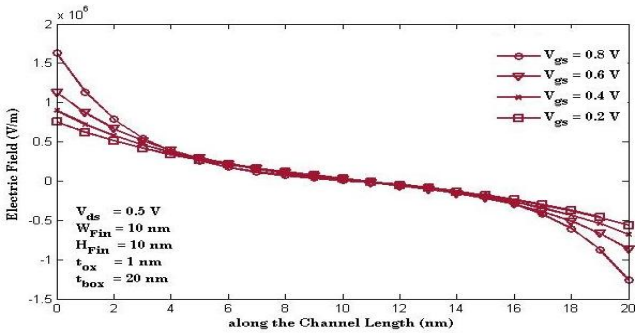


Fig 4.logarithmic scale,Transfer characteristics(TC) linear and at different drain bias (V_{DS}).

The *V-I* characteristics shown in Fig-4that thelogarithmic scale and linear for different drain biases.
The V-I characteristics for linear portion illustrations the upper charge for current of drain that is for higher input drain bias, conjointly shown in this distinction laterally with the input biases. V-I characteristics mistreatment graduated table that shows the off current (IOFF), and on current (ION) of the device. The device presentation is assessed by the upper ION/IOFF magnitude relation. This model demonstrations AN OFF current of 10-14 A and ON current of 10-5 A with ION/IOFF magnitude relation of around 109 for drain bias of zero.4.25 V.

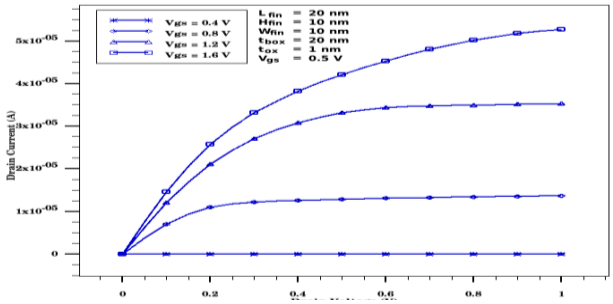
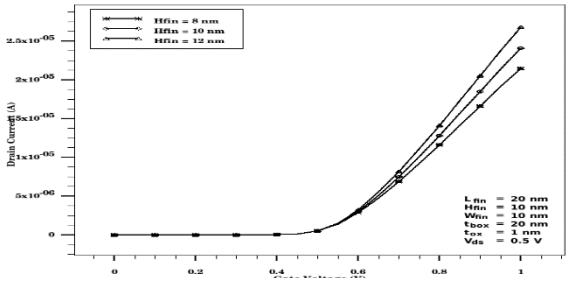


Fig.5.O/P characteristics for different I/P biases



.Fig 6. V-I Characteristics(VIC) for various Silicon Fin Height (H_{Fin}).

For the numerous input gate bias, the Tri-gate FinFET output characteristics is as shown in Fig five. The drain current is constant for input voltage but one.5 V, that is that the the purpose at saturation that is drain saturation voltage VDSat. that indicates that the input gate has no current at the (0.45 V), supply voltage is a smaller amount than threshold voltage (0.42 V). Above 1.5V input voltage for the channel length modulation will appear atthe output current by increasing linearly WRT drain bias.
Table-2 displays the standards of sub threshold swing and threshold voltage for unlike device parameters. Constructed on the attaineddata obtain a sub threshold swing of approximately55-60 mV/decade for device parameters $H_{Fin}=W_{Fin}=9\ nm$ and $L_{Fin}=42\ nm$ with threshold voltage of 0.39 V.

Table 2.Threshold voltage(Vt) and Sub threshold swing (STS for different parameters of device

Fin Length (L_{Fin}) nm	**Fin Width (W_{Fin}) nm**	**Fin Height (H_{Fin}) nm**	**Sub threshold Swing (SS) mV/decade**	**Threshold Voltage (V_t) V**
22	15	15	74.1	0.341

22	12	10	64.7	0.334
22	12	08	64.5	0.318
22	10	08	65.8	0.320
30	10	08	61.32	0.354
30	08	08	61.21	0.343
42	10	08	60.48	0.338

On the basis of work carried out, t for device parameters with H_{Fin}*=14 nm,* W_{Fin}*=10 nm* and L_{Fin}*=32 nm* shows a better performance with *SS* nearly *64 mV/decade,* I_{ON}/I_{OFF} ratio of 10^9, threshold voltage of *0.39 V* which shows better device constructionmeant for VLSI circuits and semiconductor memories.

V. CONCLUSION

The modelling SOI-FinFET for semiconductor reminiscences developed by estimating the surface potential values mistreatment super-position principle. These models remained wont to examine the performance of SOI-FinFET and I-V characteristics, of many geometrical parameters on the device performance, The numerical simulation results ar castoff to manifest the device parameters. By rising the dimensional options, a sub threshold swing (SST) just about to fifty five to sixty mV/decade and a threshold voltage of zero.35 to 0.45 V are often achieved for SOI-FinFET for semiconductor reminiscences.

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