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Power Quality Improvement For On-Board EV Using Boost PFC And An Interleaved SEPIC Converter

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Abstract :
The transition to electric mobility demands onboard chargers that are not only compact and efficient but also compliant with power quality standards. Nonlinearities introduced during AC–DC conversion often result in distorted input currents and reduced power factor, posing challenges to grid stability and charger performance. Addressing these concerns through simulation, a two-stage converter structure is modeled using MATLAB/Simulink, integrating a Boost Power Factor Correction (PFC) stage followed by an interleaved Single-Ended Primary Inductor Converter (SEPIC).
The input supply from the AC grid to an EV, then the AC-DC conversion in an EV chargers intrinsically incorporates non-linearities, giving rise to fluctuating input currents and an attenuated power factor. To diminish this concern, a Boost PFC stage employing a dual-loop PI control mechanism is deployed to precisely shape the input current and simultaneously regulate the DC link voltage at 350V. The stabilized DC link voltage is sequentially treated by a two-phase interleaved SEPIC converter configuration, stepping up the output to 430V for the purpose of battery charging. The interleaved SEPIC topology considerably improves efficiency, minimizes ripple, and enhances thermal performance. This entire system is simulated using MATLAB/Simulink and the results confirms the efficacy of the control strategy, reinforcing effective power factor correction, voltage regulation, and On the whole suitability for onboard EV charging applications.
Keywords: *Boost PFC, Closed loop control, Dual loop PI control, Interleaved SEPIC loop, On-Board EV*

I. Introduction

In recent years, the global push for environmental sustainability and efficient energy utilization has accelerated the transition toward electric mobility [1]. Among the critical subsystems enabling this transformation, onboard electric vehicle (EV) chargers play an essential role in delivering safe and effective charging from conventional AC grid sources [2].

The evolution from combustion-based vehicles to electrified transport has elevated EVs as central components of sustainable mobility. As EV adoption expands, there is increasing pressure on the charging infrastructure to deliver not only reliable energy transfer but also maintain system efficiency and comply with power quality standards [3]. Onboard chargers, which condition power directly from the grid to the battery, become central to this requirement. However, traditional AC–DC conversion techniques in these systems often contribute to electromagnetic interference (EMI), input current distortion, and low power factor, which deteriorate grid-side power quality [4].

A significant number of standard EV chargers rely on passive rectifiers combined with conventional filtering techniques. These designs often lack scalability and efficiency under dynamic loading conditions, failing to maintain sinusoidal current profiles and leading to higher Total Harmonic Distortion (THD) [5]. This situation increases the risk of violating grid standards. As a corrective approach, active Power Factor Correction (PFC) has gained traction due to its ability to improve regulation, enhance transient performance, and support compact, high-density power designs [6].

Within active PFC configurations, the Boost converter is preferred for onboard charging applications because of its simplicity and capability to stabilize the DC link voltage. This intermediate DC link serves as the power input to downstream converters [7]. However, the Boost PFC alone cannot cater to varying battery voltage demands, especially under multi-voltage or isolated conditions. A secondary DC–DC stage becomes necessary to ensure the appropriate output characteristics are achieved [8].

For the second stage, this work models a non-isolated, two-phase interleaved Single-Ended Primary Inductance Converter (SEPIC) following the Boost PFC. The SEPIC topology supports buck–boost conversion with continuous input and output current profiles, allowing flexible voltage regulation [9]. Interleaving this converter across two phases effectively reduces ripple, distributes thermal load, and enhances overall efficiency, making it a compact and robust choice for onboard chargers [10].

The overall system, modeled in MATLAB/Simulink, integrates the Boost PFC stage with an interleaved SEPIC converter. The Boost stage is controlled using a dual-loop PI controller to ensure unity

power factor and maintain the DC link voltage at 350 V. The SEPIC stage boosts this to 450 V for battery charging, also under closed-loop PI control. A complete simulation block representation of the proposed architecture is shown in Fig. 1.

The rest of the document is structured as follows : Section II presents the design and operating principles of the proposed converter architecture, including component sizing for the Boost PFC and interleaved SEPIC stages. Section III discusses the control loop architecture, focusing on the dual-loop PI control implemented for both stages. Section IV showcases the simulation setup and analyzes the key performance results such as voltage regulation, input current shaping, and battery charging behavior. Finally, Section V concludes the paper with a summary of findings and highlights the effectiveness of the proposed system for onboard EV charging applications.

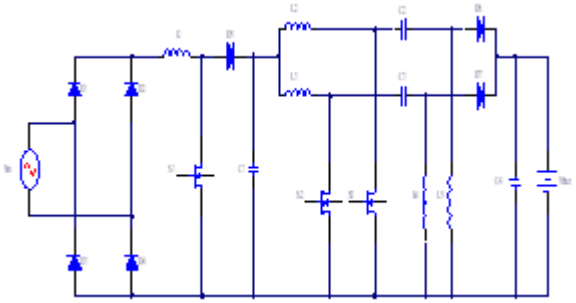

Fig 1: Onboard Battery Charger using Boost PFC with an interleaved SEPIC

The following section contains detailed system parameter design for Boost PFC and an Interleaved SEPIC is outlined.

General Architecture Overview

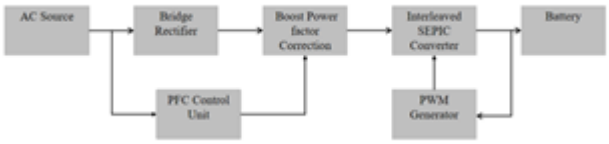

Fig 2 : Block diagram of the proposed Onboard Charger System

The proposed onboard electric vehicle (EV) charger architecture employs a two-stage topology that efficiently conditions and regulates power drawn from the AC grid. The first stage consists of a Boost Power Factor Correction (PFC) converter that serves to improve the input power factor, mitigate harmonics, and maintain a stable DC link voltage under varying load conditions. A dual-loop PI control system is used to ensure tight regulation of the DC link voltage and to achieve near-unity power factor operation. This intermediate voltage serves as the input to the second stage, which is a non-isolated interleaved Single-Ended Primary Inductor Converter (SEPIC).

The interleaved SEPIC stage boosts the regulated DC link voltage to a higher value suitable for battery charging, significantly reducing output current ripple and enhancing thermal performance. This is achieved by employing two SEPIC phases operating with a switching delay, thus enabling effective ripple cancellation through interleaving. The control of each stage is managed independently using dedicated PI controllers, ensuring precision in voltage regulation and current shaping. The functional block representation of this integrated system is shown in Fig. 2, outlining the signal flow from AC input to regulated DC output with appropriate control loops in place.

Interleaved SEPIC

The Fig. 3 shows the Interleaved Single-Ended Primary Inductor Converter (SEPIC), It is an enhanced version of the conventional SEPIC topology designed to improve power quality and thermal performance in medium power applications. In this configuration, two SEPIC converter stages operate in parallel and are interleaved with a 180° phase shift between their gate signals. This interleaving technique effectively reduces the input and output current ripple by allowing the ripple components of each phase to partially cancel each other out. As a result, the required filter size can be significantly reduced, leading to smaller passive components and improved dynamic response.

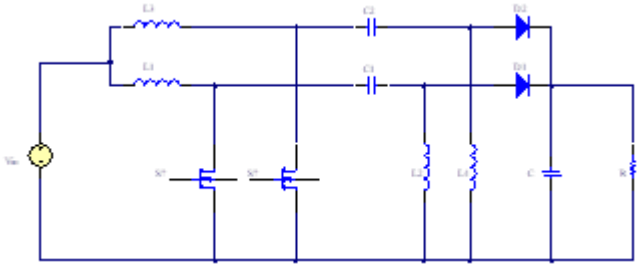

Fig 3: Circuit diagram of an interleaved SEPIC

Each SEPIC stage in the interleaved structure consists of a series-coupled inductor, coupling capacitor, diode, and switch, but the shared load allows both channels to contribute equally to the output power. The interleaving not only helps distribute the thermal stress across the components, enhancing reliability, but also enables higher overall efficiency due to reduced RMS current through the switches and inductors. Furthermore, by operating at higher frequencies with lower ripple, electromagnetic interference (EMI) is minimized, making it suitable for sensitive applications like photovoltaic energy systems and battery charging units.

In this work, the interleaved SEPIC stage is placed after the Boost PFC to step up the DC link voltage from 350 V to 450 V, providing a stable DC output suitable for charging electric vehicle batteries. The control of each SEPIC phase is managed independently using a dual-loop PI-based feedback mechanism. The advantages of interleaving are clearly evident in the improved efficiency, thermal balance, and reduced filter requirements compared to conventional single-phase converters.

II. System Parameter Design

The following section contains detailed system parameter design for Boost PFC and an Interleaved SEPIC is outlined.

Boost Converter Design

Inductance Calculation (L_1)

The intermediate DC link voltage of the converter is maintained at 350V with a peak AC input of 325V i.e. (230 V_{rms}). The regulated DC link voltage is fed to the input side of an interleaved SEPIC and it's reference output voltage is set at 450V for battery charging in electric vehicle's. The peak power capacity of the converter is 2.2kW. ΔI_L is taken as 25% of I_{L1} and computed inductance value of L1 using (1) and listed in Table 1 [5].

$$\Delta I_L = \frac{d * V_s}{f_{sw} * L} \qquad (1)$$

Capacitance Calculation (C_1)

Differeing from traditional boost converter, the ripple frequency of the boost PFC stage is not at switching frequency but instead double the input line frequency, i.e.,2f, as a result it requires a large sized capacitor. The smallest value of the DC link capacitance is calculated using (2) and shown in Table 1 [5].

$$C_{1min} = \frac{Iout}{2f\Delta V_{out}} \left(1 - \frac{Vin_{rms}}{V_{out}} \right) \qquad (2)$$

Interleaved SEPIC Design

Inductance Calculation (L_2, L_3, L_4, L_5)

Each SEPIC stage uses two inductors—one in the input side and the other in the series coupling path. For an interleaved SEPIC converter with two channels, four inductors are required (L_2, L_3, L_4, and L_5). The inductance of each is calculated using:

$$L = \frac{d * V_s}{f_{sw} * \Delta I_L} \qquad (3)$$

Coupling Capacitor Calculation (C_2, C_3)

The coupling capacitors in each SEPIC leg (C_2 and C_3) must block DC and transfer energy from the input to the output. Their sizing is based on:

$$C = \frac{Iout * D}{f_{SW} * \Delta VC}$$

Table 1: Nominal System Parameters

Parameter	Symbol	Value
AC Source Voltage	V_{in}	230V
Power frequency	f	50Hz
Switching frequency	f_{sw}	50kHz
Boost Inductor	L_1	1.5mH
DC Link Capacitance	C_1	2.6µF
Power rating	P	500W
DC link voltage	V_{dc}	350V
SEPIC Inductors	L_{SEPIC}	250µH
SEPIC Capacitors	C_{SEPIC}	7µF
SEPIC output voltage	V_{bat}	430V

Control loop architecture

The simulation of the onboard EV charger system incorporates a dual-loop control strategy for both the Boost Power Factor Correction (PFC) stage and the Interleaved SEPIC converter. This hierarchical control structure is implemented using standard Simulink blocks in MATLAB, ensuring voltage regulation, current control, and system stability under varying load conditions.

Boost PFC Stage Control

*I*n the Boost PFC stage, a dual-loop PI-based control is implemented. The outer voltage loop monitors the DC link voltage (targeted at 350 V) and compares it to a fixed reference. The voltage error is processed by a PI controller with proportional and integral gains tuned for fast yet stable response. The controller output serves as a reference current.

This reference current is compared with the measured inductor current in the inner current loop. The corresponding current error is fed into a secondary PI controller, which generates the required control signal for modulating the PWM duty cycle applied to the Boost converter switch. This two-level control approach ensures decoupled regulation and improved system response.

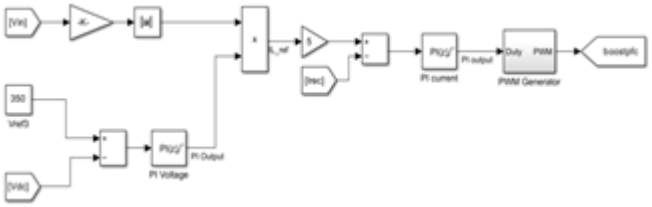

Fig 4: Boost PFC Control loop

The complete Simulink-based implementation of the Boost converter's dual-loop control logic is illustrated in Fig. 4, capturing both the outer voltage and inner current regulation loops integrated with the PWM generation mechanism.

Interleaved SEPIC Converter Control

The interleaved SEPIC converter is modeled using a dual-loop PI control structure designed to regulate voltage and current precisely. The outer loop maintains the output voltage at a target level of 450 V by processing the error through a PI controller. The resulting output defines the reference for the inner current control loop.

Each SEPIC phase is equipped with a dedicated current controller that compares the actual current to this reference and adjusts the PWM duty cycle accordingly. A small time delay is introduced between the switching signals of the two SEPIC phases to simulate interleaving behavior. This configuration improves current sharing and reduces ripple by staggering the switching events across the two channels.

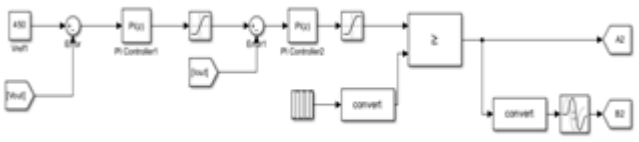

Fig 5: Interleaved SEPIC Control loop

The complete Simulink-based control structure for the interleaved SEPIC stage is illustrated in Fig. 5, detailing the feedback loops, control logic, and delayed switching implementation.

III. Simulation Results

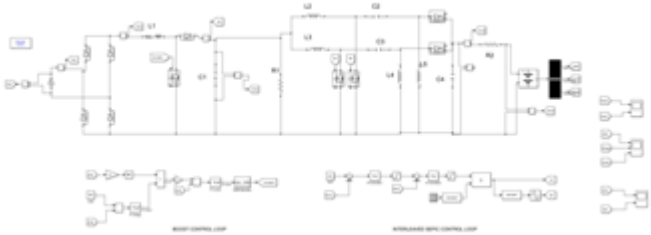

Fig 6: Interleaved SEPIC Control loop

To verify the designed onboard electric vehicle (EV) charger topology, an in-depth simulation study using MATLAB/Simulink is carried out.The simulation model, shown in Fig. 6, includes detailed subsystem representations of the Boost PFC stage and the interleaved SEPIC converter, each integrated with proportional-integral (PI) controllers for accurate regulation of voltage and current. The simulation considers a 230 V, 50 Hz AC input source with a 500-watt power capacity. The Boost PFC converter maintains the intermediate voltage at 350V, which is then handled by the interleaaved SEPIC converter to ensure a stable 450V output supply for the battery. Propotional - Integral (PI) Controllers are employed for managing voltage and current levels to achieve accuracy in control in both stages. The following simulation outcomes presented below includes Input Voltage and Current waveforms, DC link Voltage behavior, and load-end behavior including battery voltage, current, and state-of-charge (SOC) level characteristics.

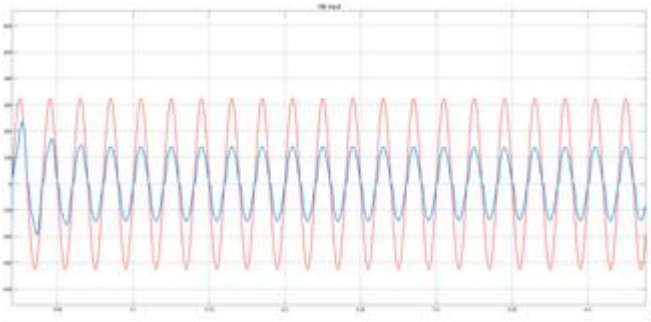

Fig 7: Input voltage and Input current

Fig. 7 shows thewaveform confirms successful Power Factor Correction (PFC) by showing input current nearly in phase with the input voltage and sinusoidal in nature. This indicates effective shaping of the current waveform to improve grid-side power quality and minimizing input current distortion.

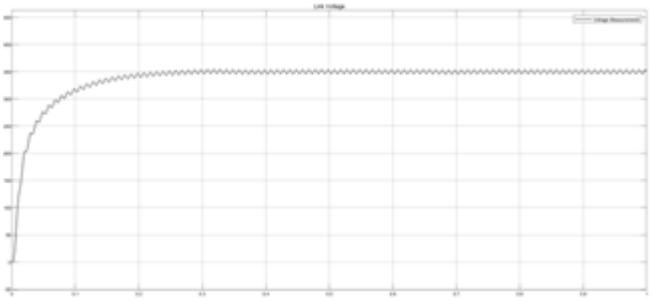

Fig 8: DC Link Voltage

As shown in Fig. 8, the DC link voltage is well-regulated at 350 V with minimal ripple, which confirms the robustness of the outer voltage loop in the Boost PFC stage and supports stable operation of the subsequent SEPIC stage.

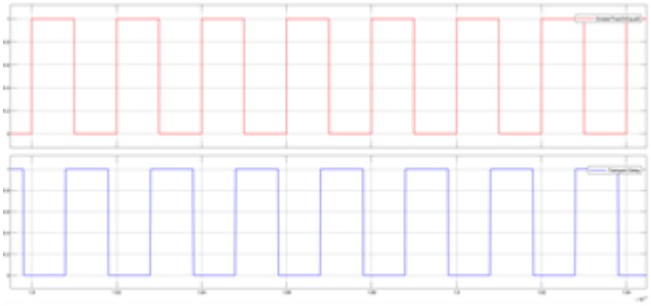

Fig 9: Switching states of interleaved SEPIC switches

Fig. 9 illustrates the gate pulses of the two interleaved phases in the SEPIC converter. A 180° phase shift is introduced between the switching signals to achieve proper interleaving operation. This phase shift allows partial cancellation of ripple currents from each phase, leading to reduced input and output current ripple. As a result, the system achieves improved efficiency, reduced EMI, and better thermal performance. These characteristics align with the interleaving benefits discussed in [6].

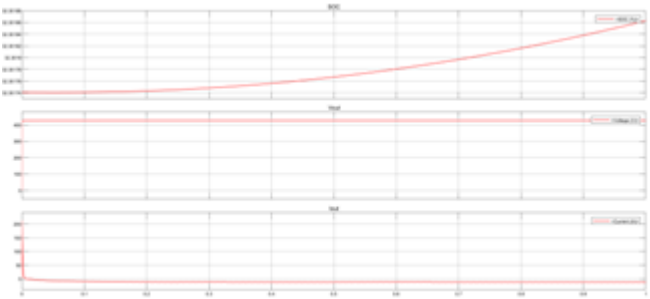

Fig 10: Waveforms of Battery SOC, Voltage and Current

Fig. 10 presents the output-side performance of the onboard charger during the battery charging cycle. The voltage increases and stabilizes at 450 V, which is the target output of the interleaved SEPIC converter. As charging progresses, the current gradually decreases, and the State of Charge (SOC) rises, indicating a smooth transition from constant current to constant voltage mode. This behavior demonstrates effective voltage regulation and proper functioning of the dual-loop PI control. The results validate the system's ability to deliver regulated power to the battery with minimal ripple and improved charging efficiency.

IV. Conclusion

This paper outlines a simulation-oriented design implementation of an onboard electric vehicle charger incorporating a Boost PFC stage cascaded with an interleaved SEPIC stage for enhanced power characteristics and to regulate the DC output voltage. The Boost converter effectively conditions the input current to be sinusoidal and aligned with the voltage. Thereby achieving higher power factor. The stabilized 350V DC link voltage is effectively handled by the interleaved SEPIC converter, provides a consistent 450V DC appropriate for EV battery systems. Simulated outcomes validate the system's constant voltage control capability, minimize ripple, and ensure seamless energy delivery to battery with progressive rise in state of charge (SOC). The entire system architecture demonstrates enhanced energy conversion performance, ripple minimization, and applicability for onboard EV charging applications.

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