Sapna Singh, Neha Arora , Neha Gupta, Meenakshi Suthar / IOSR Journal of Engineering (IOSRJEN) www.iosrjen.org ISSN : 2250-3021
Vol. 2 Issue 1, Jan.2012, pp.145-149

Simulation and Analysis of 6T SRAM Cell using Power Reduction Techniques

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***Abstract*- The demand for static random-access memory (SRAM) is increasing with large use of SRAM in System On-Chip and high-performance VLSI circuits. The high-density VLSI circuits and the exponential dependency of the leakage current on the oxide thickness is becoming a major challenge in deep-sub-micron CMOS technology. As the density of SRAM increases, the leakage power has become a significant component in chip design. This paper represents the simulation of 6T SRAM cells using low power reduction techniques and their comparative analysis on different parameters such as Power Supply Voltage, Delay, Operating Temperature and area efficiency etc. In comparison to the conventional 6T SRAM bit-cell, the total leakage power is reduced. All the simulations have been carried out on BSIM 3V3 90nm and 45nm at Tanner EDA tool.**

***Keywords* –CMOS Logic, Low power, Speed, SRAM and VLSI.**

I. INTRODUCTION

Static random access memory (SRAM), the most widely used embedded memory, typically occupies the largest portion of SoC die area, and often dominates the total chip power. In order to maintain performance, however, this has required a corresponding reduction in the transistor oxide thickness to provide sufficient current drive at the reduced supply voltages. To further reduce the leakage current, the stacking effect is used by switching off the stack transistors when the memory is ideal**.** The transistors have been lowered which also contributes to leakage currents and reduces the battery life dramatically. The low power reduction techniques reduce the leakage based on the dependencies of the tunneling currents on the terminal voltages, the gate oxide thickness, and the type of the transistor. Various efficient techniques which gives overall best performance over existing SRAM design approaches that allow the analysis and simulations of different parameters at 90nm and 45nm technology successfully on the basis of the power dissipation, speed and their temperature dependence with the area efficiency of the circuit.

II. LITERATURE REVIEW OF DIFFERENT SRAM CELLS

A. 6T SRAM CELL

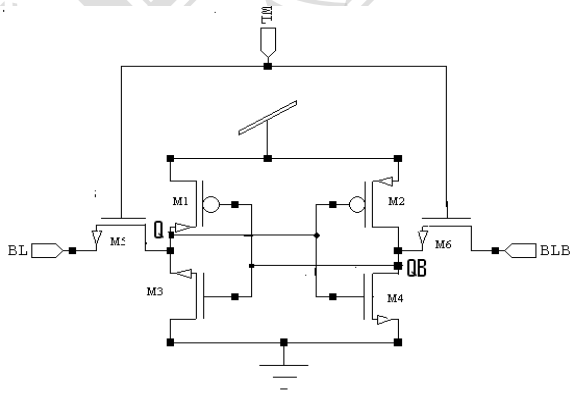

Fig.1 Schematic of 6T SRAM Cell

The schematic diagram of 6T SRAM cell is shown in Fig.1 [3]. During read, the WL voltage VWL is raised, and the memory cell discharges either BL (bit line true) or BLB (bit line complement), depending on the stored data on nodes Q and BQ. A sense amplifier converts the differential signal to a logic-level output. Then, at the end of the read cycle, the BLs returns to the positive supply rail. During write, VWL is raised and the BLs are forced to either V_{DD} (depending on the data), overpowering the contents of the memory cell. During hold, VWL is held low and the BLs are left floating or driven to V_{DD}. Each bit in an SRAM is stored on four transistors that form two cross-coupled. This storage cell has two stable states, which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit and the explanation here is based on the same. Access to the cell is enabled by

the word line which controls the two access transistor M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided to improve noise margins. During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM bandwidth compared to DRAMs. A SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents

B. 6TSRAM Cell using stacking Technique

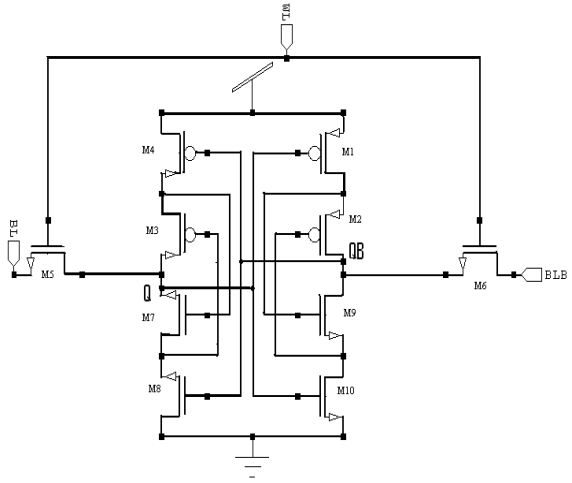

Fig.2 Schematic of Modified 6T SRAM Cell

In the Modified SRAM cell, is shown in Fig.2 the transistors M8, M4, M10 and M6 form cross coupled inverters. The basic idea behind our approach for reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground. This is based on the observation made in [4],[7] that "a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path." In our method, we introduce two leakage control transistors in each inverter pair such that one of the leakage control transistor is near its cutoff region of operation. Two leakage control transistors (PMOS) and (NMOS) are introduced between the nodes and of the pull-up and pull-down logic of the inverter. The drain nodes of the transistors and are connected together to form the output node of the Inverter. The source nodes of the transistors are connected to nodes of pull-up and pull-down logic, respectively. The switching of transistors is controlled by the voltage potentials at nodes respectively. This wiring configuration ensures that one of the leakage control transistor is always near its cutoff region, irrespective of the input. Hence the resistance of will be lesser than it's OFF resistance, allowing conduction. Even though the resistance of is not as high as it's OFF state resistance, it increases the resistance of to ground path, controlling the flow of leakage currents, resulting in leakage power reduction. Thus, the introduction of leakage control transistors increases the resistance of the path from supply voltage to ground.

C. 6T SRAM Cell using Asymmetric SRAM Cell technique

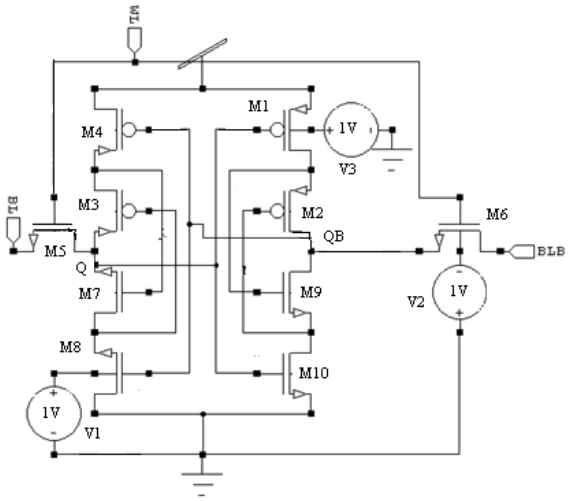

Fig.3 *Schematic of Asymmetric Modified 6T SRAM Cell*

In this technique, we propose an asymmetric SRAM cells that use a mix of regular- and high-V_t transistors. Common to all cells is *asymmetric* leakage power behavior: When the cell stores the preferred value, leakage power is significantly lower .This technique drastically reduces leakage power since ordinary programs exhibit a strong bias in their resident bit values. Compared to the six transistor cell, our cells also exhibit asymmetric access behavior. We can exploit this behavior to maintain fast access latency. Schematic of asymmetric 6T SRAM cell as shown in Fig.3. In this technique, we start by reviewing the conventional regular-V_t transistor cell and focus on where leakage power is dissipated. We then explain how we can reduce leakage power with no or little impact on access

latency by selectively "weakening" some of the transistors (i.e., replacing some transistors with high-V_t ones) [3].Initially, we ignore stability issues and present a simple to understand asymmetric cell design. Our asymmetric cell is best understood by explaining where leakage power is dissipated in the conventional regular-V_t cell. The majority of cells spend most of their time in the inactive state where the word line is pulled low and the two-bit lines are charged at V_{DD}.

In this state, most of the leakage power is dissipated by the transistors that are off and that have a voltage differential across their drain and source. Which are those transistors depends on the value stored in the cell. In Fig.3 we show the cell storing a one on the left side. In this state, the leaking transistors are M1, M6 and M8. If the cell was storing a zero on the left side, then the leaking transistors would be M4, M6 and M10. One way of reducing leakage power would be to use an high-V_t cell where all transistors are replaced with high-V_t ones. High-V_t transistors are not as strong and hence require a lot more time to discharge the relatively large capacitance of the bit lines.

III. SIMULATION AND ANALYSIS

All the circuits have been simulated using BSIM 3V3 90 nm and 45nm technology on Tanner EDA tool with supply voltage ranging.Fig.4-Fig.9 shows comparative analysis of the circuits stated above at 90nm and 45nm technology.

A. At 90nmTechnology

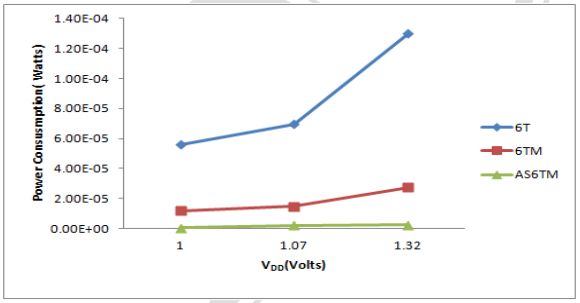

Fig.4 Power Consumption vs. Vdd for Different SRAM Cells

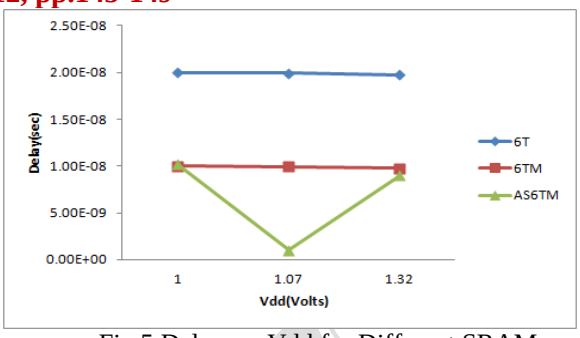

Fig.5 Delay vs. Vdd for Different SRAM Cells

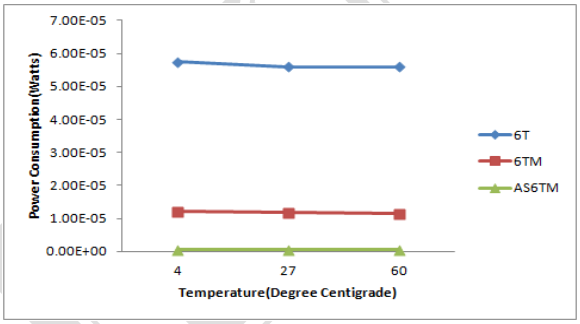

Fig.6 Power Consumption vs. Operating Temperature for Different SRAM Cells.

B. At 45nmTechnology

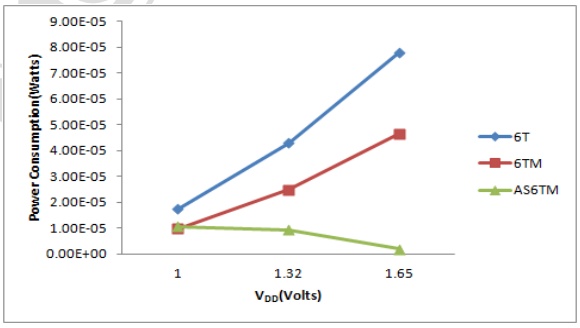

Fig.7 Power Consumption vs. Vdd for Different SRAM Cells.

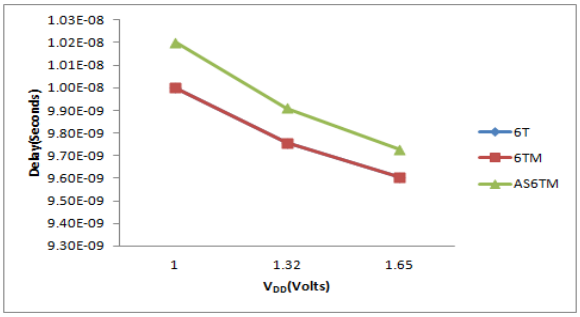

Fig.8 Delay vs. Vdd for Different SRAM Cells.

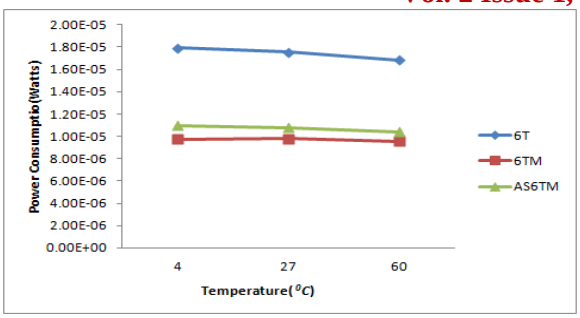

Fig.9 Power Consumption vs. Operating Temperature for Different SRAM Cells.

C. Simulation Result

TABLE 1: Power Delay Product Comparison of Different SRAM Cells at 27 ^{0}C.

Different SRAM Cells	Power Delay Product (Watt Seconds)		
	Vdd = 1v	Vdd= 1.07v	Vdd=1.32 v
6T	5.00E-14	3.05E-12	9.85E-13
6TM	6.43E-14	2.66E-13	6.37E-13
AS6TM	5.75E-15	2.20E-15	2.13E-14

V. CONCLUSION

Technology scaling demands a decrease in both V_{dd} and V_t to sustain delay reduction, while restraining active power dissipation. To increase their reliability, the lifetime of battery is a prime concerned at the cost of speed. The simulation results reveal low power techniques shows best performance for the range of power consumption, delay and temperature. In this paper, we present a Modified model using power reduction techniques that predicts the scaling nature of this leakage reduction effect and tries to find out an efficient SRAM memory cell in both the aspects power consumption and speed in terms of power delay product.

VI. ACKNOWLEDGEMENT

We would like to sincerely thank Prof. B.P Singh, Head of Department of Electronics & Communication, Mody Institute of Technology and Science, Lakshmangarh who inspired us to do this work. In addition we would like to thank Prof P.K Das, Dean, Faculty of Engineering, Mody Institute of Technology and Science for providing us resources to carry out our work.

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BIOGRAPHY

Sapna Singh received her B.Tech degree in Electronics and Communication Engineering from Kumaon Engineering College, Dwarahat in 2010 and presently pursuing M.Tech VLSI Design in Mody Institute of Technology and Science, Lakshmangarh. Her research interests are low power VLSI design, analog and digital integrated circuit design.

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