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Hardware/Software Co-Simulation of BPSK Modulator Using Xilinx System Generator

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Abstract— *The paper presents a theoretical background overview of the digital communication systems and the BPSK modulation. The BPSK modulation Represents an important modulation technique in terms of signal power. The BPSK system is simulated using Mat lab/ Simulink environment and System Generator, a tool from Xilinx used for FPGA design as well as implemented on Spartan 3E Starter Kit boards. The local clock oscillator of the board is 50 MHz which corresponds with a period of 20ns. The frequency of the BPSK carrier is 31,250 kHz.*

Key words*- BPSK, system generator, Spartan 3e*

I. INTRODUCTION

In the last years, a major transition from analog to digital modulation techniques has occurred and it can be seen in all areas of satellite communications systems, cellular and wireless. A digital communication system is more reliable than an analog one thanks to the advanced signal processing algorithms used at the transmitter and the receiver ends. The aim of the paper is to create a BPSK (Binary Phase Shift Keying) system made of a modulator, a channel and a demodulator. The modulated signal was achieved in the first Spartan 3E board, passed through a channel and transmitted to the second board, which behaves as a Demodulator. At the end of the demodulator, the modulating signal was obtained. The main difference is the System Generator block which makes possible the administration of the Xilinx components.

The paper is organized into 6 sections. The paper begins with an introduction in section 1. Section 2 presents the theoretical backgrounds about the digital communication system and about the BPSK modulation. After discussing in theory, implementation of the BPSK system in Mat lab/ Simulink and System Generator are presented in section 3. Section 4 is dedicated to the implementation of the system: modulator on the Spartan 3E Starter Kit boards. The results are discussed in section 5. The final section, 6, presents the conclusions.

II. THEORETICAL BACKGROUND

2.1 Digital Communication System

A typically digital communication system is presented in Fig.1. The components of the digital communication system are both digital and analog parts. The digital part consists of digital source/user, source encoder/ decoder, channel encoder/ decoder and the digital modulator/ demodulator. The analog part is made of the

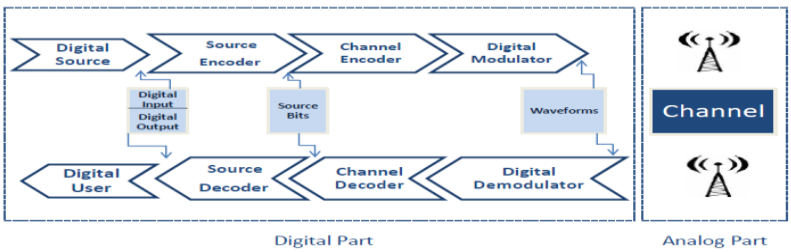

Figure 1. A Digital Communication System.

The message to be sent is from a digital source, in our case, from a computer. The source encoder accepts the digital data and prepares the source messages. The role of the channel encoder is to map the input symbol sequence into an output symbol sequence. The binary information obtained at the output of the channel encoder is than Passed to a digital modulator which serves as interface with the communication channel. The

main purpose of the modulator is to translate the discrete symbols into an analog waveform that can be transmitted over the channel.

In the receiver, the reverse signal processing happens. A channel is the physical medium that carries a signal between the transmitter and the receiver. The digital data is transmitted between the transmitter and the receiver by varying a physical characteristic of a sinusoidal carrier, either the frequency or the phase or the amplitude. This operation is performed with a modulator at the transmitting end to impose the physical change to the carrier and a demodulator at the receiving end to detect the resultant modulation on reception.

2.2 BPSK Modulation

Digital modulation is the process by which digital symbols are transmitted into waveforms that are compatible with the characteristics of the channel. The modulation technique used in this paper is BPSK (Binary Phase Shift Keying) and it is widely used in digital transmission..The BPSK modulator is quite simple and is illustrated in fig.2. The binary sequence m(t) or modulating signal is multiplied with a sinusoidal carrier and the BPSK modulated signal s(t) is obtained. The waveforms of the BPSK signal generated by the modulator are shown in fig.3.

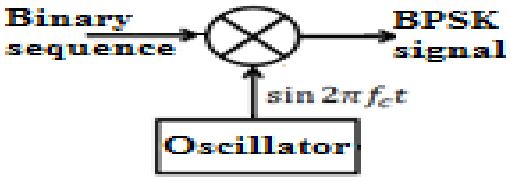

Figure 2. BPSK Modulator

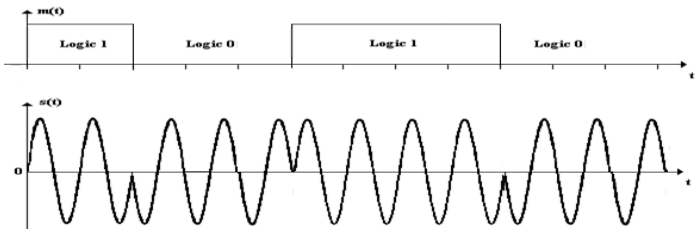

Figure 3. BPSK waveforms

III. BPSK SYSTEM

3.1 BPSK System in Simulink

The BPSK modulator (fig.4) is made of two sine carriers, the second one delayed with 180º and a switch which will choose between the first or third output depending on the value of the second input. If the second input is "1", the output value will be sine, but if the second input is "0", the output will be –sine.

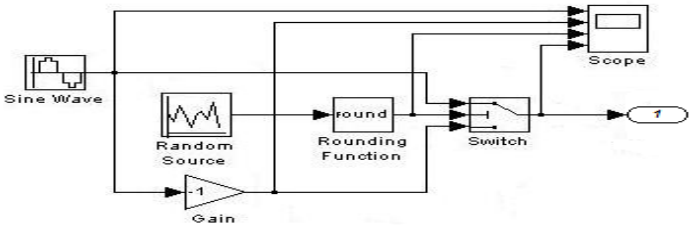

Figure 4. Binary data source and BPSK Modulator

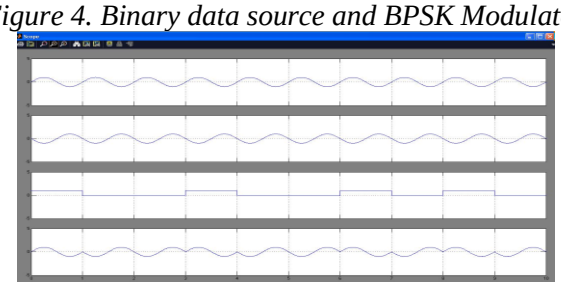

Figure 5. The waveforms on the scope
(a) Sine (b) –Sine (c) Modulating signal (d) Modulated signal

3.2 BPSK System in System Generator

System Generator is a digital signal processing design tool from Xilinx. Designs are made in the Simulink environment using a Xilinx specific block set. All implementation steps, including synthesis, place and route are automatically performed to generate an FPGA programming file.Our BPSK system implemented in System Generator has the same block as in fig.4: data source, a modulator, a channel. The main difference is the System Generator block which makes possible the administration of the Xilinx components.

The DDS Compiler Block is a direct digital synthesizer and it uses a lookup table scheme to generate sinusoids. A digital integrator generates a phase that is mapped by the lookup table into the output waveform. The mux block implements a multiplexer. It has one select input and a configurable number of data inputs that can be defined by the user. The d0 and d1 inputs of mux represent the sine waves.

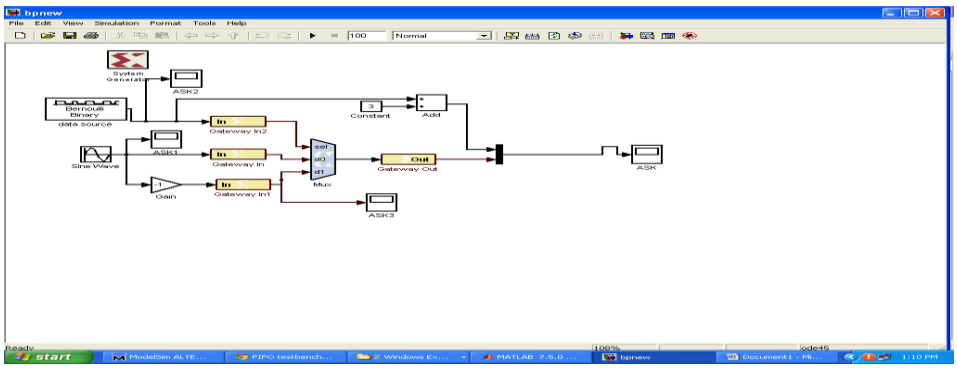

Figure 6. BPSK Modulator in System Generator.

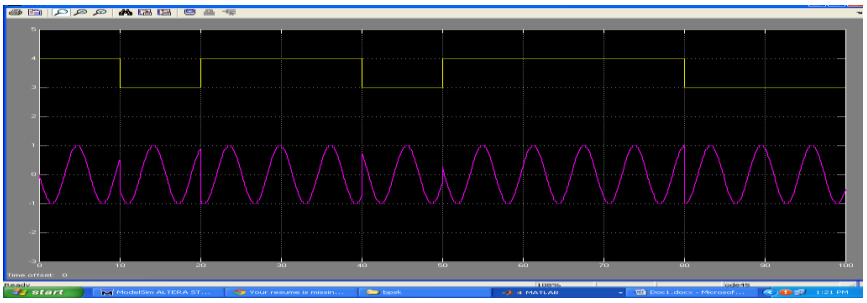

Fig 7: bpsk waveform

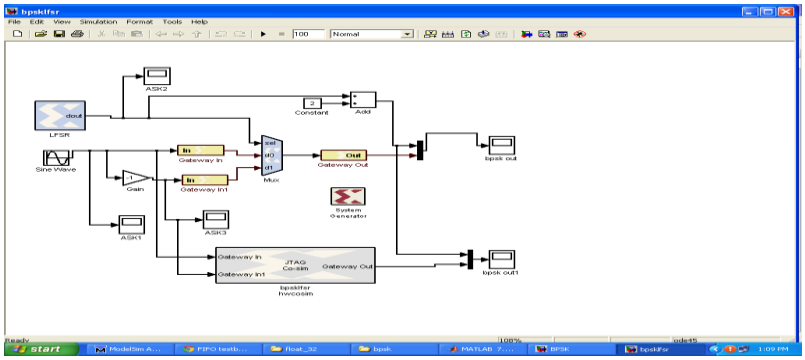

Figure 7(a) : A second implementation of the BPSK Modulator in System Generator.

Fig 8: 2nd implementation bpsk waveforms

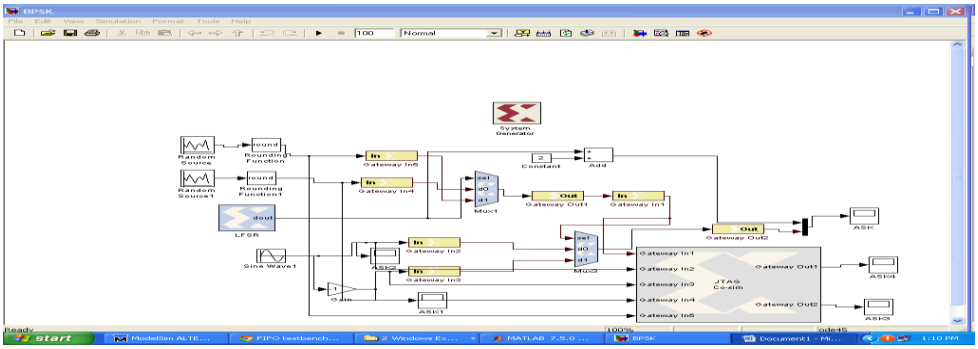

Figure 9 : A third implementation of the BPSK Modulator in System Generator.

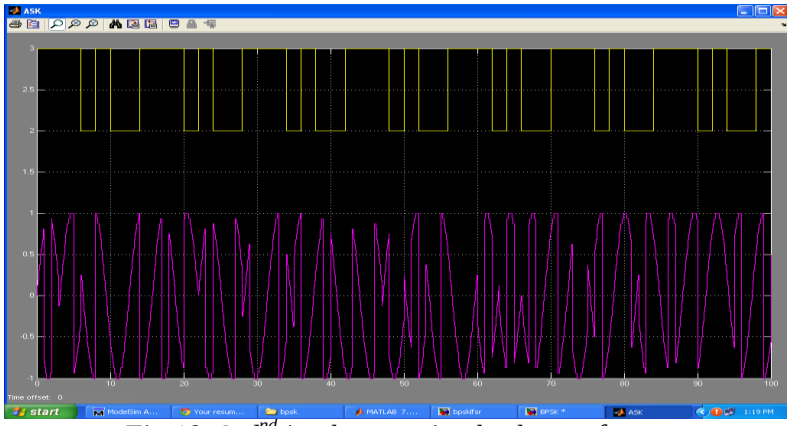

Fig 10: 3rd[nd] implementation bpsk waveforms

IV. BPSK SYSTEM ON THE SPARTAN 3E BOARD

The BPSK System Modulator is implemented on the Spartan 3E Starter Kit board is, exactly, the implementation in System Generator which is shown below. The carrier is generated internal, in a ROM

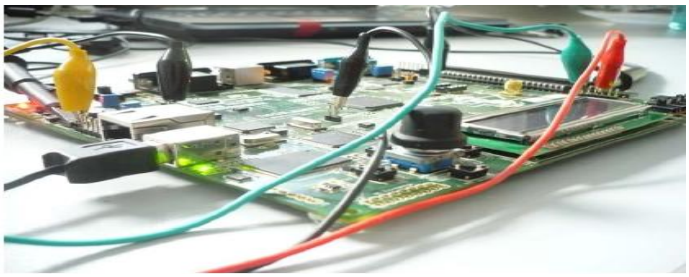

Figure 11. BPSK Modulator – experimental setup.

The modulating signal is generated internal, in the modulator, by a LFSR. The carrier is also generated internal, and is made of 16 different values kept in a ROM memory. The yielded carrier with 180º phase shift is obtained by reading the ROM memory later with 8 samples. If LFSR was '1', the modulated signal remained same as the carrier, but if '0' was transmitted, the modulated signal became the yielded carrier.
The principle of the BPSK modulator implemented on the FPGA is illustrated in fig.12.

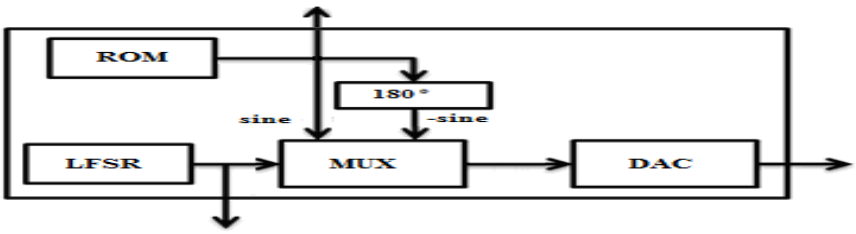

Figure 12. The principle of the BPSK modulator on the FPGA

V. RESULTS

Fig. 13 and illustrate the design summary of the modulator board. The design summary shows the various synthesizer options that were enabled and some device utilization and timing statistics for the synthesized design.

Design Summary:

Number of errors: 0

Number of warnings: 2

Device utilization summary

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	387	3840	10%
Number of 4 input LUTs	421	3840	10%
Number of occupied Slices	341	1920	18%
Number of Slices containing only related logic	347	347	100%
Number of Slices containing unrelated logic	0	347	0%
Total Number of 4 input LUTs	505	3840	13%
Number used as logic	421		
Number used as a route-thru	84		
Number of bonded IOBs	1	97	1%
Number of BUFGMUXs	4	8	50%
Number of RAMB16s	2	12	16%
Number of BSCANs	1	1	100%

VI. CONCLUSION

We proposed a implementation of the BPSK System (Modulator) in the Mat lab/Simulink environment**.** Then, we made a proposal of a BPSK System in System Generator. Both, the modulating signal and the carrier are generated internal, the modulating signal by a LFSR and the carrier by a DDS Compiler. The modulated signal is obtained at the output of a mux block and, then, passed through a communication channel where noise is added. The obtained signal is then added with all the multiplied samples from the carrier in a period. The operation takes place in the accumulator. Once we have a result, it is compared with a decision threshold.

Comparing the design summary obtained the logic utilization of the board was lower in terms of the slice flip-flops and LUTs used. All of these make the design suitable in terms of propagation, implementation and logic utilization of the Spartan 3E boards used in this work.

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