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9-Level Trinary DC Source Inverter Using Embedded Controller

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Abstract : *This paper presents the Trinary DC source H-bridge multilevel multilevel inverter. Embedded switching pattern scheme is used to improve the performance of Multilevel Inverter. This scheme reduces the switching loss. The proposed inverter can synthesize high quality output voltage near to sinusoidal waves. Unlike other schemes, the proposed firing method significantly reduces the Total Harmonic Distortion (THD) and switching losses. The circuit configuration is simple and easy to control.To validate the developed technique; simulations are carried out through MATLAB/SIMULINK.*

Keywords: *THD, Vrms, MLI, Embedded controller .*

I. INTRODUCTION

Multilevel inverters can be divided into three presentable topologies; diode-clamped, flying-capacitor, and cascaded H-bridge cell [1]-[5]. Among them, cascaded H-bridge multilevel inverters have been received a great attention because of their merits such as minimum number of components, reliability, and modularity. In the viewpoint of obtaining a sinusoidal output voltage wave, multilevel inverters may increase the number of output voltage levels. However, it will need more components resulted in complexity and cost increase. To minimize these drawbacks, multilevel inverters employing cascaded transformers have been studied [6]-[8]. Owing to the Trinary characteristic of output voltage, they can synthesize high quality output voltage near to sinusoidal waves. By using a cascaded transformer, they obtain galvanic isolation between source and loads. However, the transformer may decrease the power conversion efficiency, and volume and cost will be increased To alleviate these problems, we propose a cascaded H-bridge multilevel inverter using Trinary DC input source without transformers [6].To alleviate these problems, we propose a cascaded H-bridge multilevel inverter using trinary dc input source without transformers [6]. This circuit topology is simple and easy to control. The operational principle and key waveforms are illustrated in detail.This paper presents a single phase Trinary DC source nine level inverter topology for investigation with embedded controller switching technique. Simulations were performed using MATLAB-SIMULINK.

II. BASIC OPERATION OF MULTILEVEL INVERTER

Fig. 1 shows a circuit configuration of a cascaded H-bridge multilevel inverter employing Trinary DC input source. It looks like a traditional cascaded H-bridge multilevel inverter except input dc sources. By using Vdc and 3Vdc, it can synthesize nine output levels; -4Vdc, -3Vdc, -2Vdc, -Vdc, 0, Vdc, 2Vdc, 3Vdc, 4Vdc.The lower inverter generates a fundamental output voltage with three levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Here, the final output voltage levels becomes the sum of each terminal voltage of H-bridge, and it is given as

$$V_{out} = V_{HB1} + V_{HB2} \quad (1)$$

In the proposed circuit topology, if *n* number of H-bridge module has independent DC sources in sequence of the power of 3, an expected output voltage level is given as

$$V_n = 3^n, n = 1, 2, 3.. \quad (2)$$

TABLE. I
Switching Sequence of Trinary MLI

V_{out}	S11	S12	S13	S14	S21	S22	S23	S24
4Vdc	1	0	0	1	1	0	0	1
3Vdc	0	1	0	1	1	0	0	1
2Vdc	0	1	1	0	1	0	0	1
Vdc	1	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1
-Vdc	0	1	1	0	0	1	0	1
-2Vdc	1	0	0	1	0	1	1	0
-3Vdc	0	1	0	1	0	1	1	0
-4Vdc	0	1	1	0	0	1	1	0

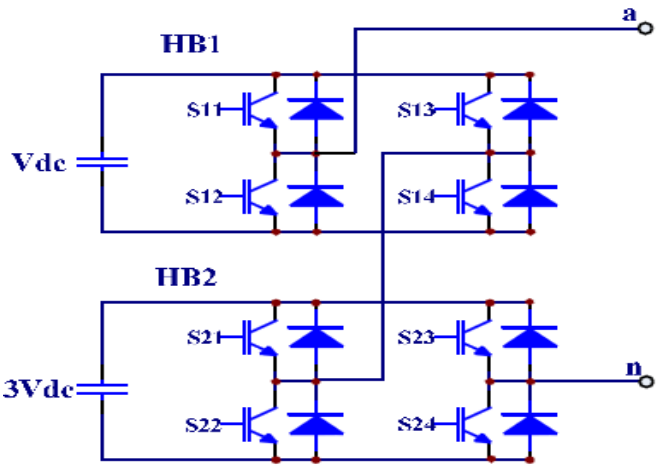

Fig. 1 Trinary DC source MLI.

It is compared with the conventional multilevel inverters, i.e., diode-clamped, flying capacitor, cascaded H-bridge, and cascaded transformer based multilevel inverter. In the case of diode-clamped, a large number of clamping diodes are a severe drawback. And a lot of balancing capacitors is a disadvantage of the flying capacitor method. Among them, the isolated CML looks very effective to synthesize output voltage levels. It only needs a single dc input source. However, it shows low efficiency because of adopting a cascaded transformer. And it will be suffered from large size and heavy weight. Moreover, this method is not desirable for the motor drives employing VF (variable frequency) control scheme because of the saturation of transformer.

III. SWITCHING SIGNAL GENERATION

Switching signal generation for proposed multilevel inverter is generated using embedded controller. Fig 2-9 shows the gating pattern generated using embedded controller.PWM signals are generated using embedded m-file, which significantly reduces the switching stress and it makes the system reliable.

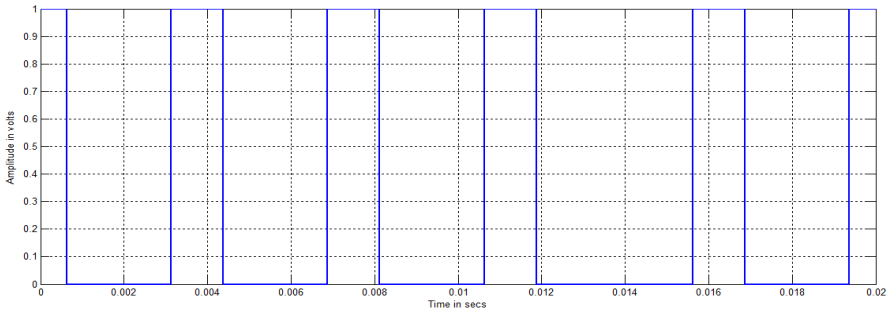

Fig 2: Gating pattern of Switch S11

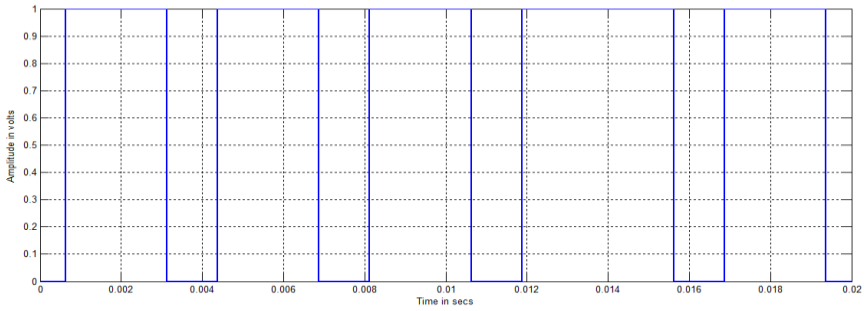

Fig 3: Gating pattern of Switch S12

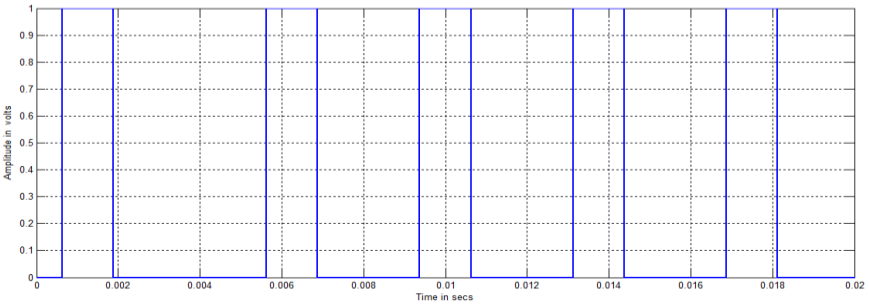

Fig 4: Gating pattern of Switch S13

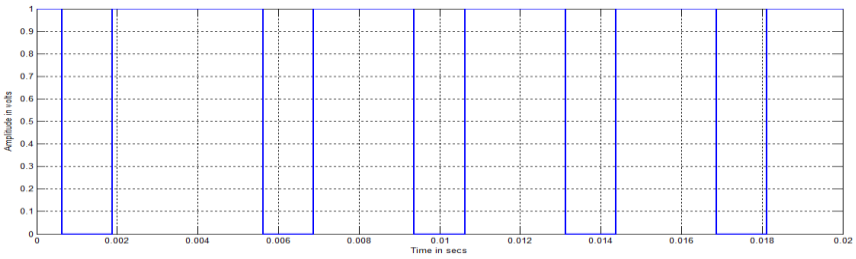

Fig 5: Gating pattern of Switch S14

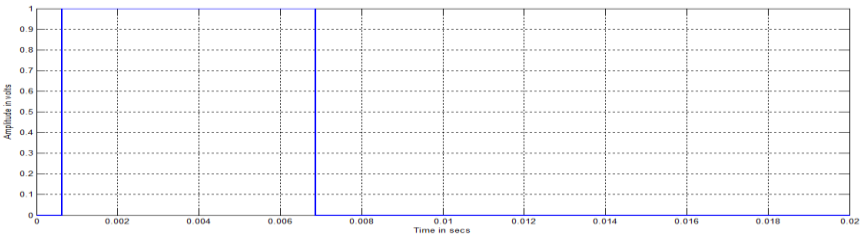

Fig 6: Gating pattern of Switch S21

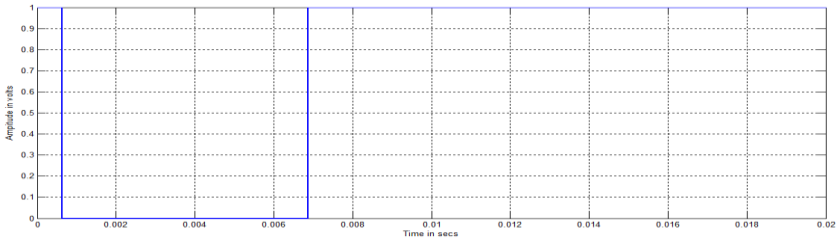

Fig 7: Gating pattern of SwitchS22

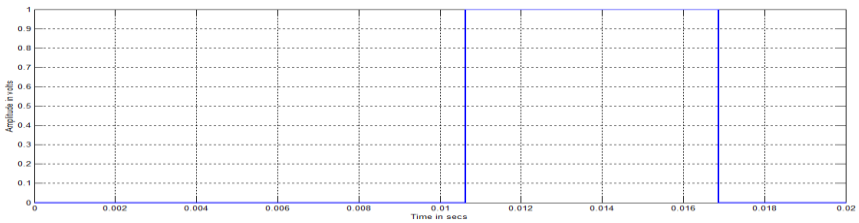

Fig 8: Gating pattern of Switch S23

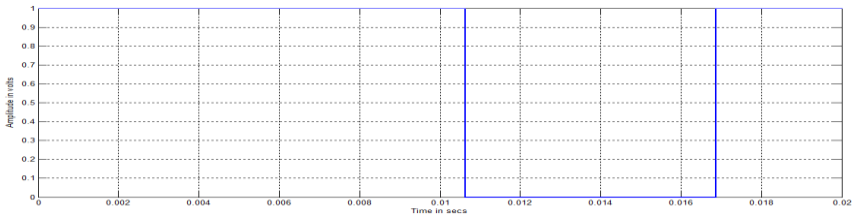

Fig 9: Gating pattern of Switch S24

IV. SIMULATIONS AND RESULTS

We are performed computer-aided simulations to prove availability of the proposed multilevel inverter. The simulations are implemented using Mat lab and it was considered to a pure resistive load. We can notice that the lower inverter generates a fundamental output voltage of three levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Consequently, the final output voltage becomes the sum of terminal voltage of H-bridge modules. Fig.13 shows the FFT plot for nine level inverter. We can notice that the lower inverter generates a fundamental output voltage of three levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Consequently the final output voltage becomes the sum of output voltage of upper and lower H bridge modules. The following parameter values are used for simulation: V_{dc} =25V, R (load) = 100 ohms

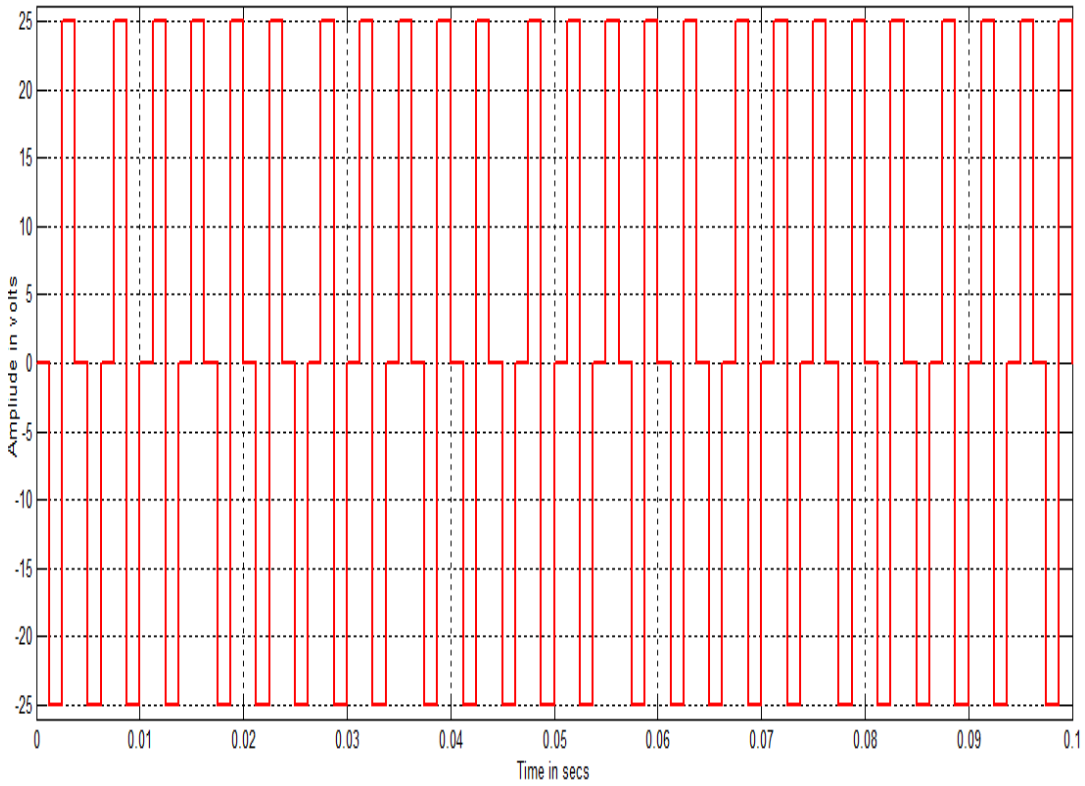

Fig 10: Upper inverter terminal voltage

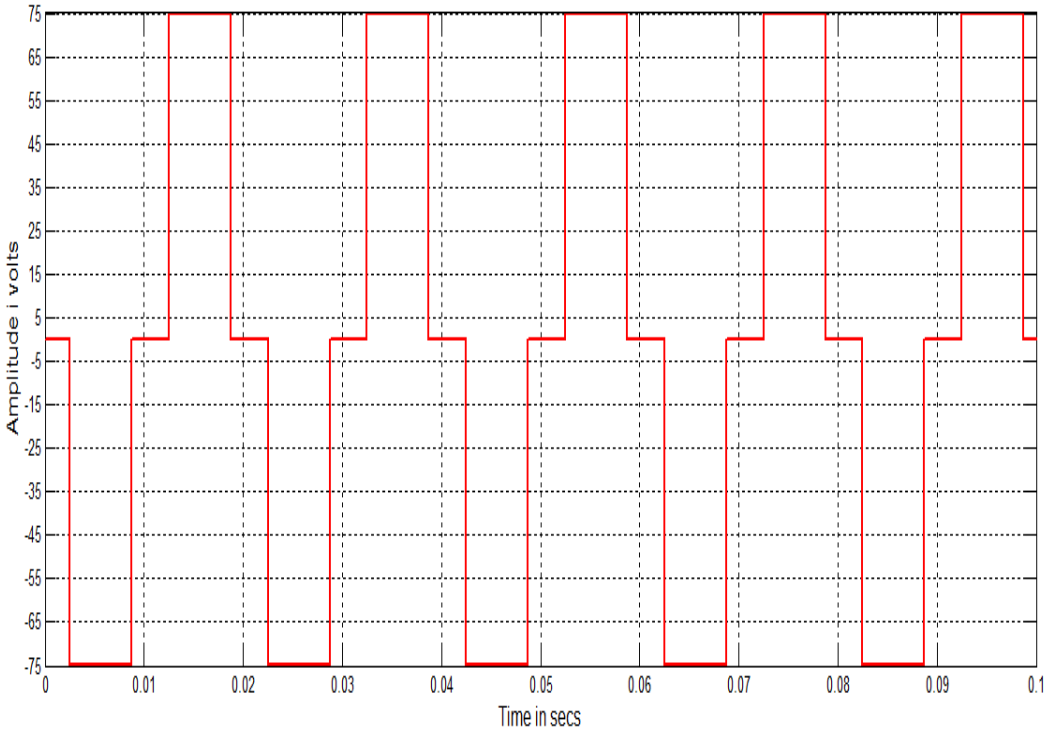

Fig 11: Lower inverter terminal voltage

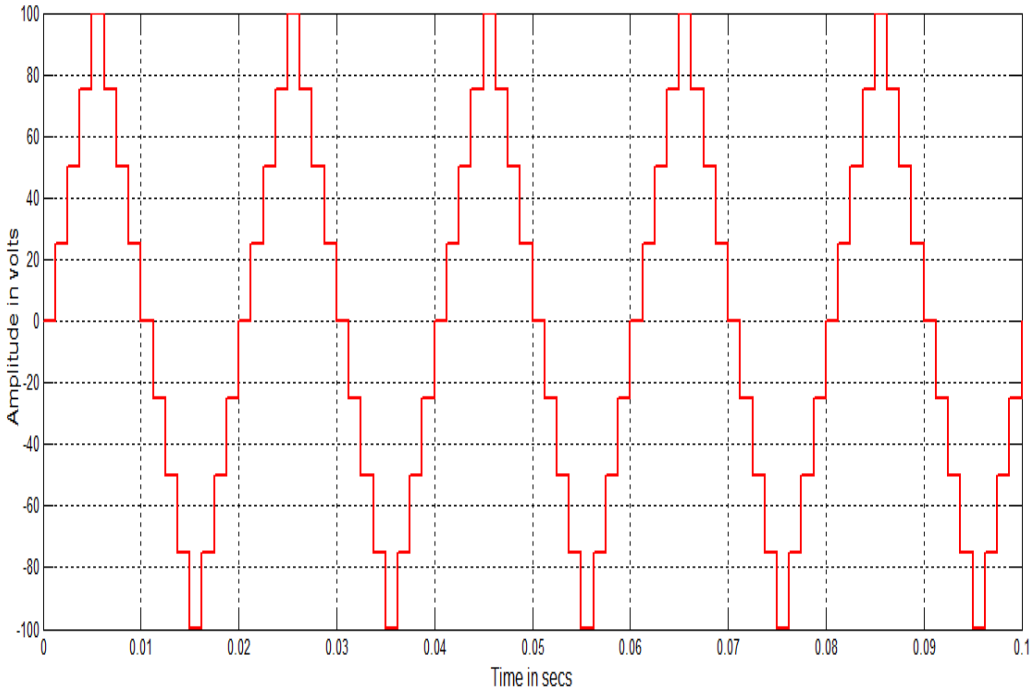

Fig 12: Nine level output voltage of Trinary MLI

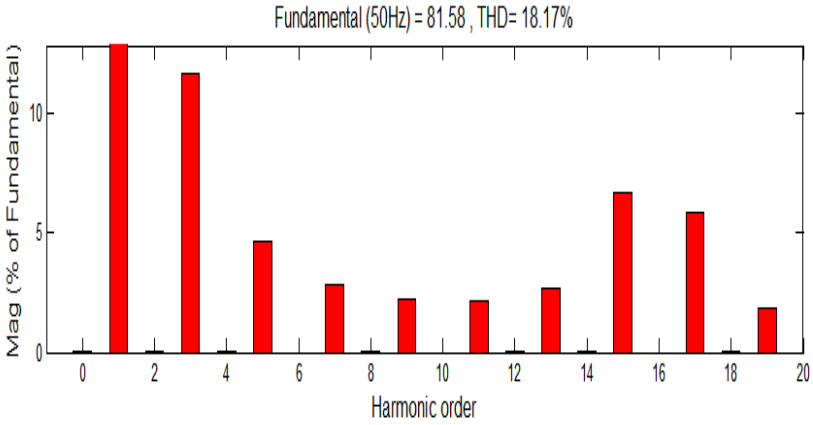

Fig 13: FFT plot for nine level output voltage

V. CONCLUSION

It proposed a cascaded H-bridge multilevel inverter employing Trinary DC sources to obtain a large number of output voltage levels with minimum devices. The proposed inverter can synthesize high quality output voltage near to sinusoidal waves. In this paper embedded switching scheme is employed and the advantage of using digital scheme is that it reduces the uneven degradation of power switches and switching losses. It is observed that proposed topology produce THD of 18.17% .This proposed system eliminates the complexity of generating gate signals when the stages are added.

Valuable and presentable merits of the proposed approach are summarized as

(1) Economical circuit configuration to produce multilevel outputs by using Trinary input sources,

(2) Easy to increase of the output voltage levels and output power owing to modularity characteristic,

(3) Little transition loss of switches due to low switching frequency and reduced EMI; it is suitable for high voltage applications.

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