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A Low Power Gain Boosted Fully Differential OTA for a 10bit pipelined ADC

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***Abstract* - Based on 0.18□ technology, a low power gain-boosted fully differential amplifier circuit is designed and used in the 10-bit, pipelined A/D converter which is supplied by 1.8 V power. In order to meet specifications, gain-boosting technique is used to improve the gain of OTA. The boosting amplifiers are two fully-differential op-amps which have a p-type or n-type input differential. At last, simulation results showed that 45dB loop gain and a phase margin of 180 ° have been achieved. The design is implemented using 180nm technology in Cadence software.**

Keywords- low-power; gain boosting; OTA

I. INTRODUCTION

Designing high-gain and high-speed operational amplifier is becoming increasingly challenging. [1][2]The main bottleneck is that there is a tradeoff between speed and gain, because high dc gain demands a multistage design with long-channel devices, a low bias current levels; whereas the high-speed demands single stage design, short-channel devices, a high bias current levels. But there have been several approaches to resolve this conflict, gain-boosting technique is one of these approaches to solve this problem in the condition that the auxiliary amplifier is designed reasonably, otherwise, the introduction of zero-pole deteriorate settling performances of operational amplifier, even though it does not noticeably affect the frequency response.

An OTA is basically an op-amp without any output buffer, preventing it from driving resistive or large capacitive loads. They are preferred over op-amps mainly because of their smaller size and simplicity. The OTA is based on a differential amplifier at the input. If the inputs are equal, the transistors in the differential pair conduct equal currents. When the inputs change, the current changes through the pair. The purpose of an OTA is to generate a current proportional to an input voltage difference. This paper is concerned with the design of a fully differential OTA, meaning there are two outputs. The difference in the output currents should be proportional to the difference in the input voltages.

In this paper a Gain boosted fully differential OTA is proposed to satisfy the requirement for high-speed applications. The proposed OTA has a N gain boost and P gain boost auxiliary amplifiers. This auxiliary amplifier boosts the gain of the main amplifier structure.

II. CIRCUIT ANALYZE

A. OTA STRUCTURE

Compared with single ended output operational amplifier, fully differential amplifier employs two-stage topology, which has a lot of advantages for example no influence of common mode noise, more high linearity and reducing even harmonics. So we employ the two-stage fully differential OTA structure as shown in Figure 1.

The OTA structure uses gain boosted auxiliary amplifier which ensures the main op-amp to achieve specifications required. Gain boost amplifiers that is P gain boost and N gain boost are also fully differential structures. The auxiliary gain boosted amplifiers in this design are shown in Figure 3, Figure 4.

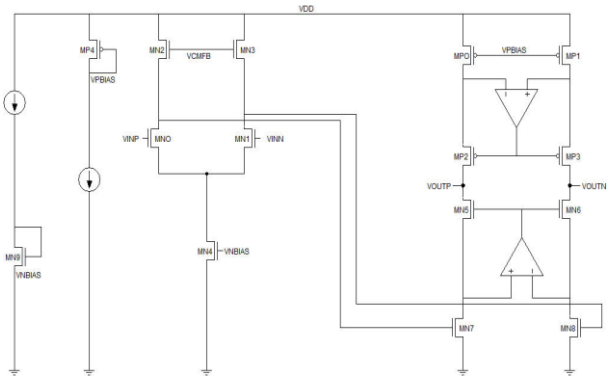

Fig.1 Circuit of gain boosted fully differential OTA

B. GAIN BOOSTING MODEL

Gain-boosting technology allows to make op-amp's output impedance get multiplied approximately by A_{add} (A_{add} is the gain of auxiliary amplifiers), thus the overall gain is increased, this technology has been widely used in designing of high gain operational amplifier under low voltage. However, if the auxiliary amplifier is designed unreasonably, However, if the auxiliary amplifier is designed unreasonably, it will introduce a pole-zero doublet, the existence of pole-zero doublet will sluggish signal settling, which degrade performance of whole S/H module seriously [3][4].

Fig.2 Illustrates the model of the gain-boosted amplifier [5]. M1 and M2 form the main cascode amplifier. A is a gain-boosted amplifier. A drives the gate of M2 and forces the voltage at the drain of M1 and Vref to be equal. Because of the gain-boosted amplifier, voltage variations at the output will affect the voltage at the drain of M1 to a lesser extent variations [6].

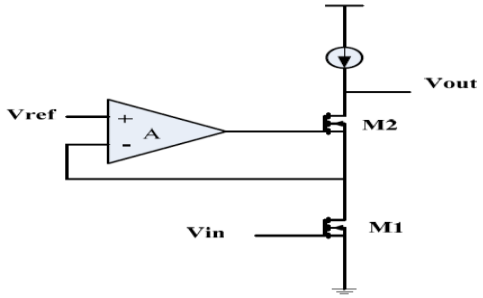

Fig.2 The model of Gain boosted amplifier

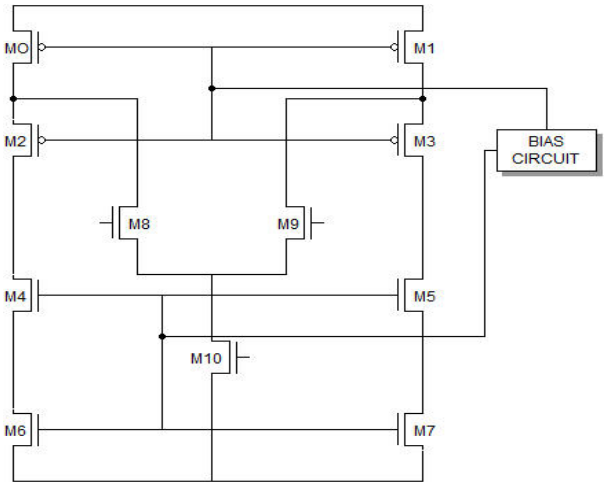

Fig.3 N gain boost amplifier

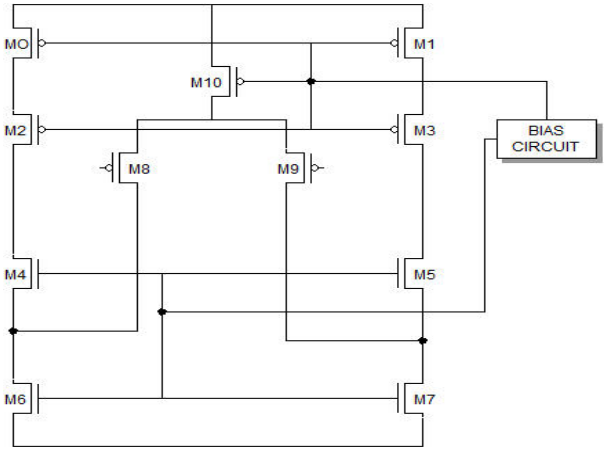

Fig.4 P gain boost amplifier

III. DESIGN PROCEDURE

For a supply voltage of 1.8V Firstly, we simulated the gain-boosted circuit in order to verify whether it meet to the specifications. An initial power budget was allotted, which gives total biasing current. This is the total current from rail to rail which should be divided through branches. Generally, the overdrive of PMOS should be higher than NMOS as mobility of PMOS is approx. 2.5 times less than NMOS. Based upon this we assigned overdrive voltages for all devices.

Initial W/L values (in um) can be chosen by using the current expression in saturation region operation. We assumed $\mu_n * C_{ox} = 150\ uA/V^2$ and $\mu_p * C_{ox} = 60\ uA/V^2$ for first iteration. The saturation region current expression helps us in calculating the aspect ratios (W/L) of transistors as the current through them is known and overdrive voltage is assigned.

$$I_d = \frac{\mu n C_{ox}}{2}\left(\frac{W}{L}\right)[Vgs - Vt]^2 \qquad (1)$$

Here I_d is the biasing current, μ and C_{ox} are process parameters, W/L is aspect ratio of a transistor, Vgs is gate-source voltage and V_T is threshold voltage of device. The circuits were simulated in a 0.18um CMOS technology with Cadence.

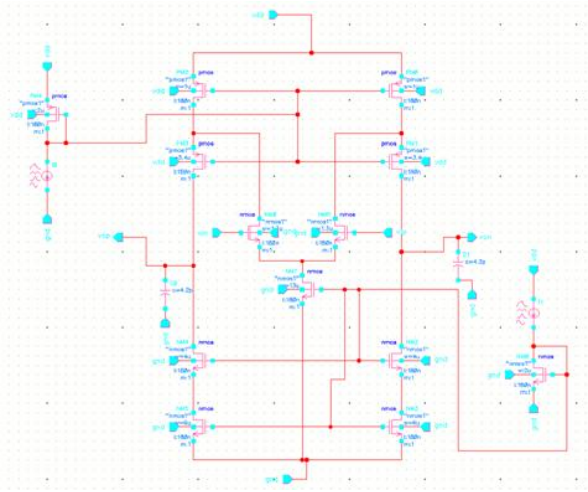

Fig.5 Schematic of N Gain Boost Amplifier

Fig.5 shows the simulated circuit diagram of the N gain boost amplifier in Cadence. The load capacitors were chosen to have values of 4.2pF each.

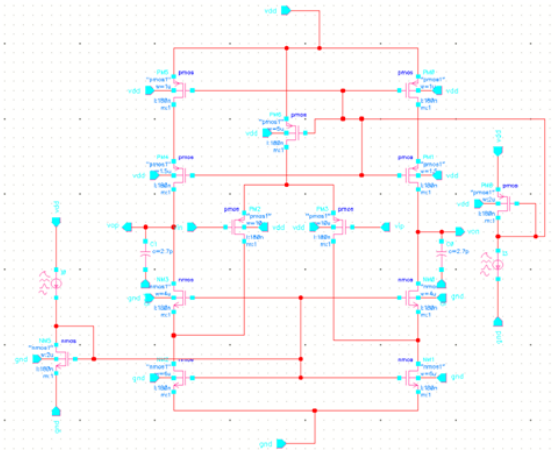

Fig.6 Schematic of P Gain Boost Amplifier

Fig.6 shows the simulated circuit diagram of the P gain boost amplifier in cadence. The load capacitors were chosen to have values of 2.7 pF each.

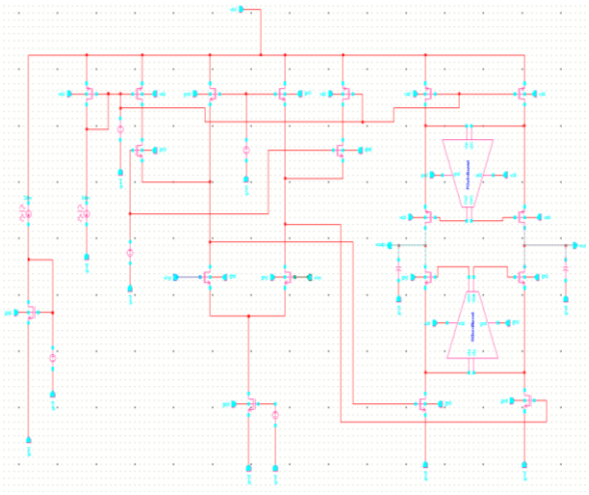

Fig.7 Schematic of Main Amplifier

Fig.7 shows the simulated circuit diagram of the main amplifier. The load capacitors were chosen to have values of 2.3 pF each.

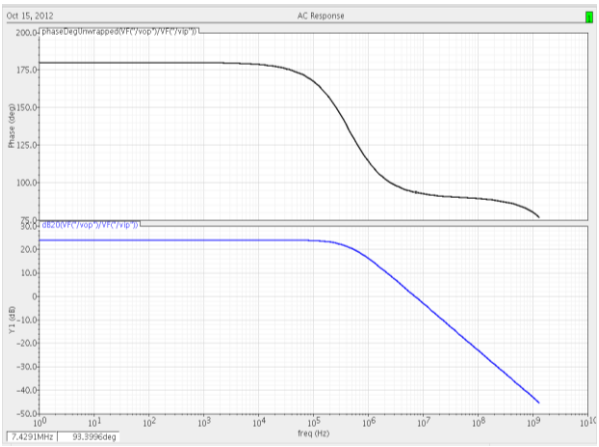

Fig.8 Frequency characteristics of N gain boosted

Fig.8 and Fig.9 shows the Frequency characteristics of the auxiliary amplifiers with 10us time. It shows the dc gain of 24dB and 15dB respectively.

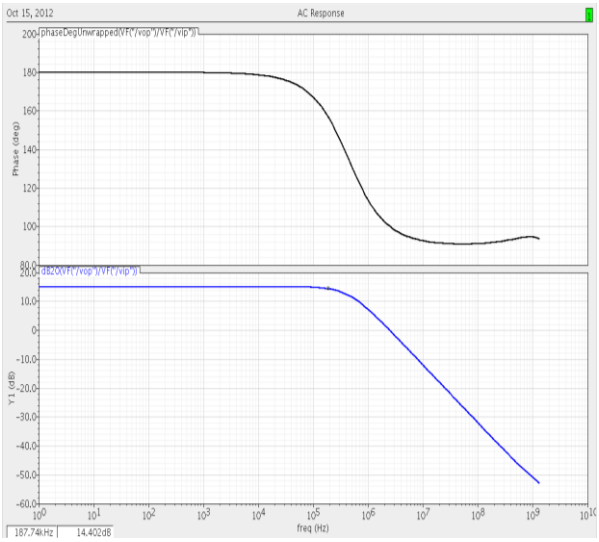

Fig.9. Frequency characteristics of P gain boosted

Fig.10 shows the frequency characteristics of the main amplifier with 10us time. It shows the dc gain of 45dB.

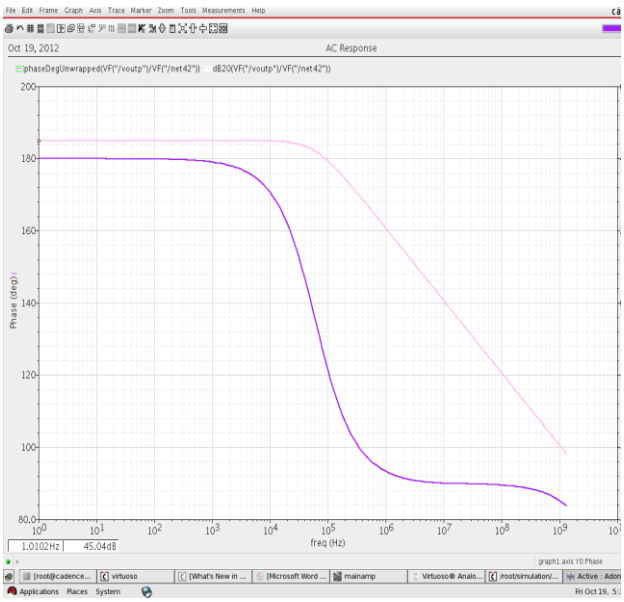

Fig.10 Frequency characteristics of main amplifier

IV. CONCLUSION

A Gain boosted fully differential OTA has been designed. The result of schematic simulation is setting out below: gain up to 45 dB, with the power supply of 1.8V, the power consumption is 1.64mW. Table 1 shows the performance summary of the OTA. This OTA is used in a 10 bit 50 MSPS SHA-Less ADC which uses both capacitor sharing and op-amp sharing techniques for power reduction.

TABLE.1 : Performance summary of the OTA

Power Supply	1.8v
Technology	180 nm Technology
DC gain (Main Amplifier)	45 dB

DC gain (N gain boost)	24 dB
DC gain (P gain boost)	15 dB
Phase	180^0
Power Consumption(Main amplifier)	1.64mW
Power consumption(N Gain boost amplifier)	$7.049X10^{-4}W$
Power consumption(P Gain boost amplifier)	$7.26X10^{-4}W$

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