

### A Grid Connected Hybrid Asymmetrical Nine level Inverter Topology Using Boost Converter

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### ABSTRACT

This paper presents the distributed energy re-source (DER)-based single-phase inverter is usually adopted. In order to reduce conversion losses, the key is to save costs and size by removing any kind of transformer as well as reducing the power devices. This paper deals nine-level multi-string inverter topology for DERs-based dc/ac conversion system. Multilevel inverter (MLI) is a new breed of power converter that is suited for higher power applications. The various topologies of MLI are diode-clamped, capacitor clamped and cascaded H-bridge. This paper focuses on cascaded MLI using two unequal dc sources in order to produce nine-level output. In this study, a high step-up converter is introduced as a front-end stage to improve the conversion efficiency of conventional boost converters and to stabilize the output dc voltage of various DERs such as photovoltaic and fuel cell modules for use with the simplified MLI. The simplified MLI requires only eight active switches instead of the sixteen required in the conventional cascaded H-bridge MLI. This MLI offers strong advantages such as improved output waveforms, smaller filter size, and lower electromagnetic interference and total harmonics distortion. Simulation results show the effectiveness of the proposed solution.

KEYWORDS: Cascaded H Bridge inverter, Fuel Cell, High step-up converter, PV Array, THD.

### I. INTRODUCTION

For delivering premium electric power in terms of high efficiency, reliability, and power quality, integrating interface converters of DERs such as photovoltaic (PV), wind power, microturbines, and fuel cells into the micro grid system has be- come a critical issue in recent years In such systems, most DERs usually supply a dc voltage that varies in a wide range according to various load conditions. In light of public concern about global warming and climate change, much effort has been focused on the development of environmentally friendly distributed energy resources (DERs). Thus, a dc/ac power processing interface is required and is compliable with residential, industrial, and utility grid standards Multilevel inverters can be divided into three presentable topologies; diode-clamped, flying-capacitor, and cascaded H- bridge cell [1]-[5]. Among them, cascaded H-bridge multilevel inverters have been received a great attention because of their merits such as minimum number of components, reliability, and modularity. In the viewpoint of obtaining a sinusoidal output voltage multilevel inverters may increase the number of output voltage levels. However, it will need more components resulted in complexity and cost increase. To minimize these drawbacks, multilevel inverters employing cascaded transformers have been studied Owing to the trinary characteristic of output voltage, they can synthesize high quality output voltage near to sinusoidal waves. By using a cascaded transformer, they obtain galvanic isolation between source and loads. However, the transformer may decrease the power conversion efficiency, and volume and cost will be increased. To alleviate these problems,

propose a cascaded H- bridge multilevel inverter using trinary dc input source without transformers [6].

### II. PV ARRAY

Photons of light with energy higher than the bandgap energy of PV material can make electrons in the material break free from atoms that hold them and create hole- electron pairs. These electrons however, will soon fall back into holes causing charge carriers to disappear. If a nearby electric field is provided, those in the conduction band can be continuously swept away from holes toward a metallic contact where they will emerge as an electric current. The electric field with in the semiconductor itself at the junction between two regions of crystals of different type, called a p-n junction. The PV cell has electrical contacts on its top and bottom to capture the electrons. When the PV cell delivers power to the load, the electrons flow out of the n-side into the connecting wire, through the load, and back to the p-side where they recombine with holes [4]. Note that conventional current flows in the opposite direction from electrons.

### 2.1 MATHEMATICAL MODEL OF THE PV ARRAY

## 2.1.1. SIMPLIFIED EQUIVALENT CIRCUIT:

A solar cell basically is a p-n semiconductor junction. When exposed to light, a current proportional to solar



irradiance is generated. The circuit model of PV cell is illustrated in Fig.1. Standard simulation tools utilize the approximate diode equivalent circuit shown in Fig. 1 in order to simulate all electric circuits that contain diodes. The model is based on two-segment piecewise linear approximation. The circuit consists of  $R_{OII}$  in series with voltage source  $V_{OII}$ .



Fig. 1: Circuit model of PV solar cell

### 2.2. THEORETICAL MATHEMATICAL MODEL

The equation [1] & [2] that are used to solve the mathematical model of the solar cell based on simple equivalent circuit shown in Fig. 1, are given below;

Where:

I is the cell current in (A). q is the charge of electron = 1.6x10-19 (coul). K is the Boltzmann constant (j/K). T is the cell temperature (K). IL is the light generated current (A). Io is the diode saturation current. Rs , Rsh are cell series and shunt resistance (ohms). V is the cell output voltage (V).

#### **2.3. PV CHARACTERISTICS**

# 2.3.1 CURRENT VS VOLTAGE CHARACTERISTICS:

Equation (1) was used in computer simulation to obtain

the output characteristics of a solar cell, as shown in the figure4. This curve clearly shows that the output characteristics of a solar cell are non linear and are crucially influenced by solar radiation, temperature and load condition

## 2.3.2 VARIATION IN AVAILABLE ENERGY DUE TO SUN'S INCIDENT ANGLE:

PV cell output with respect to sun's angle of incidence is approximated by a cosines function at sun angles from  $0^{\circ}$  to  $50^{\circ}$ . Beyond the incident angle of  $50^{\circ}$  the available solar energy falls of rapidly as shown in the figure 1. Therefore it is convenient and sufficient within the normal operating range to model the fluctuations in photocurrent (Iph) verses incident angle is given by Eq(3).



Fig. 2: Output Characteristics Of Solar Cell

**2.3.2 POWER VS VOLTAGE CHARACTERISTICS:** Figure 3 shows the typical Power versus Voltage curve of the PV array. In this figure, P is the power extracted from PV array and V is the voltage across the terminals of the PV array.

The characteristics have different slopes at various points. When maximum power is extracted from PV array the system is operating at MPP where slope is zero. The PV curve varies according to the current insulation and temperature. When insulation increases, the power available from PV array increases whereas when temperature increases, the power available from PV Array decreases.



Fig 3: Power Vs Voltage

The graph shown in fig.4 is used to find the maximum power extracted from the sun when the PV arrays are inclined a different angles. From the figure we observe that Max power is obtained when the slope of the PV array is equal to zero.



Fig. 4: Variation In Available Energy Due Sun's Incident Angle Variation.

### III. FUEL CELL 3.1 PROTON EXCHANGE MEMBRANE (PEM) FUEL CELL

There are different fuel cell technologies that have been successfully used. Among others, the polymer electrolyte (PE) fuel cell, also named proton exchange membrane (PEM) fuel cell, can be considered a good alternative for the use aboard of electric vehicles in which simplicity, high specific power and rapid start-up at different temperatures have a significative importance [7].



**Figure 5**. Structure of a PEM fuel cell. (a) Bipolar plate; (b) Gas flow channel; (c) Electrode layer; (d) Catalyst layer and (e) polymer layer.

RT

A PEM fuel cell is constituted by a stack with a central membrane able to conduct protons. The external layers work as two electrodes. The set of layers is pressed by two conductive plates containing some channels in which the reactants flow.

A basic diagram showing the estructure of the cell is shown in Fig. 5. The main elements inside the cell are: conductor plates, electrodes and membrane. The electrodes are composed by a gas diffusion layer and a catalyst layer. Both layers have a porous, partially hydrophobic, structure.

Air is fed to the cathodic layer, and hydrogen is fed to the anodic one. The central membrane works as a

electrolyte that performs both the functions of transferring  $\mathbf{H}^+$  from the anode to the cathode and reactant separation.

The electrochemical reactions involved are summarized below,

$$H_2 \rightarrow 2H^+ + 2e^-$$
$$2H^+ + \frac{1}{2}O_2 + 2e^- \rightarrow H_2O$$
$$H_2 + \frac{1}{2}O_2 \rightarrow H_2O$$
(5)

Ec. (1) describes the chemical reaction at the anode. The electrons are transferred to the platinum layer and protons to the central membrane. Ec. (5) shows what happens at the cathode. The oxygen reacts with the protons coming from the membrane and with the electrons fed by the catalyst. The result is water. Finally ec. (5) shows the overall reaction.

### 3. Circuit model of PEM fuel cell

A typical PEM fuel cell has a V-I characteristic at room temperature and normal air pressure like the characteristic shown in Fig. 6. There are some factors that produces losses (voltage drop) in a fuel cell. Such losses will cause the cell voltage to be less than its ideal potencial. There are three main sources of losses:

- 1) Activation polarization.
- 2) Ohmic polarization.
- 3) Concentration polarization.

The output voltage of the PEM fuel cell is defined by the following equation [6], [7],

$$E = N \left( E_0 + \frac{RT}{nF} \ln \left\{ \frac{P_{H_2} (\frac{P_{O_2}}{P_{std}})^{1/2}}{P_{H_2O_c}} \right\} - L \right) \dots (7)$$

where

- E Stack output voltage
- N Number of cells in stack.
- *E*<sub>0</sub> Cell open circuit voltage at standard pressure.
- nF The Tafel slope [8], usually in the range from

0.03 to 0.12 V for 24 ° C. R is the universal

gas constant, F is Faraday's constant, T is the operating temperature and n=2 is the number of transferred electrons in the electrochemical reaction defined by ec. 1.

- $PH_2$  Partial pressure of hydrogen inside the cell.
- PO2 Partial pressure of oxygen inside the cell.
- PH2 Oc Partial pressure of gas water.
- *Pstd* Standard pressure.
- L Voltage losses.

The PEM fuel cell 's voltage losses L have the following contributions:

- Activation losses. Due to the slowness of the reactions taking place inside the cell. This term can be reduced by maximizing the catalyst contact area for reactions.
- Internal current losses. Due to the leakage of electrons that pass through the membrane to the cathode side instead of flowing through the electric
- Resistive losses. Due to the current flow through the resistance of the whole electrical circuit including the membrane and the interconnections. This term can be reduced if the membrane is well hydrated.
- Mass transport or concentration losses. Due to gas concentration changes at the surface of the electrodes.

$$L = \frac{RT}{\alpha nF} \ln\left(\frac{i+i_n}{i_0}\right) + r(i+i_n) - \frac{RT}{nF} \ln\left(1 - \frac{i+i_n}{i_L}\right)$$
......(8)

Where

- *i* Output current density.
- *in* Internal current density related to internal current losses.
- *i*0 Exchange current density related to activation losses.
- *il* Limiting current density related to concentration losses.
- *r* Area specific resistance related to resistive losses.

Fig.8 also shows the regions and the qualitative result of each one of the causes of losses.

Cell voltage (V)



Current density

Figure 8. V-I characteristic of a single PEM fuel cell.

The V-I characteristic shown in fig.8 can be modeled using the equivalent circuit shown in fig.9.



Figure 9. Equivalent circuit of the PEM fuel cell [6].

### **IV. HIGH STEP UP BOOST CONVERTER**

In this study, high step-up converter topology in [26] is introduced to boost and stabilize the output dc voltage of various DERs such as PV and fuel cell modules for employment of the proposed simplified multilevel inverter. The architecture of a high step-up converter initially introduced from depicted in Fig. 10, and is composed of different converter topologies: boost, flyback, and a charge circuit.

The coupled inductor of the high step-up converter can be modeled as an ideal transformer, a magnetizing inductor, and a leaky inductor.

According to the voltage–seconds balance condition of the magnetizing inductor, the voltage of the primary winding can be derived as

$$v_{pri} = v_{in} \cdot \frac{D}{(1-D)} \qquad \dots \dots \dots (9)$$

where *Vin* represents each the low-voltage DC energy input sources, and voltage of the secondary winding is

$$v_{sec} = \frac{N_s}{N_P} \cdot v_{pri} = \frac{N_s}{N_P} \cdot v_{in} \cdot \frac{D}{(1-D)}$$
 .....(10)

Similar to that of the Boost converter, the voltage of the charge-pump capacitor C  $_{pump}$  and clamp capacitor C  $_{c}$  can be expressed as

$$v_{c_p} = v_{c_c} = v_{in} \cdot \frac{D}{(1-D)}$$
 .....(11)

Hence, the voltage conversion ratio of the high step-up converter, named input voltage to bus voltage ratio, can be derived as

### V. PROPOSED MULTILEVEL INVERTER

Fig. 10 shows a circuit configuration of a cascaded H-bridge multilevel inverter employing trinary dc input source. It lookslike a traditional cascaded H-bridge multilevel inverter except input dc sources. By using  $V_{dc}$  and  $3V_{dc}$ , it can synthesize nine output levels; -4Vdc, -3Vdc, -2Vdc, -Vdc, 0, Vdc, 2Vdc, 3Vdc, 4Vdc.

Fig. 11 shows a basic idea to generate output voltage levels. The lower inverter generates a fundamental output voltages with three level, and then upeer interval adds or subtracts. one level from the fundamental wave to synthesize stepped waves. Here, the final output voltage levels becomes the sum of each terminal voltage of H-bridge, and it is given as

The switching frequency of  $v_y$  is lower than that of  $v_x$ . It is an effective approach in the viewpoint of efficiency because most power will be transferred via the lower inverter which has the output voltage  $v_y$ .



Fig. 10. Configuration of cascaded H-bridge multilevel inverter employing trinary dc sources.

In the proposed circuit topology, if n number of Hbridge module has independent dc sources in sequence of the power of 3, an expected output voltage level is given as

$$V_n = 3^n, n = 1, 2, 3, \cdots$$

Switching functions of the upper H-bridge inverter (SFB1) and the lower H-bridge inverter (SFB2) are expressed in (12) and (13), respectively.

$$if (S_{x1}, S_{x4}) = on \quad then \quad S_{FB1} = 1$$
  

$$if (S_{x1}, S_{x3}) or (S_{x2}, S_{x4}) = on \quad then \quad S_{FB1} = 0$$
  

$$if (S_{x2}, S_{x3}) = on \quad then \quad S_{FB1} = -1$$
  

$$if (S_{x2}, S_{x3}) = on \quad then \quad S_{FB1} = -1$$

$$if (S_{y1}, S_{y3}) or (S_{y2}, S_{y4}) = on \quad then \quad S_{FB2} = 0$$
  
$$if (S_{y2}, S_{y3}) = on \quad then \quad S_{FB2} = -1$$

Therefore, the output voltage is given as

$$v_{out} = \sum_{n=1}^{\infty} 3^{n-1} \cdot S_{FBn} \cdot V_{dc}$$

.....(14)

In (5), n means the number of H-bridge module. When it employs two H-bridge modules as shown in Fig. 1, the output voltage is expressed a

IOSR





Fig. 11. Operational waveform to synthesize nine output voltage levels.

In the case of *SFB2*, which is the switching function of the lower inverter, it takes a naught when a desired output level is equivalent or lower than  $V_{dc}$  level. In contrast, it takes a unity when an expected output voltage level is higher than  $V_{dc}$ . For a positive level, the switching function *SFB2* can be expressed by using C-language as (Here, all variables are an integer (int)









### VII. SIMULATIONS RESULTS

At first, we are performed computer-aided simulations to prove availability of the proposed multilevel inverter. The simulation was implemented by using PSIM. And it was considered to a pure resistive load. Fig. 4 shows simulation waveforms of a reference voltage, output voltage  $(v_{Out})$ , terminal voltages of the upper  $(v_x)$  and the lower  $(v_y)$  inverter in sequence. We can notice that the lower inverter generates a fundamental output voltage of three levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Consequently, the final output voltage becomes the sum of terminal voltage of H- bridge modules.

Based on the simulation results, the proposed multilevel inverter was tested by a prototype. As a

### controller, AVR MEGA 128 was used.





FIG.14 SIMULATION CIRCUIT



FIG 15. Nine level output



FIG16. Pulse sequence



Fig. 17 Simulation waveforms of a reference voltage, output voltage  $(v_{OUt})$ , output voltages of the upper inverter  $(v_x)$  and the lower inverter  $(v_y)$ .







Fig. 18. Experimental waveforms of output voltage (*vout*), terminal voltages of the upper inverter ( $v_x$ ) and the lower inverter ( $v_y$ ))

Fig18 shows experimental waveforms of output voltage  $(v_{out})$ , terminal voltages of the upper  $(v_x)$  and the lower  $(v_y)$  inverter in sequence. The output voltage has nine levels including zero level. Although it is close to a sinusoidal wave, it has lower order harmonics. So it needs more H-bridge modules or output filter to obtain high quality output voltages.

Components comparison between conventional inverters and the proposed approach appearing 9 output levels is given in Table I. It is compared with the conventional multilevel inverters, i.e., diode-clamped, flying capacitor, cascaded H- bridge, and cascaded transformer based multilevel inverter. In the case of diode-clamped, a large number of clamping diodes are a severe drawback. And a lot of balancing capacitors is a disadvantage of the flying capacitor method. Among them, the isolated CML looks very effective to synthesize output voltage levels. It only needs a single dc input source. However, it shows low

Efficiency because of adopting a cascaded transformer. And it will be suffered from large size and heavy weight. Moreover, this method is not desirable for the motor drives employing VF (variable frequency) control scheme because of the saturation of transformer.

From the comparison, it is clear that the most outstanding advantage of the proposed multilevel inverter scheme is the elimination of transformer in the main power stage. However, each cell of the proposed multilevel inverter requires its own isolated power supply. The provision of these isolated supplies is the main limitation in the power electronic circuit design. So the proposed multilevel inverter is suitable for photovoltaic power generating systems equipped with distributed power sources.

#### **IV.CONCLUSION**

It proposed a cascaded H-bridge multilevel inverter employing trinary dc sources to obtain a large number of output voltage levels with minimum devices. The proposed inverter can synthesize high quality output voltage near to sinusoidal waves. The circuit configuration is simple and easy to control. The proposed prototype consists of two dc sources with the use of eight switches instead of 16 switches for conventional H bridge inverter to get required nine level output voltage and to reduce the harmonics. The main disadvantage of conventional H bridge inverter is input voltage is fixed to over this problem, in the proposed prototype boost converter is used to regulate and to obtain the desired input voltage and further the DC source is replaced by a renewable resource such as solar panels, fuel cell to get DC voltage to grid connected system The desired operational principle and key waveforms are illustrated and analyzed.

Valuable and presentable merits of the proposed approach are summarized as

- (1) Economical circuit configuration to produce multilevel outputs by using trinary input sources,
- (2) Easy to increase of the output voltage levels and output power owing to modularity characteristic,
- (3) Little transition loss of switches due to low switching frequency and reduced EMI; it is suitable for high voltage applications



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