

# High Speed Current Mode Sense Amplifier for SRAM Applications

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## ABSTRACT

The sense amplifier is one of the most important components of semiconductor memories used to sense stored data. This plays an important role to reduce the overall sensing delay and voltage. Earlier voltage mode sense amplifiers are used to sense the data it sense the voltage difference at bit and bitb lines but as the memory size increase the bit line and data line capacitances increases. As a result large time is required by capacitance to discharge so sensing delay and power dissipation increase. Used that sense the current directly from bit and bitb lines and reduce the sensing delay. This technique is used in current mode sense amplifiers. This thesis work explores the design and analysis of current mode sense amplifier using Tanner tool (14.0) version. The simulation is carried out at 1.5V / 0.13um technology using tanner (14.0 Version) tool. The results are verified with the existing results at 1.8V / 0.18um CMOS technology.

**Keywords-** Minimum delay, current sensing, low voltage, current-mode sense amplifier.

## 1. INTRODUCTION

Sense amplifiers are used to translate small differential voltage to a full logic signal that can be further used by digital logic. The need for increased memory capacity, higher speed, and lower power consumption has defined a new operating environment for future sense amplifiers. Sense amplifiers are mainly used to read the contents of SRAM and DRAM cells. [1]

Sense amplifier can be operated in voltage, current and charge mode but we operate them in current-mode because they present a low impedance to the inputs and respond to the differential current rather than to the voltage between the inputs, this can reduce interconnect delay in long wires there by providing speed improvement. The current mode sense amplifier reduces the bit line swing during read operation as compared to voltage mode sensing

technique. It proves that current sensing technique would be faster than voltage mode due to the low impedance termination of the current

mode. It shows that current sensing is relatively insensitive to the bit line capacitance. This gives the motivation to use current mode sensing in the bit lines in SRAM.

From the past few decades, the growth of the electronics industry is very fast and also the use of integrated circuits in computing, telecommunications and consumer electronics increased. In 1958 there was only a single transistor on the chip called single transistor era and at present day ULSI (Ultra Large Scale Integration) systems with more than 50 million transistors in a single chip [9]. As operating frequency increases, chip size grows bigger and packing density reaches the ultra low scale integration level, power consumption becomes extremely important. The memory capacities of SRAM have roughly quadrupled

every three years. Each generation of CMOS SRAMs has advanced by reducing the memory cell size by about one-third and increasing the chip size by approximately 1.5 times with the advances in integrated circuit technology, the density of SRAMs in embedded applications has grown substantially in recent years. This has resulted in increase in bit and data lines capacitances thereby constituting a major bottleneck in achieving higher sensing speed in memory systems.

The three most important parameters in a memory system are: Power, Speed, and Area

The speed of VLSI chips is increasingly limited by signal delay in long interconnect lines. Major speed and power improvements are possible when using current mode rather than voltage mode signal transporting techniques. Moreover, with current mode sensing, reduction in the size of memory cell is another possibility. Since most of the memory related operations are read operations, this causes a large saving in the overall power dissipated by the memory. Also as sense amplifiers dissipates large quantity of short circuit power as opposed to the dynamic power dissipated by the cell array, large power is saved [3].

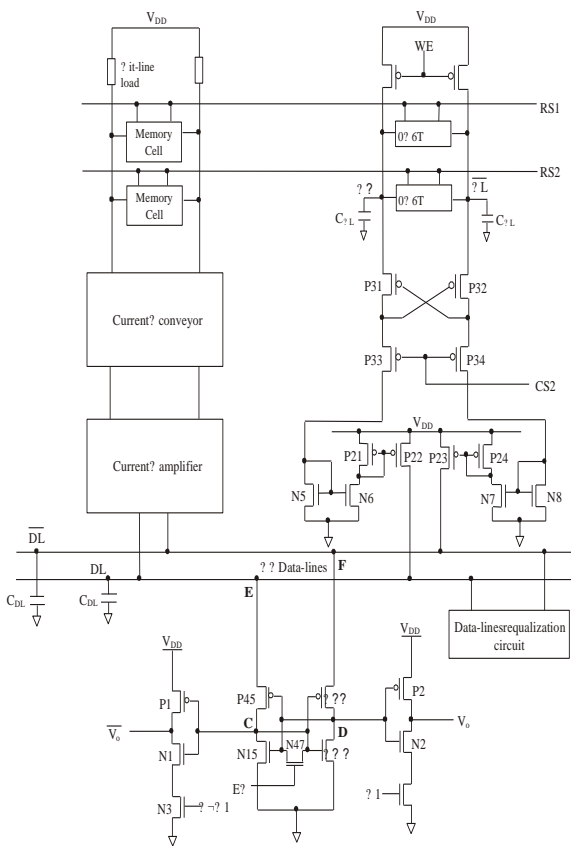
The need for the robust design of low power high speed CMOS analog VLSI circuits is growing tremendously.

## 2. ULTRA LOW POWER CURRENT MODE SENSE AMPLIFIER

The proposed current sense amplifier, coupled with a simplified read-cycle-only memory system, is portrayed in Fig.1. The left column presents the basic building blocks of the design, while the right column shows its transistor

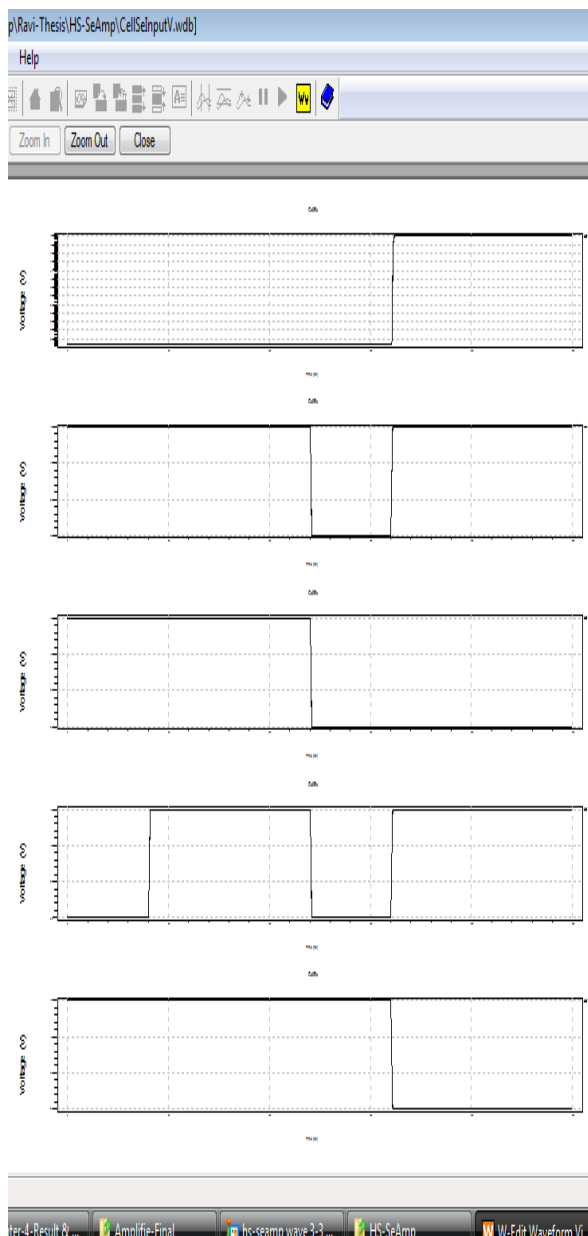
level/circuit structure .The proposed design has integrated the gist of the conventional current sense amplifier by including the transistors P 31, P 32, P 33 and P34 operating in saturation region. Owing to the simulation of this current conveyor ,the new circuit is intrinsically bit-line capacitance in sensitive science it has(ideally)zero input resistance during sensing .It also incorporates a current amplifier ,made up of two pairs of current mirrors at each bit-lines, which aims to amplify the bit-line current and Thus enhancing the sensing speed .Following that, Fig.1 embraces across coupled CMOS amplifier ( N 15, N 16, P 45, P 46and N 47)for global sensing .

differential current signals that Appear at the common bit-lines will then propagate to two pairs of NMOS current Mirror (N 5, N 6 and N 7, N 8). In view of the fact that P31, P 32, P 33and P 34 have to be in saturation mode to ensure a bit-line capacitance insensitive sensing delay ,the drains of P 33 and P 34 are pulled to a low-voltage with the aid of the relatively large-sized N 5 and N8. Mean while, the widths of N 6 and N 7 are appropriately sized to a smaller dimension to avoid non essential power wastage. However, the current mirrors at this stage act as current sink instead of current source. Two PMOS current mirrors (P 21, P 22and P 23, P 24) are therefore included to change the current direction to comply with our novel design of the power saving cross-coupled CMOS latch .These two PMOS current mirrors also double up as current amplifiers, which serve the purpose of increasing the current transmitted from the bit-lines by the same amplification ratio. After current intensification, the bit line currents are considered adequately large to enhance the sensing speed. Prior to the read cycle , nodes C and D are clamp data same potentially the pre-equalizing signal , EQ .This voltage-clamping signal can only be released after the differential current from the bit-lines resides at the data-lines to establish a correct data output .Since the current through P 22 is smaller than its P 23 counterpart , node E Is charged to a potential lower than node F( $V_E < V_F$  ).Coupled with the fact that the gates of P45 and P46 are initially clamped at an equal potential ,the magnitude of the source to gate voltage of P 45( $V_{SG}(P 45)$ ) is smaller than that of the  $V_{SG}(P46)$  .As a result , the voltage at node C is lower than the voltage at node D . Moreover , the CMOS amplifier , which is arranged in a cross-coupled configuration , causes the gate to source voltage of N15( $V_{GS}(N 15)$ ) to be higher than  $V_{GS}(N 16)$  .Due to the regenerative effect of this positive feed-back structure , the current sinking from node D will therefore be much lower than node C . The voltage at node D then increases further and the voltage at node C decreases .This process will continue until the output  $V_o$  discharges to VSS. The new current sense amplifier is capable of achieving an ultra low-powerdissipation due to the existence of then MOS devices (N 3andN 4) connected in Cascade with the output inverters .The control signal, Q1, is un asserted during the standby mode, hence rendering then MOS transistors in cutoff states .The inactive NMOS device inhibits the possibility of a DC current path flowing through VDD and VSS. Following that, a hefty portion of the unnecessary power dissipation is conserved [1].



**Fig-1 Ultra Low Power Current Mode Sense Amplifier [1]**

The complementary signals of the CMOS amplifier will feed their respective output sections, which are inverter stages, each cascaded with an additional NMOS transistor. This Supposedly minor tweak will aid in minimizing a major proportion of the unnecessary power dissipation. Data-line equalization is not compulsory in this circuit due to the inherent equalizing action of transistor N 47. C BL and C DL signify then bit-line and data-line capacitances, respectively, where as RS and CS denote the row and column-select. Consider both RS1 and CS2 being activated during a read operation. The memory cell at the upper row and right column will be selected, resulting in a smaller Current flow through BL than that at BL. These

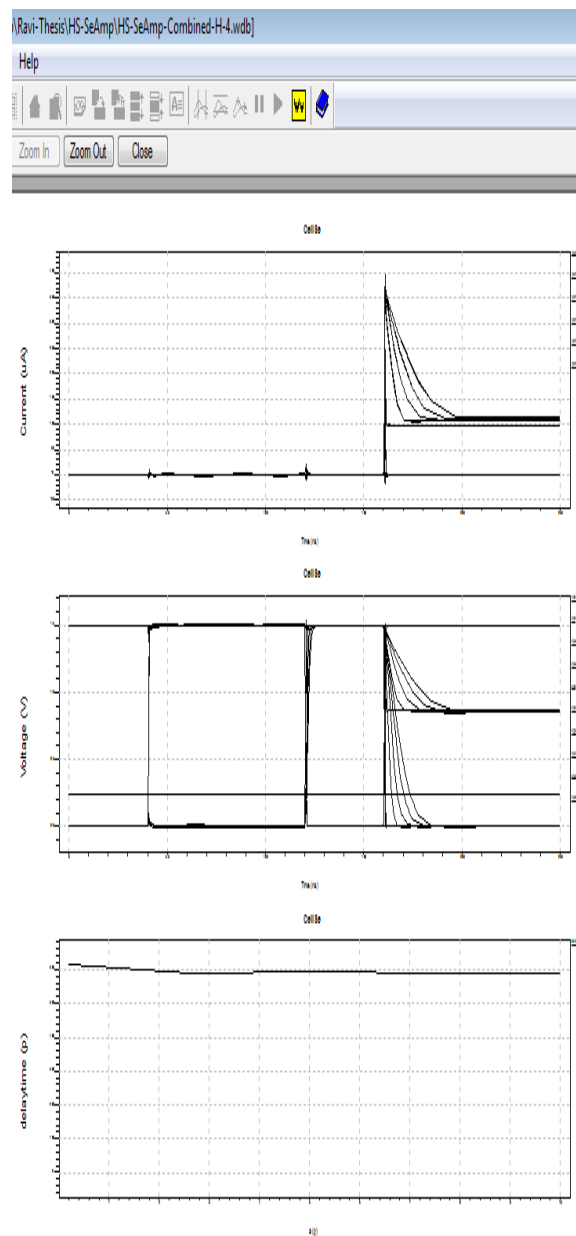


**Fig-2 Voltage Wave forms of High Speed Current Mode Sense Amplifier Circuit**

Voltage Signal of High Speed Current Mode Sense Amplifier Circuit at Node - clk

Voltage Signal of High Speed Current Mode Sense Amplifier Circuit at Node – wl

Voltage Signal of High Speed Current Mode Sense Amplifier Circuit at Node - cs



**Fig-3 Simulation Wave forms of High Speed Current Mode Sense Amplifier Circuit.**

Current waveform of High Speed Current Mode Sense Amplifier Circuit at Node – dlb

Voltage waveform of High Speed Current Mode Sense Amplifier Circuit at Node – dlb

Delay waveform of High Speed Current Mode Sense Amplifier Circuit at Node – delay

**Table-1 Comparison of sensing delay for high speed current mode sense amplifier at CDL = 1PF, Cout = 0.1 PF and CBL varies from 1 Pf of 5 Pf**

Bit Line Capacitance CBL (pf)	Sensing Delay for High Speed Current Mode Sense Amplifier(ns)
1	6.1324e-010
2	5.9127e-010
3	5.9317e-010
4	5.8848e-010
5	5.8932e-010

The analysis for High Speed Current mode Sense amplifier is done at TMS0.13um technology node with 1.5V power supply. The value of sensing delay is calculated for combinations of CBL = 1PF, CDL = 1PF Cout = 0.1Pf as shown in table-1. The analysis shows that the sensing speed of High Speed Current mode Sense amplifier independent of the variations in bit line capacitances.

### 3. CONCLUSION

The analysis for Conventional Current mode Sense amplifier is done at TMS0.13um technology node with 1.5V power supply. The value of sensing delay is calculated for combinations of CBL = 1PF, CDL = 1PF Cout = 0.1Pf as shown in table-1.

The analysis shows that the sensing speed of Current mode Sense amplifier independent of the variations in bit line capacitances. It is clear from above table the read delay of High Speed Current mode Sense amplifier is significantly less as compared to Conventional Current mode Sense amplifier

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