## Third Order Current-Mode Filter Realization using CMOS Current-Mirror

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Abstract: - In this paper, we have presented an approach to realize third order current-mode filters using CMOS current-mirrors with two different techniques. This paper presents the realization of third-order low-pass (LP) active current-mode filters using cascade technique of lossy and lossless integrators. Another important technique is the active realization of third-order low-pass filter that has been derived from the passive ladder-RLC Leapfrog filter structure. Interest in current-mode (CM) filters has been growing due to the fact that current-mode devices have wider dynamic range, improved linearity, and extended bandwidth as compared to their voltage-mode counterparts. In the sub-micron era of semi-conductor technology, the minute structure of devices causes a high electric field and thus the power supply voltage is limited to a certain low value to protect the device from destruction. Current-mode signal processing is quite attractive for operation at high frequencies and low power supply voltage operation from the viewpoint of sub-micron era. The realized filters do not contain any resistors, therefore simplifying the pattern of integrated circuits and thus reducing the chip area and the cost. The proposed circuits presented in the paper were tested in SPICE using 0.5 $\mu$ m CMOS process parameters provided by MOSIS (AGILENT) and the results thus obtained were in accordance with the theoretical values.

**Keywords:** – Continuous-time current-mode filters, Current Adders and Integrators, CMOS Current-Mirrors, Third Order Filters, Cascade realization, Leapfrog filter.

## INTRODUCTION

I.

Recent advancement in the field of integrated circuit technologies have miniaturized the devices used in an IC causing high internal electric field to develop. Therefore, the power supply voltage of the circuits must be reduced extremely to low value. In addition to this, the use of portable equipments has restricted the operation to a single battery [8], [9]. Also operation at high frequencies is a key desirable feature for these devices. In this respect, realizations of low-voltage and high-frequency active filters are an attractive choice in the field of signal processing.

Active filters are the best choice because they have the possibilities of integration and they are suitable for high frequency and low voltage operation. Among the numerous techniques available for the realization of active RC filters, we present two different methods in this paper namely (i) Cascade realization and (ii) Leapfrog realization [17]. These techniques of filter realizations are quite popular and can generate any type of transfer function. Traditionally, such circuits work in the continuous-time domain and have being designed as resistively terminated lossless LC filters where resonance could be employed to achieve complex poles and the desired steep transition region between the pass bands and the stop bands. With the growing pressure towards micro-miniaturization, inductors were found to be too bulky so that designers started to replace passive RLC filters by their active RC counterpart circuits where gain was obtained from operational amplifiers, and with the presence of resistors and capacitors in feedback networks, complex poles can be achieved. Active filters designed using the ubiquitous op-amp have found wide acceptance throughout the literature over the past and their mature development and technology guarantee their continued popularity in many applications.

One disadvantage of these op-amp based active RC filters is the limited frequency range of operation over which these circuits can be used: the finite bandwidth of op-amps usually confined the application to be below 100 kHz with performance becoming deteriorating with increasing frequency [2], [3]. For operation in MHz range the main design challenges for the analog filters are: (i) Reliable high-frequency performance. (ii) Automatic on-chip tuning against fabrication tolerances and changing operating conditions [4] and [5].

For application as continuous-time filters, the transconductance [1], [6] should satisfy the following properties: (i) Circuits must be simple, linear and should have a wider frequency response. (ii) Must have large input and output impedances to prevent undesirable interactions and simplify circuit design. (iii) They should preferably work with low-voltage power supplies to conserve power and to be compatible with the prevalent digital technologies on the same chip. (iv) Their transconductance parameter must depend on some dc bias voltage or current to facilitate electronic tuning against environmental or processing variations [7].

In many useful active simulation of filters, we may even insist that all the transconductors are identical and all the capacitors are grounded for specially simple IC layout and processing, and implementation of integrated analog filters based on analog gate arrays appears to be a distinct possibility. In addition, the wider useful bandwidth of transconductances coupled with the reduced effects of circuit and device parasitics on filter performance result in far higher operating frequencies at which the circuits can function.

## II. PROPOSED CIRCUITS

Current-mode signal processing is quite attractive for low power supply voltage operation and high frequency application. In this paper design of current-mode filters using nMOS transistor current mirrors and pMOS transistor current sources as an active load, as reported in [2], which is a counterpart of the MOS realization [4], [5] are presented. In such designs, pMOS transistors were only used for DC current sources which provide bias currents to the current mirrors and also behave as an active load for the current mirror.

The currents of these sources must match with each other and also match with the DC currents of each current mirror to give a proper DC bias to transistors. However the matching is sometimes difficult due to the parameter mismatch between nMOS and pMOS transistors [1], [5]. Here, we present design of CMOS continuous-time filters using nMOS and pMOS transistor current mirrors. Using pMOS transistors as signal processing elements, the circuits can be simplified and problems resulting from difficulty of DC biasing can be avoided.

Using integrators and adders, any kind of transfer function can be realized; therefore the method can easily be applied for wide range of filter realization. Generally, monolithic integrated filters have a difficulty on setting the filter frequency due to absolute value error of elements. In these filters, the tuning of the filter frequency can easily be achieved by adjusting the current of a single DC current source.

# 2.1 Realization of Current-Mode Third-Order Low Pass Active Filter using Cascade Realization Technique:

As the first-order low pass section can be realized by the lossy integrator of Fig. 2 and Fig. 4 of [10], the third-order section is presented here. Figure-1 shows the block diagram of the current-mode third-order low Pass section using two lossy integrators and a lossless integrator of Fig. 4 and Fig. 6 respectively of [10].



Fig. 1: Block Diagram of Third-Order Section

From the routine analysis we obtain the current transfer function of the block diagram shown in Figure-1 which is given by equation-2.1

$$T_{LP}(s) = \frac{I_O}{I_{in}} = \frac{1}{s^3 C_1 C_2 C_3 R_1 R_2 R_3 + s^2 C_1 R_1 (C_2 R_2 + C_3 R_3) + s C_1 R_1 + s C_3 R_3 + 1}$$
(2.1)

On comparing equation-2.1 with the standard form of third-order low pass transfer function given by equation-2.2 we obtain the following results for the gain (H<sub>0</sub>), cut-off frequency ( $\omega_0$ ) and the quality factor (Q) which is given by equation-2.3.

$$T_{LP}(s) = \frac{H_0 \omega_0^3}{s^3 + s^2 \omega_0 \left(\frac{1}{Q} + 1\right) + s \omega_0^2 \left(\frac{1}{Q} + 1\right) + \omega_0^3}$$
(2.2)

where,

$$H_{0} = 1, \omega_{0} = \sqrt[3]{\frac{1}{C_{1}C_{2}C_{3}R_{1}R_{2}R_{3}}} \text{ and } Q = \frac{\omega_{0}}{\frac{C_{2}R_{2} + C_{3}R_{3}}{C_{2}C_{3}R_{2}R_{3}} - \omega_{0}}$$
(2.3)

Figure-2 shows the practical realization of the proposed third-order low pass filter where the complementary type of the simplified lossy integrator shown in Fig. 4 [10] and the lossless integrator of Type-I shown in Fig. 5 [10] are used and the DC bias current source  $I_B$  of simplified lossy integrator of Fig. 4 [10] is eliminated by the use of the output DC bias current of M<sub>4</sub> of Fig. 2 [10].



Assuming that all transistors of Figure-2 have an equal aspect ratio's that is, all the current mirrors have same (W/L) ratios, so we obtain the following transfer function:

$$T_{LP}(s) = \frac{1}{s^3 C_1 C_2 C_3 R^3 + s^2 C_1 R^2 (C_2 + C_3) + sR(C_1 + C_3) + 1}$$
(2.4)

Since the DC bias currents of all transistors are equal to the bias current  $I_{\rm B}$ , the resistances are given by, kT 1 0.0259 n (**0** 5)

$$R_{1} = R_{2} = R_{3} = R \cong \frac{1}{q} I_{B} \cong \frac{1}{I_{B}}$$
and also we have,  $I_{B1} = I_{B2} = I_{B3} = I_{B}$ .
(2.5)
(2.6)

and also we have,  $I_{B1} = I_{B2} = I_{B3} = I_B$ .

Equation-2.5 shows that  $I_B$  controls  $R_1$ ,  $R_2$  and  $R_3$  simultaneously and equation-2.3 shows that the simultaneous control of R<sub>1</sub>, R<sub>2</sub> and R<sub>3</sub> does not affect the Q factor. Thus we can control the cut-off frequency of the filter  $\omega_0$ without changing the Q factor.

While cascading the first-order or second-order sections, the DC bias current  $I_B$  of each stage can be provided from the output of the former stage and therefore a single DC bias current source is only required at the front stage of filters.

### 2.2 Realization of Current-Mode Third-Order Low Pass Active Filter using Leapfrog Realization **Technique:**

Leapfrog structure that simulates doubly terminated LC filters has been highly appreciated since it inherits the low sensitivity natures of the prototype LC filters [9], [18]. From the viewpoint of high frequency and low voltage applications of the filters, low gain amplifiers such as unity gain voltage buffer and unity gain current buffer would be the most reasonable active blocks that could have a wide gain bandwidth and operate at a low power supply voltage. Figure-3 shows a prototype of the third-order LC low pass filter whose block diagram representation is shown in Figure-4, realized using lossy and lossless integrators. The CMOS implementation of the same using lossy and lossless integrators is shown in Figure-5.



Fig. 3: Third-order Leapfrog LC ladder Low-Pass Prototype



Fig. 4: Block Diagram Representation of Third-order Leapfrog LC ladder Low-Pass Prototype



Fig. 5: CMOS Implementation of Current-Mode Third-order Leapfrog LC ladder Low-Pass Prototype

#### SIMULATION RESULTS III.

The workability of the proposed circuits were tested and verified in SPICE using 0.5µm CMOS process parameters provided by MOSIS (AGILENT) as listed in Table-1.

TABLE-1: CMOS PROCESS PARAMETERS										
TRANSISTOR	PROCESS PARAMETERS									
nMOS	LEVEL=3 UO=460.5 TOX=1.0E-8 TPG=1 VTO=0.62 JS=1.08E-6 XJ=0.15U RS=417 RSH=2.73 LD=0.04U VMAX=130E3 NSUB=1.17E17 PB=0.761 ETA=0.00 THETA=0.129 PHI=0.905 GAMMA=0.69 KAPPA=0.10 CJ=76.4E-5 MJ=0.357 CJSW=5.68E-10 MJSW=0.302 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=3.07E-28 AF=1 WD=0.11U DELTA=0.42 NFS=1.2E11									
pMOS	LEVEL=3 UO=100 TOX=1.0E-8 TPG=1 VTO=0.58 JS=0.38E-6 XJ=0.10U RS=886 RSH=1.81 LD=0.03U VMAX=113E3 NSUB=2.08E17 PB=0.911 ETA=0.00 THETA=0.120 PHI=0.905 GAMMA=0.76 KAPPA=2 CJ=85E-5 MJ=0.429 CJSW=4.67E-10 MJSW=0.631 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=1.08E-29 AF=1 WD=0.14U DELTA=0.81 NFS=0.52E11									

## 3.1 Simulation Results for the Current-Mode Third-Order Low Pass Active Filter using Cascade **Realization Technique:**

For the circuit shown in Figure-2 the ac analysis were carried out with the value of dc bias current  $I_{B1}$  =  $I_{B2} = I_{B3} = 40\mu A$ ,  $C_1 = C_2 = C_3 = 1 \text{ pF}$ ,  $(W/L)_P$  ratio =  $1\mu m/1\mu m$ ,  $(W/L)_N$  ratio =  $1\mu m/1\mu m$  and supply voltage  $V_{DD} = 2.5V$ . The value of cut-off frequency is found to be  $f_0 = 6.146MHz$  which is very well in agreement with the calculated theoretical value of  $f_0 = 6.15$  MHz. SPICE simulation results are shown in Figure-6.



Figure-7 shows the change in the value of cut-off frequency with change in the values of capacitor  $C_1$ ,  $C_2$  and  $C_3$  where the values of the three capacitors were varied from 1pF to 20pF.

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Fig. 7: Variation in the cut-off frequency with change in Capacitor values

Figure-8 shows the change in the value of gain with change in the value of bias current when varied from  $1\mu A$  to 40uA.



**3.2** Simulation Results for the Current-Mode Third-Order Low Pass Active Filter using Leapfrog Realization Technique:

For the circuit shown in Figure-5 the ac analysis were carried out with the value of dc bias current  $I_{B1} = I_{B2} = 70\mu$ A and  $I_{B3} = 30\mu$ A,  $C_1 = C_2 = 5pF$  and  $C_3 = 1pF$ ,  $(W/L)_P$  ratio =  $10\mu$ m/1 $\mu$ m,  $(W/L)_N$  ratio =  $1\mu$ m/1 $\mu$ m and supply voltage  $V_{DD} = 2.5V$ . The value of cut-off frequency is found to be  $f_0 = 9.763$ MHz which is very well in agreement with the calculated theoretical value of  $f_0 = 9.75$ MHz. SPICE simulation results are shown in Figure-9.



Fig. 9: Low Pass Response of Third-Order Current-Mode Leapfrog LC ladder Low-Pass Prototype

Figure-10 shows the change in the value of cut-off frequency with change in the values of capacitor  $C_1$  and  $C_2$  while the value of the capacitor  $C_3$  is kept constant. The values of the two capacitors  $C_1$  and  $C_2$  were varied from 5pF to 50pF.



Fig. 10: Variation in the gain of Third-Order Current-Mode Leapfrog LC ladder Low-Pass Prototype with Capacitor C<sub>1</sub> and C<sub>2</sub>

## IV. CONCLUSION

In the given paper high frequency third order current-mode filter have been presented which are quite suitable for the realization in high frequencies of more than 10MHz and these filters can operate at a voltage as low as 1.5V or less. Also, it has been verified that variations in the value of either the capacitor or the bias current improves the gain as well as the operating frequency of the filters. The frequency of this filter can be easily and widely controlled by a single DC bias current and thus provides good tunability. All the circuits were tested using SPICE and the verified results confirms the theoretical values.

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