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# 4-Input Decimal Adder Using 90 nm CMOS Technology

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***ABSTRACT-****The core of every microprocessor, digital signal processor (DSP), and data processing application-specific integrated circuit(ASIC) is its data path. At the hearts of data paths and addressing units are arithmetic units, such as a comparators , adders, and multipliers. In this paper, a 4-input decimal adder has been developed using 90 nm CMOS technology. The schematic of decimal adder is designed and simulated for its behavior using DSCH-3.1 The layout of simulated adder is created using Verilog based netlist file which is further simulated using Micro wind 3.1 to analyze the performance. The result shows that designed decimal adder has consumed 0.603mW power.*

***Keywords-****Adders, ALU,ASIC, Carry Look Ahead Adders, CMOS, Decimal Addition, DSP .*

## I. INTRODUCTION

Binary addition is one of the most primitive and most commonly used applications in computer arithmetic .With the rapid growth of decimal arithmetic in many applications such as commercial, financial, or internet field. The use of simplest and easy method of decimal arithmetic becomes very important for the designers and users. In the past decades, although the binary arithmetic is widely used in processors or any other applications, but some problem occurred in performing some binary arithmetic operations. For Example, the fraction numbers cannot be represented by using the binary numbers. E.g., $0.7_{10} = 0.10111_{.....2}$ , it will require infinite bits for representation, so it become incorrect decimal fractions.[2] This incorrect representation of decimal fraction causes approximation errors. So, to overcome this drawback of binary arithmetic, the Binary Coded Decimal numbers is used. In BCD , each bit of decimal numbers 0 to 9 uses four bits $0000_2$ to $1001_2$ . The focus here is to design a decimal adder using four inputs. The rest of this paper is organized as follows . Section II will introduce BCD additions. Then the basic schematic & layout of 1-digit decimal adders are given in Section III & IV. The schematic & implementations results of 4-input BCD adder is discussed in Section V and Section VI is our conclusion.

## II. METHODOLOGIES

BCD numbers exist from 0 to 9, these give a coded sequence for all decimal numbers. The numbers above 9 are represented as a combination of two BCD codes.BCD numbers are weighted codes usually of the form 8 4 2 1 , where each value gives the weight for each digit. The BCD code for decimal numbers are shown in table no. 1

**Table No. 1: BCD representation of Decimal Numbers**

| Bits | Digit | Bits | Digit |
|---|---|---|---|
| 0000 | 0 | 0101 | 5 |
| 0001 | 1 | 0110 | 6 |
| 0010 | 2 | 0111 | 7 |
| 0011 | 3 | 1000 | 8 |
| 0100 | 4 | 1001 | 9 |

| Bits | Digit | Bits | Digit |
|---|---|---|---|
| 1010 | - | 1101 | - |
| 1011 | - | 1110 | - |
| 1100 | - | 1111 | - |

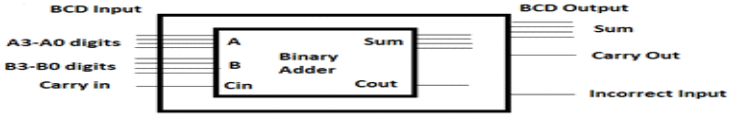


**Figure 1:**

If we try to add two BCD numbers , then there is no error till the sum lies from 0 to 9 . But , as the sum is above 9 , then it will not give the correct BCD output. The addition of BCD number is shown in figure 1. In order to correct this output ,add $6(0110)_2$ to the sum output to overcome the six unused states at the output .The output of the BCD addition which lies between 10 to 19 is shown below in Table no. 2.

**Table. 2 Binary Vs BCD Addition**

| **Sum** | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|
| **Binary Sum** | 1010 | 1011 | 1100 | 1101 | 1110 |
| **Binary $C_{out}$** | 0 | 0 | 0 | 0 | 0 |
| **BCD Sum** | 0000 | 0001 | 0010 | 0011 | 0100 |
| **BCD $C_{out}$** | 1 | 1 | 1 | 1 | 1 |
| **Sum** | 15 | 16 | 17 | 18 | 19 |
| **Binary Sum** | 1111 | 0000 | 0001 | 0010 | 0011 |
| **Binary $C_{out}$** | 0 | 1 | 1 | 1 | 1 |
| **BCD Sum** | 0101 | 0110 | 0111 | 1000 | 1001 |
| **BCD $C_{out}$** | 1 | 1 | 1 | 1 | 1 |

To make a 4 bit BCD adder , we require a 4 bit carry ripple adder along with some logic to convert the output into correct form. It is possible to create the logical circuit using multiple full adders to add n- bit binary numbers. The full adder inputs a $C_{in}$ ,which is the $C_{out}$ of the previous adder .This kind of adder is a Ripple Carry Adder , since each carry bit "ripples" to the next full adder . The first (and only the first) full adder may be replaced by a half adder. Figure No. 2 shows the block Diagram of 4-bit Ripple Carry Adder.

## III. SCHEMATIC

Suppose, it is given that there are two inputs of 1 digit BCD numbers A and B,the conventional conventional architecture of the decimal addition of A and B is shown in Fig. 2.By using this 1 digit adder composed of 4 consecutive full adders to sum up the values of A and B , the digit adder with with correction in yhe parenthesis which is also composed of 4 consecutive full adders to produce the sumsw of A and B and the correction values 0110 , is determined by the output of $C_{out}$ +(S[3].S[4] +S[2]. S[3]), where ' +' denotes logical OR and '. ' denotes logical AND operations , and $C_{out}$ is the carry -out of A+B.[2]

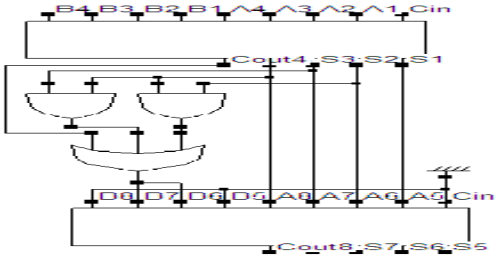


**Fig. 2: Basic One-digit BCD Adder [1]**

## III. LAYOUT DESIGN & ANALYSIS

The layout of above 1 -digit decimal adder given in fig.2 has been simulated and designed using CMOS 90 nm technology in Microwind 3.1 which is shown in fig. 3

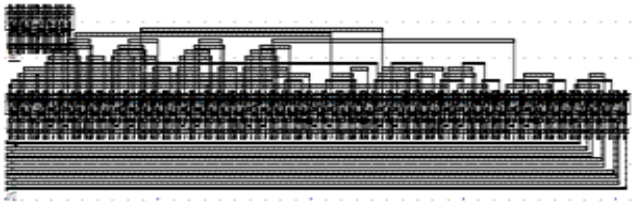

**Fig. 3: Layout of one-digit BCD adder**

## V. SCHEMATIC AND LAYOUT OF 4-INPUT ADDER

In this paper, a decimal adder with 4-input with each input is four digits has been presented using 90 nm CMOS technology. The hierarchical structured approach has been used for designing the decimal adder .In this approach , initially 1-bit adder has been developed which is converted into its modular form. The created module has been further utilized to design 4-input decimal adder which is shown in figure 4

**Fig. 4: Hardware of 4-input decimal addition**

**The simulated result of 4-input decimal adder in Microwind 3.1 is shown below in fig.**

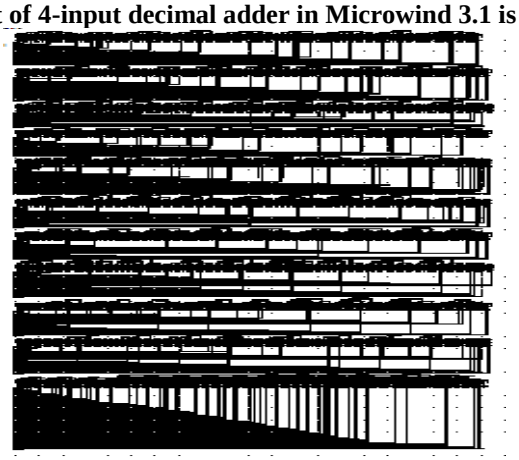

**Fig. 5: Layout of 4-input BCD Adder**

The performance of both adder is analyzed and compared in terms of power which is shown in table no. 4

## VI. CONCLUSION

A decimal adder with 4-input has been designed using 90 nm CMOS technology for its implementation .It can be observed from simulated results that 1 - bit adder provides 50.751µW power & 4-input adder provides 0.603mW power respectively.

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