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Performance Analysis of Energy Efficient and Charge Recovery Adiabatic Techniques for Low Power Design

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Abstract: **-** The power consumption of the electronic devices can be reduced by adopting different design styles. Adiabatic logic style is said to be an attractive solution for such low power electronic applications. By using Adiabatic techniques energy dissipation in PMOS network can be minimized and some of energy stored at load capacitance can be recycled instead of dissipated as heat. In analysis, two logic families, ECRL(Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) are compared with conventional CMOS logic for inverter and 2:1 multiplexer circuits. The proposed technique has less power dissipation when compared to the conventional CMOS design style.

Key Words- *Adiabatic, dissipation, Logic families, low power, recycled.*

I. INTRODUCTION

Power consumption plays an important role in the present day VLSI technology. As many of the present day electronic devices are portable, they need more battery backup which can be achieved only with the low power consumption circuits that are internally designed in them. So energy efficiency has become main concern in the portable equipments to get better performance with less power dissipation. As the power dissipation in a device increases then extra circuitry is necessary to cool the device and to protect the device from thermal breakdown which also results in increase of total area of the device. In order to overcome these problems the power dissipation of the circuit is to be reduced by adopting different low power techniques. The less the power dissipation, the more efficient the circuit will be [1]. From the past few decades CMOS technology plays a dominant role in designing low power consuming devices. Compared to different logic families CMOS has less power dissipation which made it superior over the previous low power techniques [2].

The power consumption in conventional CMOS circuit is due to switching activity of the devices from one state to another state and due to the charging and discharging of load capacitor at the output node. The power dissipation in conventional CMOS design can be minimized by reducing the supply voltage, node capacitance value and switching activity [3]. But reducing the values of these parameters may degrade the performance of the device. So an efficient low power technique other than CMOS is needed that has less power dissipation compared to CMOS which can be done by using adiabatic techniques. The present paper focuses on a novel energy efficient technique called adiabatic logic which is based on energy recovery principle. In this technique instead of discharging the consumed energy is recycled back to the power supply thereby reducing overall power consumption [4].

II. CMOS INVERTER

CMOS is the basic building block of many of the digital circuits. The CMOS circuit itself acts as an inverter. It can be realized as a combination of PMOS in the pull up section whose source is connected to power supply and NMOS in the pull down section whose source is connected to ground and the output is taken across the drain junction of the two devices. The CMOS circuit has less power dissipation when compared to many of the previous VLSI families of RTL, TTL and ECL [5]. The power consumption in CMOS is due to the switching activity of the transistors from one state to another state, charging and discharging of the load capacitance and frequency of operation. The basic CMOS inverter circuit is shown in fig. 1.

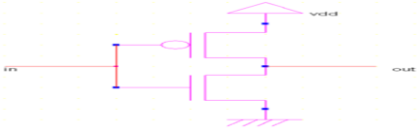

Fig 1: Conventional CMOS inverter

The operation of the circuit can be evaluated in two stages of charging phase and discharging phase. During the charging phase, the input to the circuit is logic LOW. During this phase, the PMOS transistor conducts and NMOS transistor goes in to OFF state which charges the output value to power supply results in

logic HIGH output. The equivalent circuit consists of a resistor in series with the output load capacitance which shows a charging path from power supply to output terminal. Here the resistor acts a PMOS ON resistor.

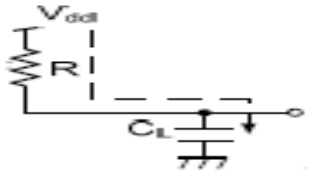

Fig 2: Equivalent Circuit for Charging Process in CMOS

During the discharging phase, the input to the circuit is logic HIGH. During this phase, the NMOS transistor conducts and PMOS transistor goes into OFF state which results in a discharging path from output terminal to ground. The value that is stored at the output during the charging phase discharges towards the ground results in logic LOW output. The equivalent circuit consists of a resistor in series with output terminal to ground. Here the resistor acts as NMOS ON resistor.

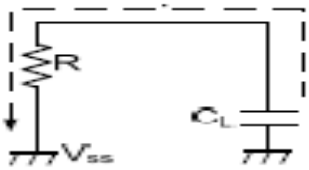

Fig. 3: Equivalent Circuit for Discharging Process in CMOS

From the operation of the CMOS design it is evident that during the charging process, the output load capacitor is charged to $Q = C_{L.}V_{DD}$ and the energy stored at the output is $(1/2)C_{.L}V_{DD.}^{2}$ During the discharging phase, the amount of energy dissipated is also $(1/2)C_{L.}V_{DD}^{2}$

So the total amount of energy dissipated during the charging and discharging phases is

$E_{dissipated} = C_{L}V_{DD}^{2}$ ……(1)

The power consumption of the CMOS circuit is based on the following equation

$P = CV^{2}f$ ……(2)

From the equation it is evident that the power dissipation of CMOS can be reduced by minimizing the supply voltage, node capacitance and switching activity to some extent. But reducing the values of these parameters may suffer from some disadvantages. Reducing the load capacitance is strongly limited by the technology. Reducing the supply voltage may degrade the performance of the device. Reducing the supply voltage may also suffer from leakage problems. In order to overcome these problems an efficient low power technique called adiabatic logic is explained in this paper.

III. ADIABATIC LOGIC

The word ADIABATIC is derived from the Greek word "adiabatos",which means there is no exchange of energy with the environment and hence no energy loss in the form of heat dissipation. Adiabatic logic is commonly used to reduce the energy loss during the charging and discharging process of circuit operation. Adiabatic logic is also known as "energy recovery" or "charge recovery" logic. As the name itself indicates that instead of dissipating the stored energy during charging process at the output node towards ground it recycles the energy back to the power supply thereby reducing the overall power dissipation and hence the power consumption also decreases. The adiabatic logic uses AC power supply instead of constant DC supply this is one of the main reasons in the reduction of power dissipation. The adiabatic logic can be explained with the help of basic inverter circuit.

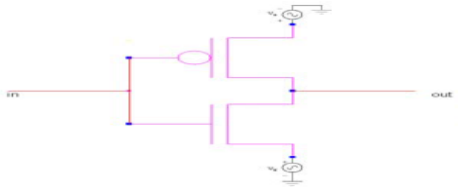

Fig. 4: Adiabatic Inverter

The adiabatic inverter circuit can be constructed using CMOS inverter with two AC power supplies instead of DC supply. The power supplies are arranged in such a way that one of the clock is in phase while the other is out of phase with the first one. The operation of the adiabatic inverter can be explained in two stages.

During the charging phase, the PMOS transistor conducts and NMOS transistor goes into OFF state which charges the output load capacitor towards the power supply results in logic HIGH output.

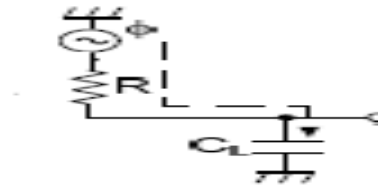

Fig. 5: Equivalent Circuit for Charging Process in Adiabatic Inverter

During discharging phase, the NMOS transistor conducts and PMOS transistor goes into OFF state. Instead of discharging the stored value at the output towards ground, the energy is recycled back to the power supply. Its equivalent circuit consists of a resistor in series with output load capacitance and power supply.

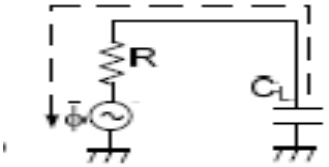

Fig. 6: Equivalent Circuit for Charge Recovery Process in Adiabatic Inverter

The charging process and the charge recovery process are efficient only when the charging voltage is varying one. Lower the rate of charging, lesser the power drawn from the supply voltage.

IV. DISSIPATION MECHANISMS IN ADIABATIC LOGIC CIRCUITS

Fig.7 shows, the equivalent circuit used to model the conventional CMOS circuits during charging process of the output load capacitance. But here constant voltage source is replaced with the constant current source to charge and discharge the output load capacitance. Here R is on resistance of the PMOS network, C_L is the load capacitance [6].

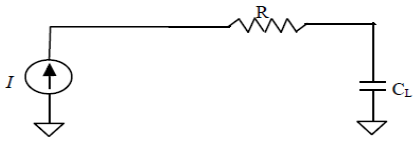

Fig.7 Equivalent model during charging process in Adiabatic circuits.

Energy dissipation in resistance R is [1]

$$E_{DISS} = I^2.R.T = \left(\frac{C_L V_{DD}}{T}\right)^2 .R.T = \left(\frac{RC_L}{T}\right).C_L V_{DD}^2 \dots\dots(3)$$

Since E_{DISS} depends upon R, so by reducing the on Resistance of PMOS network the energy dissipation can be minimized. The on resistance of the MOSFET is given by the first order approximation is [9-10],

$$R = \left[\mu C_{OX} \frac{W}{L} (V_{GS} - V_{TH})\right]^{-1} \dots\dots(4)$$

Where μ is the mobility, C_{OX} is the specific oxide capacitance, V_{GS} is the gate source voltage w is the width, L is the length and V_{TH} is the threshold voltage.

E_{DISS} also depends upon the charging time T, If T>>2RC then energy dissipation will be smaller than the conventional CMOS [6]. The energy stored at output can be retrieved by the reversing the current source direction during discharging process instead of dissipation in NMOS network. Hence adiabatic switching technique offers the less energy dissipation in PMOS network and reuses the stored energy in the output load capacitance by reversing the current source direction [6, 7].

V. ADIABATIC LOGIC FAMILIES

There are the many adiabatic logic design technique [12-22] are given in literature but here two of them are chosen ECRL [14] and PFAL [15], which shows the good improvement in energy dissipation and are mostly used as reference in new logic families for less energy dissipation.

Practical adiabatic families can be classified as either PARTIALLY ADIABATIC or FULLY ADIABATIC. In a PARTIALLY ADIABATIC CIRCUIT, some charge is allowed to be transferred to the

ground, while in a FULLY ADIABATIC CIRCUIT, all the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face a lot of problems with respect to the operating speed and the inputs power clock synchronization.

Popular Partially Adiabatic families include the following:

i. Efficient Charge Recovery Logic (ECRL).
ii. 2N-2N2P Adiabatic Logic.
iii. Positive Feedback Adiabatic Logic (PFAL).
iv. NMOS Energy Recovery Logic (NERL).
v. Clocked Adiabatic Logic (CAL).
vi. True Single-Phase Adiabatic Logic (TSEL).
vii. Source-coupled Adiabatic Logic (SCAL).

Some Fully adiabatic logic families include:

i. Pass Transistor Adiabatic Logic (PAL).
ii. Split- Rail Charge Recovery Logic (SCRL).

Among these logic families two of them are chosen ECRL [14] and PFAL [15], which shows the good improvement in energy dissipation and are mostly used as reference in new logic families for less energy dissipation.

A. EFFICIENT CHARGE RECOVERY LOGIC (ECRL)

The schematic of ECRL inverter gate is shown in Fig.8. Initially, input 'in' is high and input '/in' is low. When power clock (pck) rises from zero to V_{DD}, since F is on so output 'out 'remains ground level. Output '/out' follows the pck. When pck reaches at V_{DD}, outputs 'out' and '/out' hold logic value zero and V_{DD} respectively. This output values can be used for the next stage as an inputs. Now pck falls from V_{DD} to zero, '/out 'returns its energy to pck hence delivered charge is recovered. ECRL uses four phase clocking rule to efficiently recover the charge delivered by pck. For detailed study follow the reference [14].

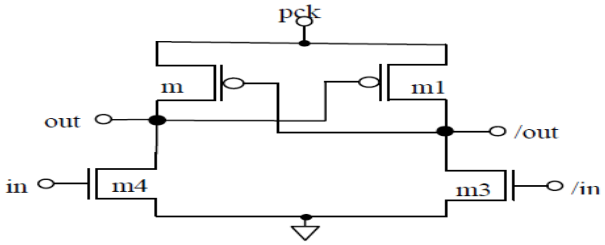

Fig.8 Schematic of ECRL inverter

The schematic of ECRL 2:1 Multiplexer is shown in Fig.9 Initially, select input 's' is high and power clock (pck) rises from zero to V_{DD}, output 'out' will select the input 'b'. If select input 's' is low and power clock (pck) rises from zero to V_{DD}, output 'out' will select the input 'a'. When pck reaches at V_{DD}, outputs 'out' and '/out' hold logic values. This output values can be used for the next stage as an inputs. Now pck falls from V_{DD} to zero, high outputs return its energy to pck hence delivered charge is recovered.

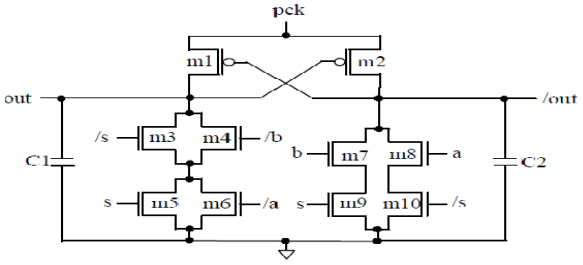

Fig 9.Schematic of ECRL multiplexer

B. Positive Feedback Adiabatic Logic (PFAL)

The schematic of the PFAL inverter gate is shown in Fig10 Initially, input 'in' is high and input '/in' is low. When power clock (pck) rises from zero to V_{DD}, since m5 and m4 are on so output 'out' remains ground level. Output '/out' follows the pck When pck reaches at V_{DD}, outputs 'out' and '/out' hold logic value zero and V_{DD} respectively. This output values can be used for the next stage as an inputs. Now pck falls from V_{DD} to zero, '/out' returns its energy to pck hence delivered charge is recovered. PFAL uses four phase clocking rule to efficiently recover the charge delivered by pck. For detailed study follow the reference [15, 17].

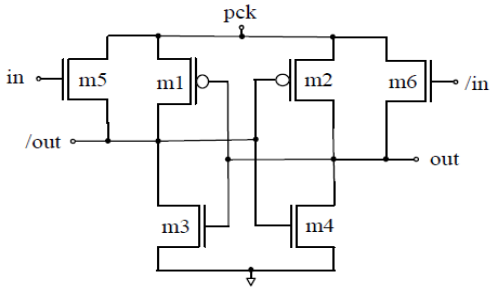

Fig 10:Schematic of PFAL inverter

The schematic of PFAL 2:1 Multiplexer is shown in Fig.11. Initially, select input 's' is high and power clock (pck) rises from zero to V_{DD}, output 'out' will select the input 'b'. If select input 's' is low and power clock (pck) rises from zero to V_{DD} output 'out' will select the input 'a'. When pck reaches at V_{DD}, outputs 'out' and '/out' hold logic values. This output values can be used for the next stage as an inputs. Now pck falls from V_{DD} to zero, high outputs return its energy to pck hence delivered charge is recovered.

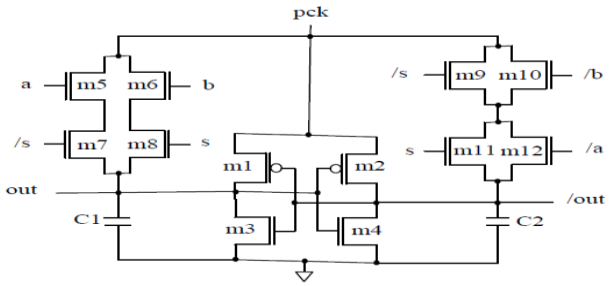

Fig 11:Schematic of PFAL multiplexer

VI. IMPACT OF PARAMETER VARIATIONS ON THE ENERGY CONSUMPTION

Energy consumption in adiabatic circuits strongly depend on the parameter variations [22-24]. The impact of parameter variations on the energy consumption for the two logic families is investigated with respect of CMOS logic circuit, by means of MICROWIND simulations. Simulations are carried out at 250nm technology node. The W/L ratio of the PMOS and NMOS are taken as 9ʎ/2ʎ and respectively, where ʎ = 125nm.

A. Transition Frequency Variation

Fig.12 shows the energy dissipation per cycle versus switching frequency of the two adiabatic logic families and CMOS for the inverter logic. Fig.13 shows the energy dissipation per cycle versus switching frequency of the two adiabatic logic families and CMOS for the 2:1 multiplexer. It is seen that for high frequency the behavior is no more adiabatic and therefore the energy dissipation increases. At low frequencies the dissipation energy will increase for both CMOS and adiabatic logic due to the leakage currents of the transistors. Thus the simulations are carried out only at useful range of the frequencies to show better result with respect to CMOS.

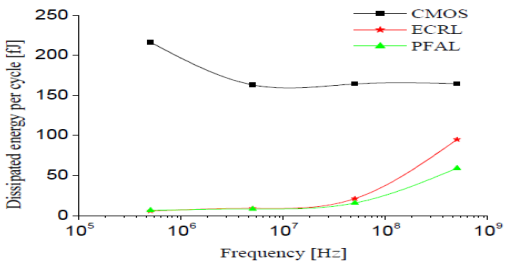

Fig.12 Energy consumption per cycle versus frequency for an inverter at V_{DD}= 2.5V and load capacitance = 20fF.

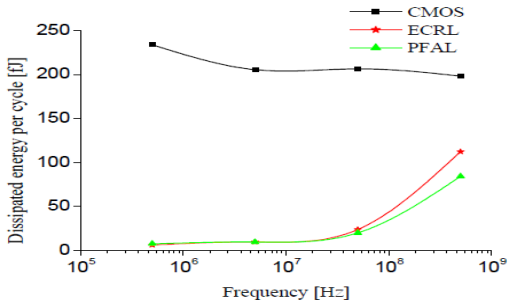

Fig.13 Energy consumption per cycle versus frequency for a 2:1 multiplexer at V_{DD}= 2.5V and load capacitance = 20fF.

B. Load Capacitance Variation

Fig.14 shows the energy dissipation per cycle versus load capacitance of the two adiabatic logic families and CMOS for the inverter logic. Fig.15 shows the energy dissipation per cycle versus load capacitance of the two adiabatic logic families and CMOS for the 2:1 multiplexer. The Figures show that adiabatic logic families having better energy savings than CMOS logic over wide range of load capacitances. PFAL shows better energy shavings than ECRL at high load capacitance.

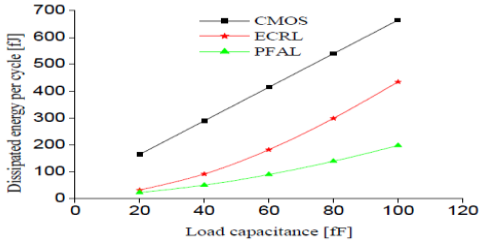

Fig.14: Energy consumption per cycle versus load capacitance for an inverter at V_{DD} = 2.5V and frequency = 100 MHz

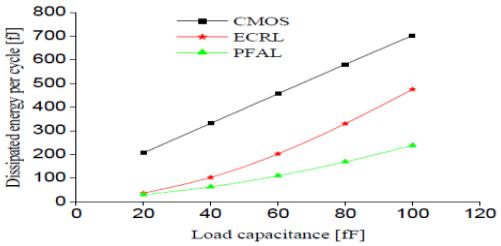

Fig. 15 Energy consumption per cycle versus load capacitance for a 2:1 multiplexer at V_{DD} = 2.5V and frequency = 100 MHz.

C. Supply Voltage Variation

Fig.16 shows the energy dissipation per cycle versus supply voltage of the two adiabatic logic families and CMOS for the inverter logic. Fig. 17 shows the energy dissipation per cycle versus supply voltage of the two adiabatic logic families and CMOS for the 2:1 multiplexer. It is seen that supply voltage decreases, the gap between CMOS and logic families is reduced. But ECRL and PFAL still shows large energy savings over wide range of supply voltage.

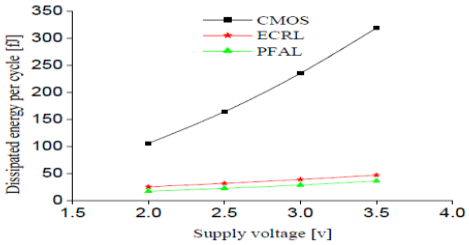

Fig. 16: Energy consumption per cycle versus supply voltage for an inverter at load capacitance = 20fF and frequency = 100 MHz.

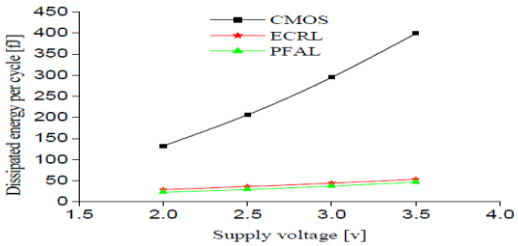

Fig.17: Energy consumption per cycle versus supply voltage for a 2:1 multiplexer at load capacitance = 20fF and frequency = 100 MHz..

VII. SIMULATION RESULTS

In this section I have describes the simulation results that were generated using DSCH3.l. First, we take the output for the schematic designed using DSCH 3.l. Then we convert the schematic into layout using the micro wind, and develop the layout design. From running the layout, we obtain various characteristics of the circuit including the V-I characteristics.

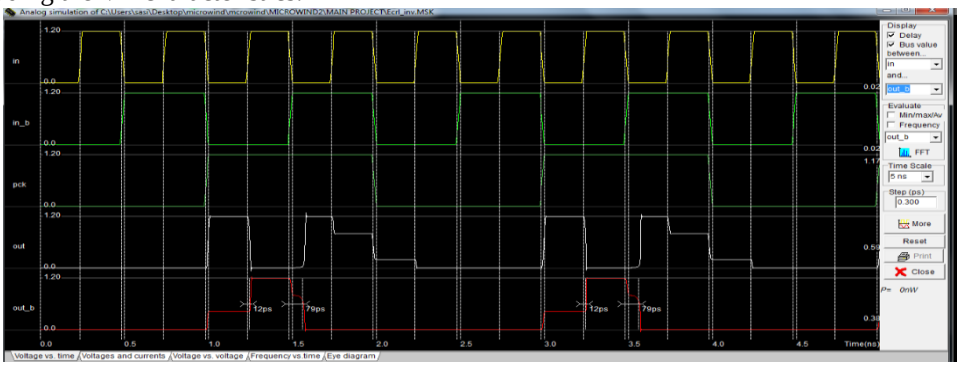

Fig 18: Simulated waveform of the ECRL inverter gate.

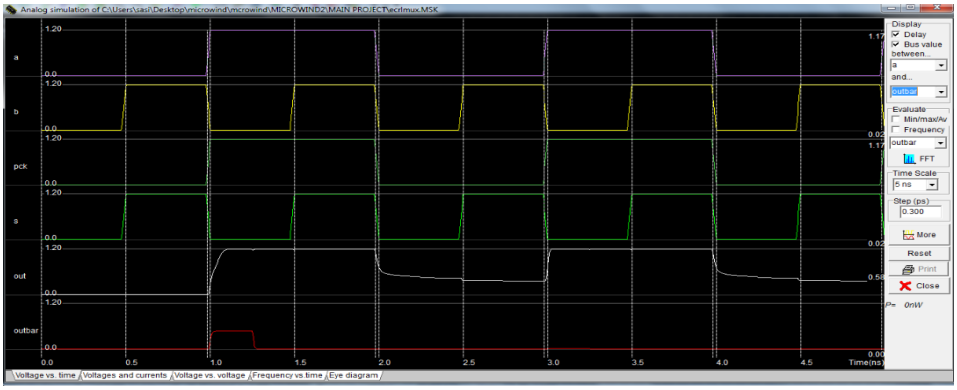

Fig 19: Simulated waveform of the ECRL multiplexer.

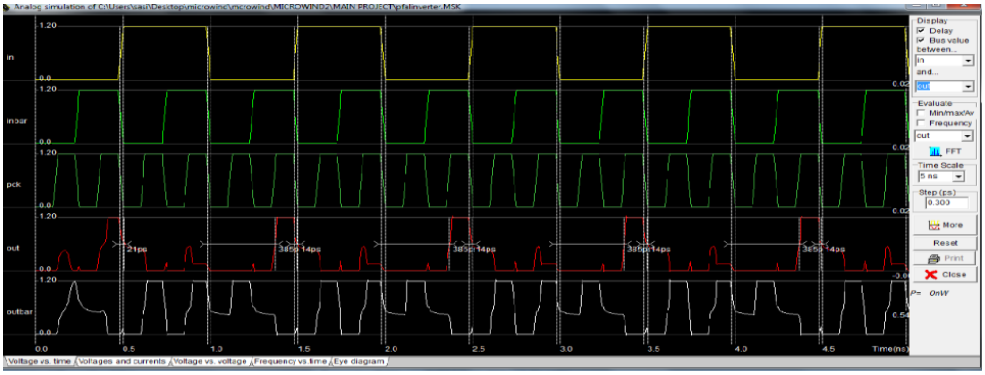

Fig 20: Simulated waveform of the PFAL inverter gate.

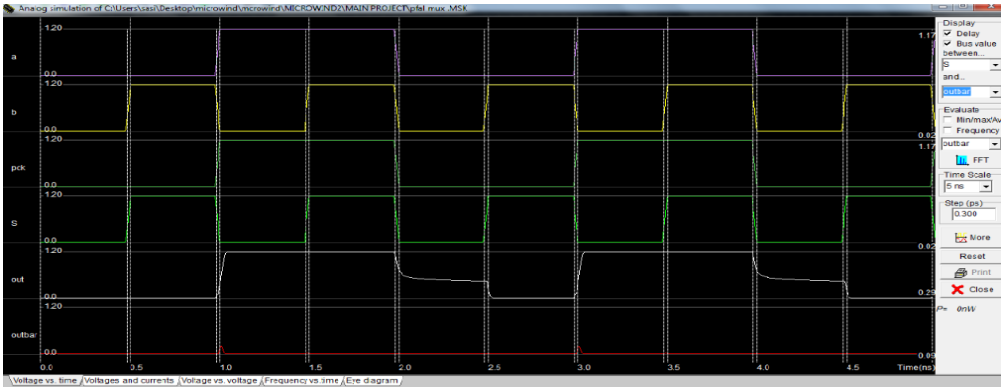

Fig 21: Simulated waveform of the PFAL multiplexer.

Table: 1.Comparission Of CMOS, ECRL And PFAL INVERTER

PARAMETER	POWER DISSIPATION	AREA (L*B)
CMOS INVERTER	3.703uw	6.415um^2
ECRL INVERTER	0nw	9.968um^2
PFAL INVERTER	0nw	19.98um^2

Table: 2.Comparission Of CMOS, ECRL And PFAL MULTIPLEXERS

PARAMETER	POWER DISSIPATION	AREA (L*B)
CMOS 2:1 MULTIPLEXER	17.753uw	125.01um^2
ECRL 2:1 MULTIPLEXER	0nw	129.11um^2
PFAL 2:1 MULTIPLEXER	0nw	146.11um^2

VIII. CONCLUSION

The different parameter variations against adiabatic logic families are investigated, which shows that adiabatic logic families highly depend upon its. But less energy consumption in adiabatic logic families can be still achieved than CMOS logic over the wide range of parameter variations. PFAL shows better energy shavings than ECRL at the high frequency and high load capacitance. Hence adiabatic logic families can be used for low power application over the wide range of parameter variations.

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