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Soft Switching Three Phase Push-Pull DC-DC Converter using Space-Vector PWM

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Abstract: **-** In this paper, a SV-PWM Three-phase push-pull DC-DC Converter has been proposed. By using Space Vector-PWM, the output of the converter is increased when compared with the Sine-PWM.The three-phase DC-DC conversion increases the power density, uses the magnetic core of the transformer more efficiently and it reduces the stress on switches and require small filters since the frequency is higher when compared to single-phase topologies. An active clamping technique is employed by connecting the primary side of the transformer to the three-phase full bridge of switches and a clamping capacitor. The energy from the leakage inductances is reused in this circuit, thus efficiency of the converter is increased. The applications include fuel cell systems, transportation and uninterruptable power supplies that can benefit from the advantages presented by this converter.

I. INTRODUCTION

The space vector modulation (SVM) technique uses a fixed frequency in synthesizing the reference vector, enabling many power applications to lower their switching losses. This clearly improves the efficiency, which is vital for high power applications such as DC/AC converters that are interconnected to power systems through transformers. While the SVM can be practically considered as a voltage based technique for the AC/DC converter output, one should obtain the reference voltage vector based on the required objectives of a certain application. Unlike the voltage-based SVM techniques, the current-based modulation techniques (e.g. hysteresis modulation) impose high losses despite their easy approach towards providing required reference current vector. Hence, the problem can be narrowed down to two problems for the SVM technique; first, provision of a three-phase reference voltage vector for the AC/DC converter output, and, second, making up the provided reference vector using the different switching status produced by a three-dimensional SVM technique. The instantaneous phase quantities *abc* are transferred to the so called αβo space to achieve a better distinction of zero sequence component for four-wire systems, in particular the active power filter.

Sinusoidal PWM has been a very popular technique used in AC motor control. This relatively unsophisticated method employs a triangular carrier wave modulated by a sine wave and the points of intersection determine the switching points of the power devices in the inverter. However, this method is unable to make full use of the inverter's supply voltage and the asymmetrical nature of the PWM switching characteristics produces relatively high harmonic distortion in the supply.

Three-phase systems are well known by their use in electric power generation transmission and distribution. The cost saving they provide by employing less material than single-phase systems assured success in these areas and led to three-phase rectifiers, inverters and also DC-DC converters. Industrial environments have an increasing need for high-efficiency DC-DC converters. Applications including distributed generation and uninterruptable power supplies generally count on single-phase DC-DC converters with big and heavy transformers.

II. PROPOSED SV-PWM THREE-PHASE DC-DC CONVERTER

A. Circuit Description

The circuit of the proposed Space Vector-PWM three-phase current-fed push-pull DC-DC Converter is shown in Fig 1.Switches S1' ,S2' and S3' and the capacitor Cg were added to the converter. It is to achieve active clamping. Inductances Ld1, Ld2 and Ld3 are responsible for maintaining the current during the commutation intervals. These inductances represent the sum of the leakage inductance of the transformer and an external inductance of the transformer, which is added to each phase if needed. The capacitors C1,C1',C2,C2',C3 and C3' are added. It gives appropriate dead time between main and complementary gate signals provide the possibility to operate with soft-switching.

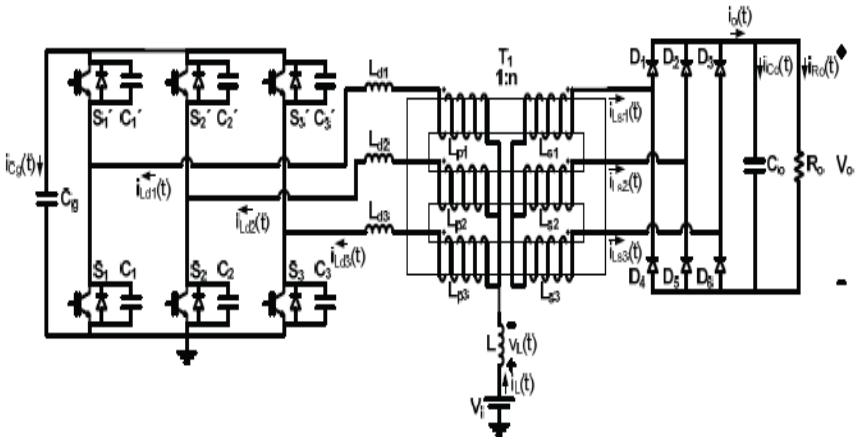

Fig.1 Circuit diagram of SV-PWM three-phase current-fed push-pull DC-DC converter

B. Simplified Circuit

The analysis can be simplified maintaining the same waveforms using the Fig 2 despite the complete circuit being shown in Fig 1.This circuit represents the non-isolated equivalent version of the proposed converter with current source input and voltage source output. The coupled three-phase reactor substitutes the transformer. The transformer was substituted by a coupled three-phase reactor. The voltages and currents from the secondary side are referred to the primary side in this circuit. During the description of the operation stages, the time intervals related to the commutations will not be considered due to being very short and interfering very little in voltage gain.

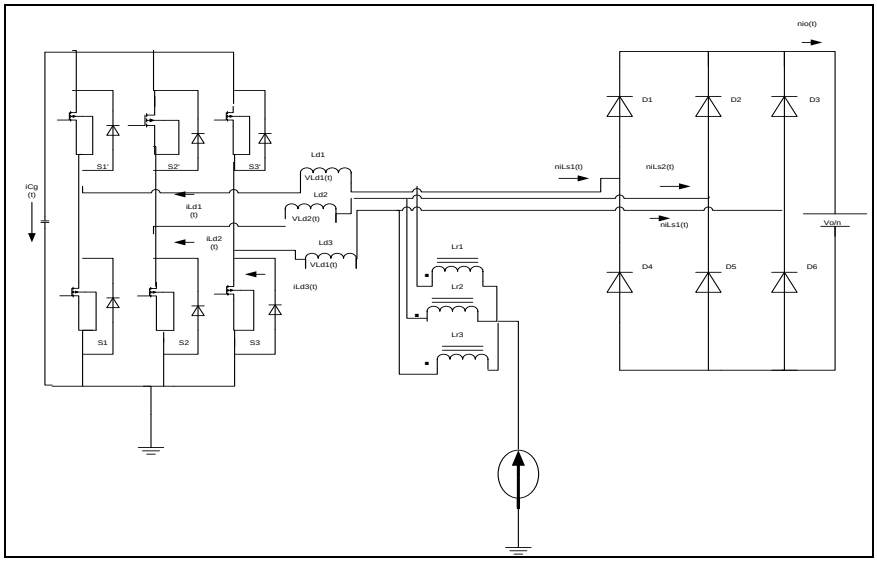

Fig. 2.Simplified non-isolated version of the active-clamped three-phase current-fed push-pull DC-DC Converter

C. Modulation

This PWM technique approximates the reference voltage V_{ref} by a combination of the eight switching patterns (V_0 to V_7) Coordinate Transformation (abc reference frame to the stationary d-q frame): A three-phase voltage vector is transformed into a vector in the stationary d-q coordinate frame which represents the spatial vector sum of the three-phase voltage.

The vectors (V_1 to V_6) divide the plane into six sectors (each sector: 60 degrees). V_{ref} is generated by two adjacent non-zero vectors and two zero vectors.S1 to S3 and S1' to S3' are the six power switches that shape the output, which are controlled by the switching variables a, a′, b, b′, c and c′. When an upper transistor is switched on, i.e., when a, b or c is 1, the corresponding lower transistor is switched off, i.e., the corresponding a′, b′ or c′ is 0. Therefore, the on and off states of the upper transistors S1', S2' and S3' can be used to determine the output voltage.

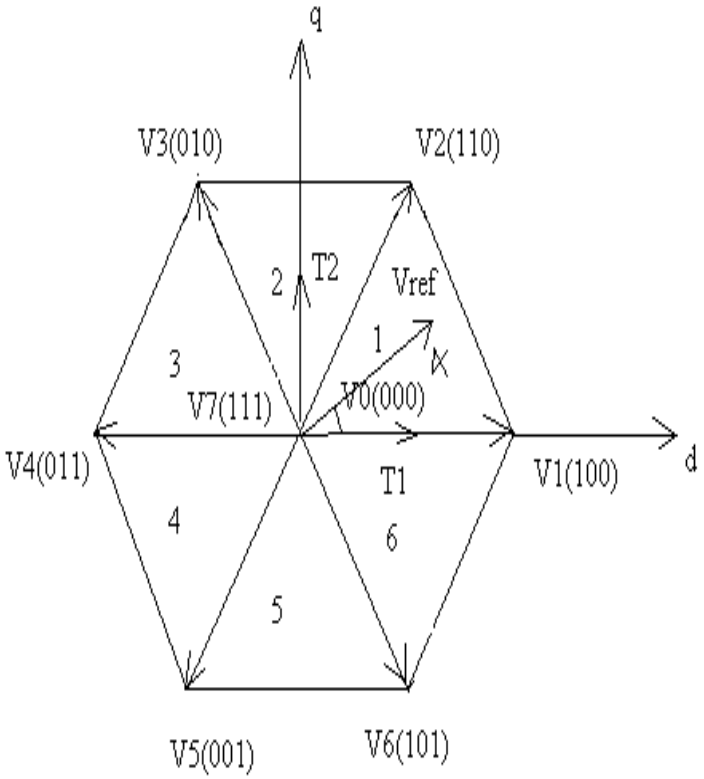

Fig.3 Basic switching vectors and sectors.

III. PRINCIPLE OF OPERATION AND VOLTAGE GAIN.

A. Operation

The Proposed converter has nine topological stages per switching period that can be described as follows:
Before the 1st stage; S1', S2 and S3 are already conducting.

1] 1st stage (t_0,t_1) - This stage starts when switch s1 is turned on. Before this stage,S1' was conducting and capacitor Cg was delivering energy. Current $i_{Ld1}(t)$,initially negative and equal to $-I_L/3$.It increases linearly through the diode of S1 as shown in Fig. 4(a) becomes positive and the value increases through S1 until reaching $I_L/3$ as shown in Fig. 4(b). The currents $iL_{d2}(t)$ and iLd3(t) decreases from $2I_L/3$ to $I_L/3$ through switches S2 and S3 respectively. The energy received by the load is from the commutation inductances through diodes D1,D5 and D6.The energy transfer from the source to load does not take place during this stage.

2] 2nd stage(t_1,t_2) – This stage starts when the currents $i_{Ld1}(t)$,$i_{Ld2}(t)$ and $i_{Ld3}(t)$ egual to $I_L/3$.The currents $i_{Ld1}(t)$,$i_{Ld2}(t)$ and $i_{Ld3}(t)$ remain at $I_L/3$ and the diodes of the rectifier remains in off condition. This is shown in Fig. 4(c). The energy is not transferred from source to load during this stage.

3] 3rd stage (t_2,t_3) – This stage starts when the switch S2 is turned off. The current $i_{Ld2}(t)$ decreases linearly from $I_L/3$ through the diode of S2' as shown in Fig. 4(d) and then it equals zero. It then starts to increase negatively until it reaches $–I_L/3$ as shown in Fig. 4(e). The energy from the commutation inductance is received by the clamping capacitor Cg as shown in Fig. 4(d). The capacitor Cg returns this energy as shown in Fig. 4(e). The currents $i_{Ld1}(t)$ and $i_{Ld3}(t)$ increases from $I_L/3$ to $2I_L/3$ through the switches S1 and S3 respectively. The source transfers the energy to the load through the diodes D2, D4 and D6.

The fourth topological stage and the seventh topological stages are similar to the first stage. The fifth topological stage and eight topological stages are similar to the second stage. The sixth and ninth topological stages are similar to the third stage. The difference is that the other switches are on. The switching period is completed after the ninth stage and the new period starts with the first stage.

The main voltages of the circuit during the described stages are shown in Table II. The main theoretical waveforms for region R3 are shown in Fig.3, whose time intervals are described by equations as presented in Table III. The waveforms plotted on Fig. 4 and the voltages presented in Table II correspond to the symbols presented previously on Fig.1 and Fig. 2.

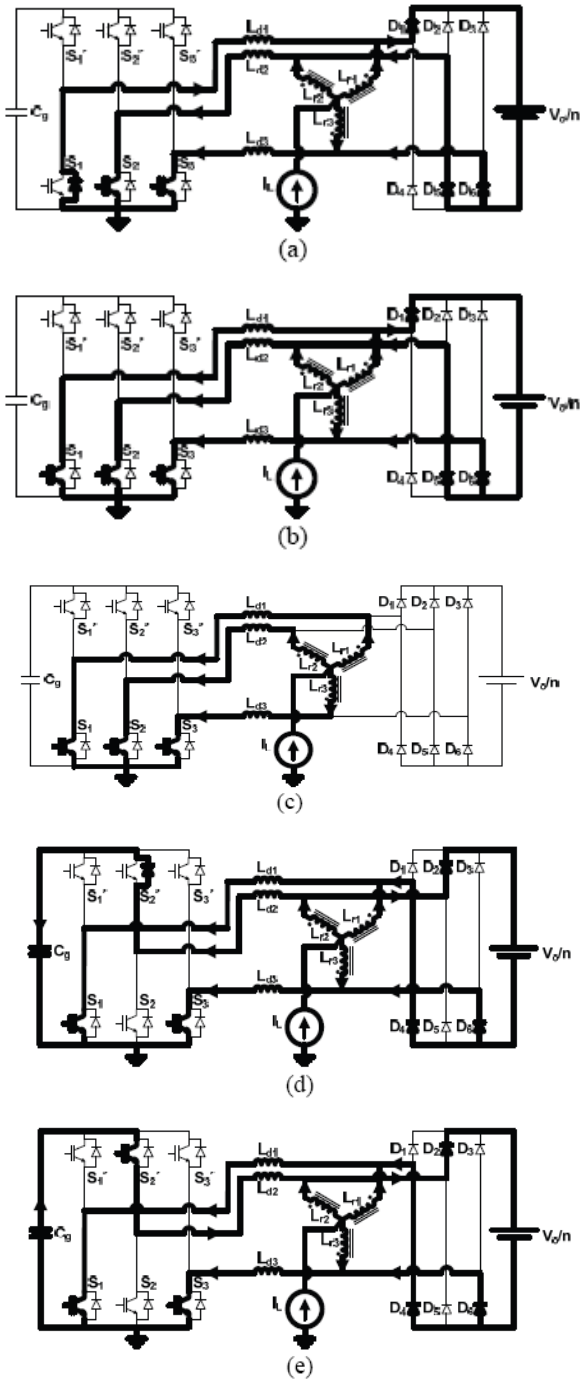

Fig 4. Topological Stages:(a) first stage – part 1, (b) first stage- part 2, (c) second stage, (d) third stage –part 1 (e) third stage-part 2

B. Voltage Gain

The average current through the clamping capacitor Cg is shown in equation (1)

$$\frac{3}{T_s} . \int_0^{(1-D)T_s} \left(\frac{I_L}{3} + \frac{V_{Ld\,2}}{L_d} . t \right) . dt = 0 \qquad (1)$$

The value of V_{Ld2} is substituted during the third stage from the table I in (1) and solving the integral gives (2)

$$V_{cg} - \frac{V_0}{n} = \frac{L_d . f_s . I_L}{1-D} \qquad (2)$$

The analysis with no losses in the converter are considered, equation (3) is valid.

$$V_i . I_L = V_0 . I_0 \qquad (3)$$

Substituting I_L from equation (3) in equations (2), (4) is found.

$$\frac{V_{Cg}}{V_o} = \frac{\bar{I}_0}{1-D} + \frac{1}{n} \qquad (4)$$

In which $\bar{I}_0$ is given by (5).

$$\bar{I}_0 = \frac{L_d . f_S . I_0}{V_i} \qquad (5)$$

The average voltage across the inductors is zero, so the average voltage across the switches S1, S2 and S3 is the input voltage Vi, and equation (6) can be written.

$$V_i = (1-D) . V_{Cg} \qquad (6)$$

Table II Main Voltages during each topological stage

Voltage	1st stage	2nd stage	3rd stage
VLr1(t)	$\frac{2}{3}\frac{V_0}{n}$	0	$-\frac{1}{3}\frac{V_0}{n}$
VLr2(t)	$-\frac{1}{3}\frac{V_0}{n}$	0	$\frac{2}{3}\frac{V_0}{n}$
VLr3(t)	$-\frac{1}{3}\frac{V_0}{n}$	0	$-\frac{1}{3}\frac{V_0}{n}$
VLd1(t)	$\frac{2}{3}\frac{V_0}{n}$	0	$\frac{1}{3}\left(V_{cg} - \frac{V_o}{(n)}\right)$
VLd2(t)	$-\frac{1}{3}\frac{V_0}{n}$	0	$-\frac{2}{3}\left(V_{cg} - \frac{V_o}{(n)}\right)$
VLd3(t)	$-\frac{1}{3}\frac{V_0}{n}$	0	$\frac{1}{3}\left(V_{cg} - \frac{V_o}{(n)}\right)$
VLdx(t)	0	0	$\frac{V_{cg}}{3}$

The equation
(6) leads to
the input clamping capacitor voltage gain in (7).

$$\frac{V_{Cg}}{V_i} = \frac{1}{1-D} \qquad (7)$$

Substituting equation (4) in equation (7) leads to the input output voltage gain(8).

$$q = \frac{V_0}{V_i} = \frac{n}{(1-D)+n\,.\bar{I}_0} \qquad (8)$$

Equation (8) represents the voltage gain of the proposed three-phase current-fed push-pull DC-DC converter with active clamping in region R3.

Table III Equations for Time Intervals of Fig.4

First stage	$\Delta t_1 = \frac{n.L_d.I_L}{V_0}$
Second stage	$\Delta t_2 = \frac{T_s}{3} - \Delta t_1 - \Delta t_3$
Third stage	$\Delta t_3 = (1-D).T_s$

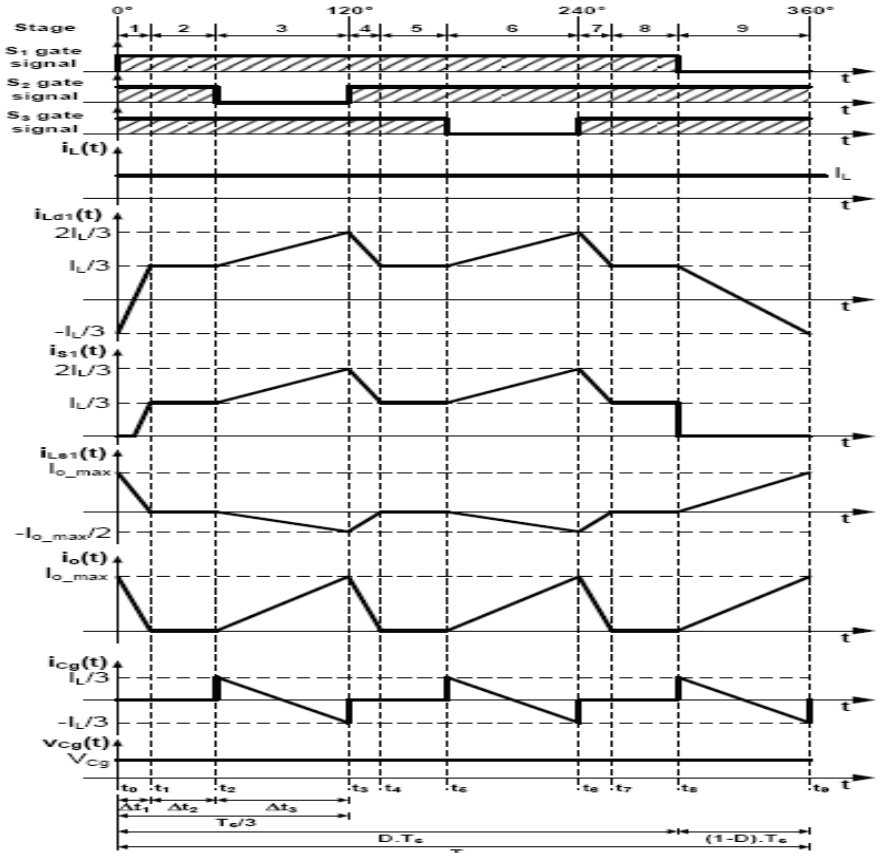

Fig.4.Main theoretical waveforms for region R3

IV. SIMULATION RESULTS

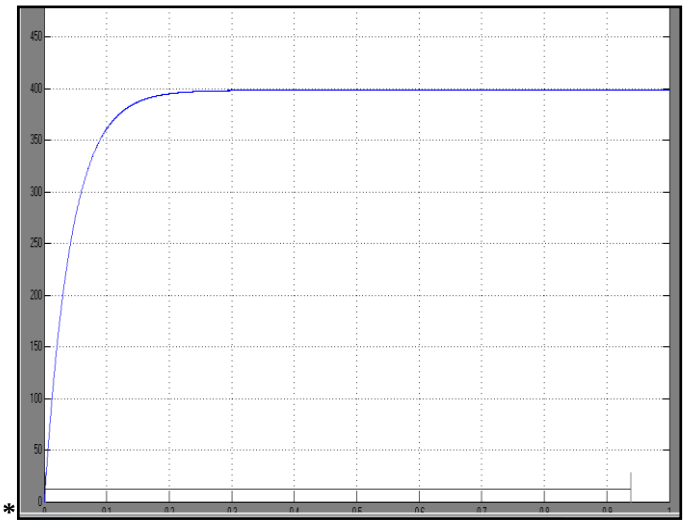

Fig.6 Output voltage of ZVS-PWM three-phase current-fed push-pull DC-DC Converter

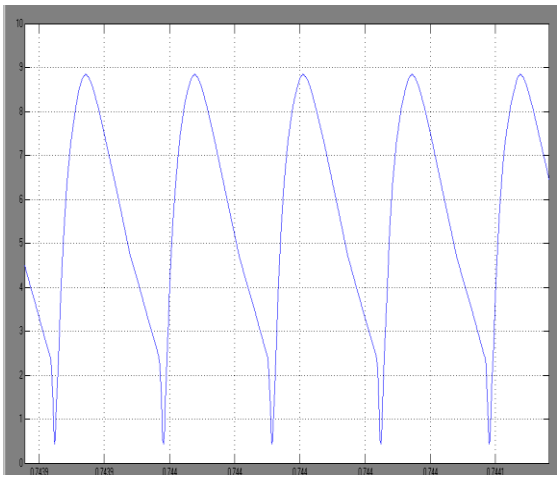

Fig.7 Output current of ZVS -PWM three-phase current-fed push-pull DC-DC Converter

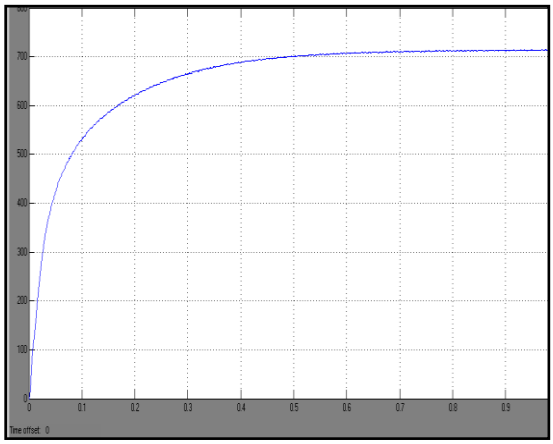

Fig.8 Output voltage of the Space-Vector-PWM Three Phase current-fed Push Pull DC-DC Converter

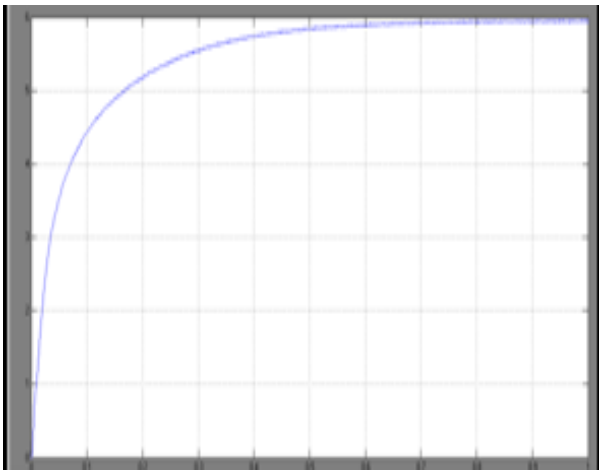

Fig.9 Output current of the Space-Vector-PWM Three Phase current-fed Push Pull DC-DC Converter

Fig 6 shows output voltage of ZVS Sine-PWM three-phase current-fed push-pull DC-DC converter. The output voltage has been obtained as 400V. Fig 7 shows output current of ZVS Sine-PWM three-phase current-fed push-pull DC-DC Converter. The output current has been obtained as 9A but has ripples in it. Fig 8 shows output voltage of Space vector-PWM three-phase current-fed push-pull DC-DC Converter. The output voltage has been obtained as 700V. Fig 9 shows output current of ZVS Sine-PWM three-phase current-fed push-pull DC-DC Converter. The output current has been obtained as 6A but the ripples are reduced by using this technique and have got high output when compared with the Sine-PWM.Thus the advantages of Space vector PWM can be effectively utilized in this paper.

V. CONCLUSION

In this paper, a Space Vector –PWM Three phase Current-fed Push-Pull DC-DC Converter has been proposed. In this paper, a SV-PWM Three-Phase Current-Fed Push-Pull DC-DC Converter has been proposed.The operation stages were described and the main waveforms were plotted. The equations of voltage gain and equations involving the commutation parameters were derived to help the design process. By using SV-PWM instead of Sine-PWM, the output of the converter was increased and the ripple in current was also reduced. The proposed converter circuit was verified by Mat lab/Simulink with detail models.

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