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A Vector Control Method for Three-Stage n-Level Cascaded Inverter with Performance Measurement

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Abstract: – This paper contains a three stage n-level hybrid inverter circuit and its control method. The three inverter stages are the high-, medium-, and low-voltage stages. The high voltage stage is a conventional three phase inverter which is used inorder to reduce the losses. The medium and low voltage stages are made of cascaded H-bridge inverters. The low voltage stage is controlled by using space-vector modulation for optimized efficiency and excellent output performance. In this, the number of inverter levels can be varied from 2 to 18 depending upon the application. The harmonic distortion gets reduced as the number of levels increases. Thus the inverter can be operated for any number of levels using this method. The simulation model of the system is created in the MATLAB/SIMULINK environment.

I. INTRODUCTION

The voltage source inverters produces an output voltage or current of levels either 0 or $\pm V_{dc}$. They are also known as two level inverters. The quality of the output voltage or current waveform can be improved with minimum amount of ripple content by making use of the high switching frequency along with various pulse width modulation (PWM) strategies. The two level inverters have some limitations in operating at high frequency, in high power and high voltage applications. This is mainly due to the switching losses and constraints of the device ratings.

The multilevel inverters have several advantages in this situation. They are widely used in power industry and are used in reactive power compensation. With multilevel structure, it is easier to produce a high power high voltage inverter because of the way by which the device voltage stresses are controlled. The power rating of the device can be increased without increasing the ratings of the individual devices which increases the number of voltage levels in the inverter. The unique structure of the multilevel inverter allows them to reach high voltages with low harmonics. As the number of voltage levels increases, the harmonic content of the output voltage waveform decreases.

Multilevel inverters have been widely recommended for medium and high power applications. The cascaded H-bridge inverters have several advantages compared to other MLI topologies due to its modular structure and the linear relationship between the number of inverter elements and the levels. The main disadvantage of CHB inverter is the use of large number of isolated dc supplies. Supplying the CHB cells with different dc voltages provides higher number of levels for the same circuit topology. When the cascaded cell dc voltages are in a ratio-3 geometric sequence, the maximum number of levels can be achieved. For high frequency pulse width modulation (PWM) controls, the ratio-3 dc sourced inverter is not appropriate. This is because the high voltage stage is subjected to high switching frequency. Asymmetrical inverters also suffer from the need for large number of isolated dc supplies similar to other CHB inverters. The number of dc sources can be reduced by cascading smaller dissimilar inverter circuits resulting in hybrid MLIs. In this paper, a three-stage inverter circuit has been used and the use of ratio-3 related dc sources maximizes the number of levels, thereby, contributing to output waveform with reduced number of harmonics.

In this paper, the topology is selected as a trade-off between the cost and the number of levels. MLI can be controlled either by high frequency or by low frequency switching. Carrier comparison PWM strategies, space vector modulation and the carrier based SVM are examples of high frequency switching. These are mainly used for symmetrical topologies. The low frequency control methods include the voltage vector approximation, selected harmonics elimination etc. For asymmetrical MLIs, the voltage vector approximation is used widely. In this, paper the high voltage stage is operated in square wave mode, the medium voltage stage is operated in low frequency mode and the low voltage stage is controlled by SVM.

II. INVERTER TOPOLOGY

The inverter circuit is shown in the figure1. It consists of a six switch conventional inverter which acts as the high voltage side. The output from this is connected in series with two single-phase full-bridge inverters. The main and H-bridge inverters are fed by dc sources $9V_s$, $3V_s$ and V_s respectively. This provides an 18-level inverter. The high voltage stage is provided with only one dc source which operates with reduced current ripple when compared with the three dc sources of CHB design. Therefore, reduction in the number of dc sources and losses will be obtained.

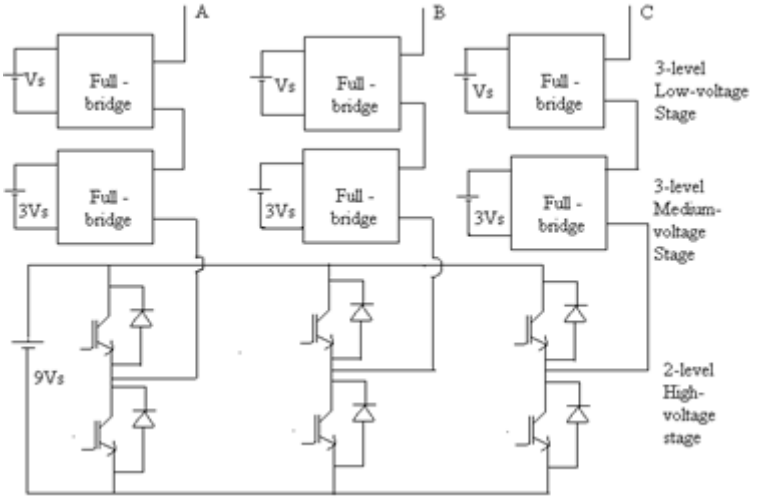

Fig1. Three-stage 18-level hybrid MLI topology

In order to understand the significance of this design, consider the reference point 0V as shown in fig.1. assuming that the output voltage at point A has to be changed between $4V_s$ and $5V_s$. The method for producing these voltage levels from these three stages includes adding up ($0+3V_s+V_s$) and ($+9V_s-3V_s-V_s$) respectively. If the reference voltage has to be located between these two levels, then there will be a carrier frequency which switches between these two levels. The algorithm used in this paper reduces this type of switching.

The switching variables of the inverter can be denoted by { (x_{abc}), (y_{abc}),(z_{abc}) in which x is a binary digit whereas y and z are trinary digits. These variables denote the states of the three stages of the inverter. The output voltage vector can also be represented in terms of the switching state. Line voltages can be represented in terms of the switching variables as:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = 9V_S \begin{bmatrix} x_a - x_b \\ x_b - x_c \\ x_c - x_a \end{bmatrix} + 3V_S \begin{bmatrix} y_a - y_b \\ y_b - y_c \\ y_c - y_a \end{bmatrix} + V_S \begin{bmatrix} z_a - z_b \\ z_b - z_c \\ z_c - z_a \end{bmatrix}. \quad (1)$$

Phase voltages of the Y-connected load can be represented as:

$$\begin{bmatrix} \nu_{an} \\ \nu_{bn} \\ \nu_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} \nu_{ab} - \nu_{ca} \\ \nu_{bc} - \nu_{ab} \\ \nu_{ca} - \nu_{bc} \end{bmatrix}$$

$$= \frac{V_s}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} 9x_a + 3y_a + z_a \\ 9x_b + 3y_b + z_b \\ 9x_c + 3y_c + z_c \end{bmatrix}. \quad (2)$$

The voltage vector diagram of the three stage inverter can be drawn by two superposition steps. First, the vector diagram of the high voltage stage is drawn which contains seven vectors. Then the vector diagram of the three level medium voltage stage inverter is drawn at the end of the above drawn vectors. Finally, the vector

diagram corresponding to the low voltage stage has to be superimposed at the end of the resultant vectors. This is shown in fig.2.

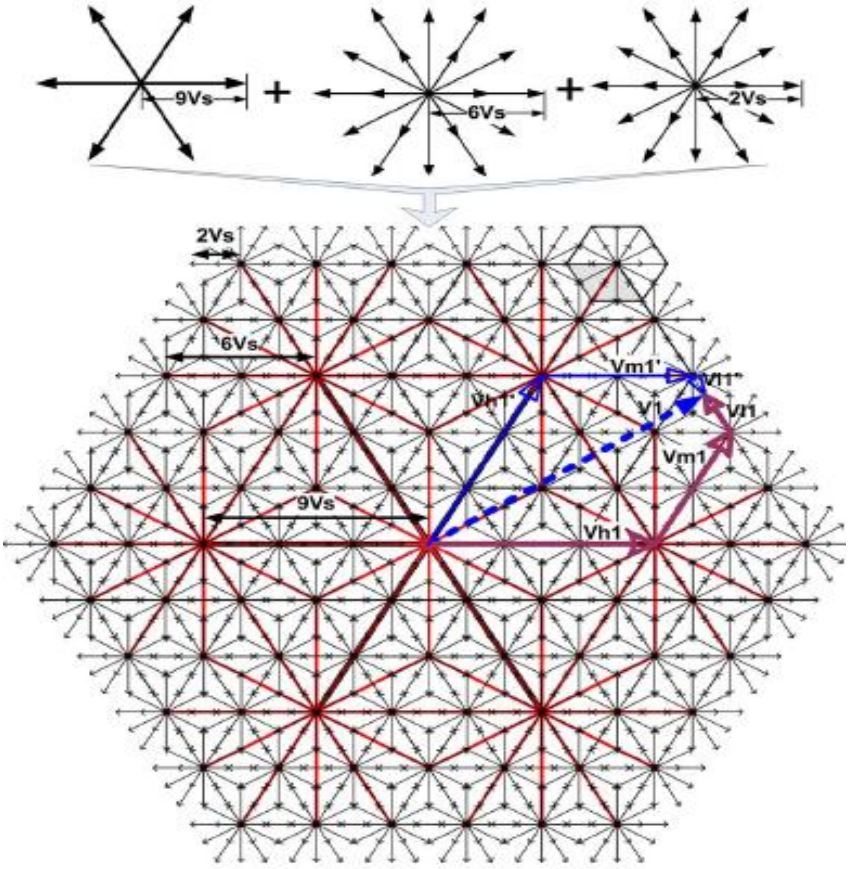

Fig 2. Voltage vectors of the 18-level inverter

The g-h coordinate system can be used to represent the voltage vectors in the control technique explained in this paper. This system is closely related with the inverter voltage vectors.

III. CONTROL METHODOLOGY

The 18 level inverter vectors can be represented by the addition of the three vectors which belongs to the three stages. Most of the 18 level inverters can be represented by the combination of the three stage voltage vectors. This can be seen in the example for the voltage vector V1 as shown in fig 2. To achieve the fundamental frequency operation at high voltage stage, the high voltage state has to be hold as such till the reference vector can be obtained by adding medium and low vectors to this high voltage state vector. The medium and low stage vectors can be superimposed on a given high state vector and the hexagonal area obtained can be defined as domain. The high voltage stage vectors has got seven domains. The area covered by the low voltage stage vector can be represented by nineteen hexagons. The selection of the medium voltage state determines the hexagons covered by the SVM control of the low voltage stage. We have to define a modified domain for avoiding any sort of distortion that arises due to the presence of reference vector on the areas which are not in the control of the SVM low voltage stage.

The control algorithm can be represented by means of the flow diagram as shown in fig 3. The reference vector has to be sampled with a sampling rate of T_s. The controller has to determine the next switching states for all the three stages during this sampling period. The three vectors which are nearest to the low stage reference is determined by the low voltage stage routine. It also determines the corresponding duty ratios. The reference vectors have to be first converted in to the g-h components. This g-h values has to be compared with the first quadrant portion of the domain and thereby checking whether the reference vector is located in the

current high (medium) voltage state. If it is located in the region we are checking, then x_{abc} (y_{abc}) has to hold its value during the next switching interval.

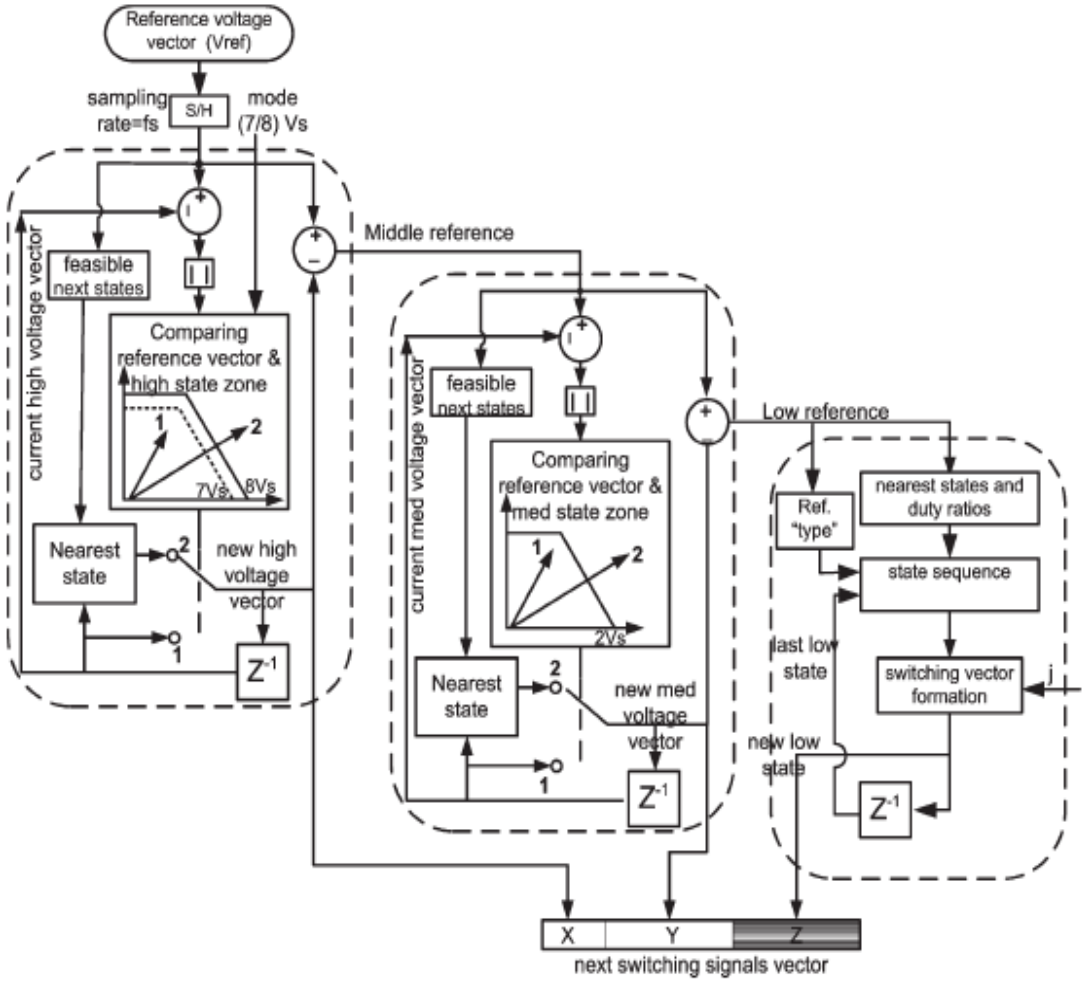

Fig 3. Flow diagram of the control algorithm

If the reference voltage vector is not present in the current state domain, then the new high (medium switching state has to be determined. The procedure for this is explained as follows:

1) The reference vector will be first compared with the seven high (19 medium) state domains. Then a short list of the feasible states for the next switching period will be generated. The feasible state can be defined as any state that has a reference vector located in its domain.
2) The next high(medium) state will be from the list if it has one element.
3) If not so, the feasible state list will be compared with the initial state and the next state will be taken as the state with minimum difference.
4) The low voltage stage comprises of a three level inverter. The control routine is described below:
5) The three inverter states which are nearer to the reference states and their corresponding duty ratios has to be calculated.
6) The inverter has to be operated in four switching states for realizing the reference vector. The first and last switching states are equivalent.

IV. SIMULATION RESULTS

The output obtained by the simulation of the algorithm presented is shown in fig 4. It shows the output of an 18 level inverter and the corresponding THD value obtained is also shown in fig 5 which is found to be 10.16%. Fig 6 and 7 shows the output of 8 level inverter and its THD value respectively.

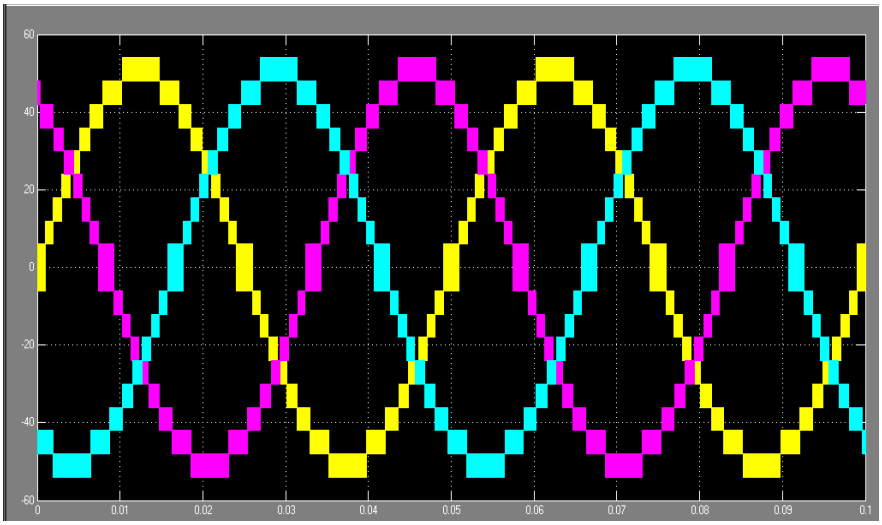

Fig 4. Output for 18 level inverter

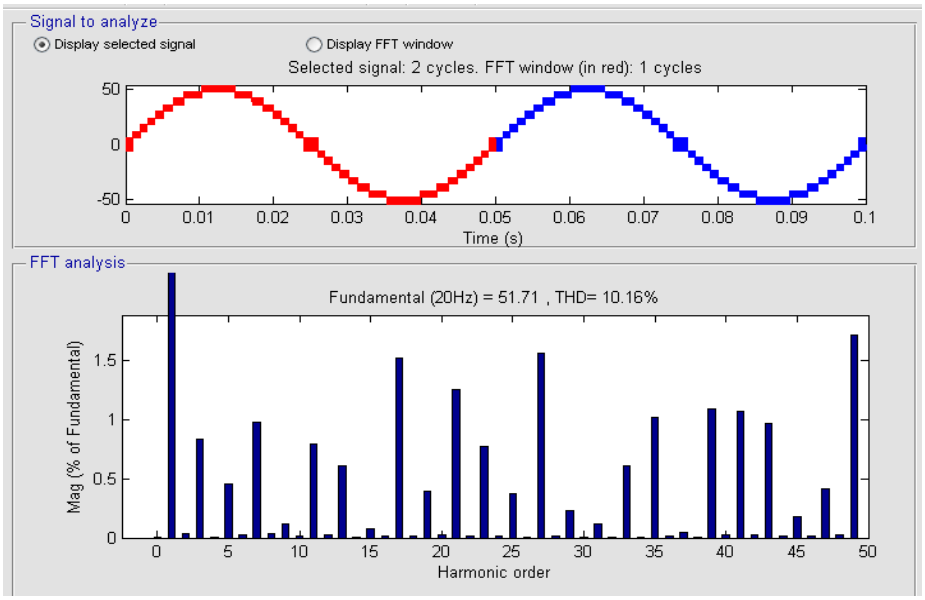

Fig 5. THD value for 18 level inverter

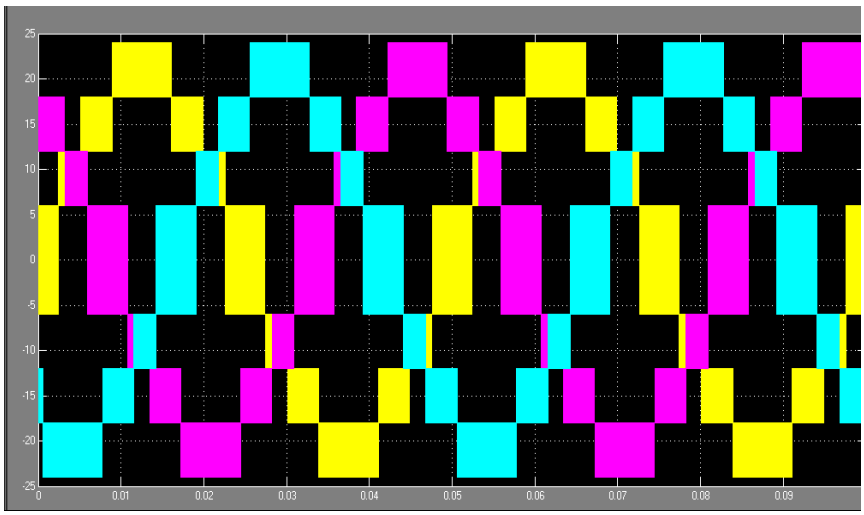

Fig 6 Output of an 8 level inverter

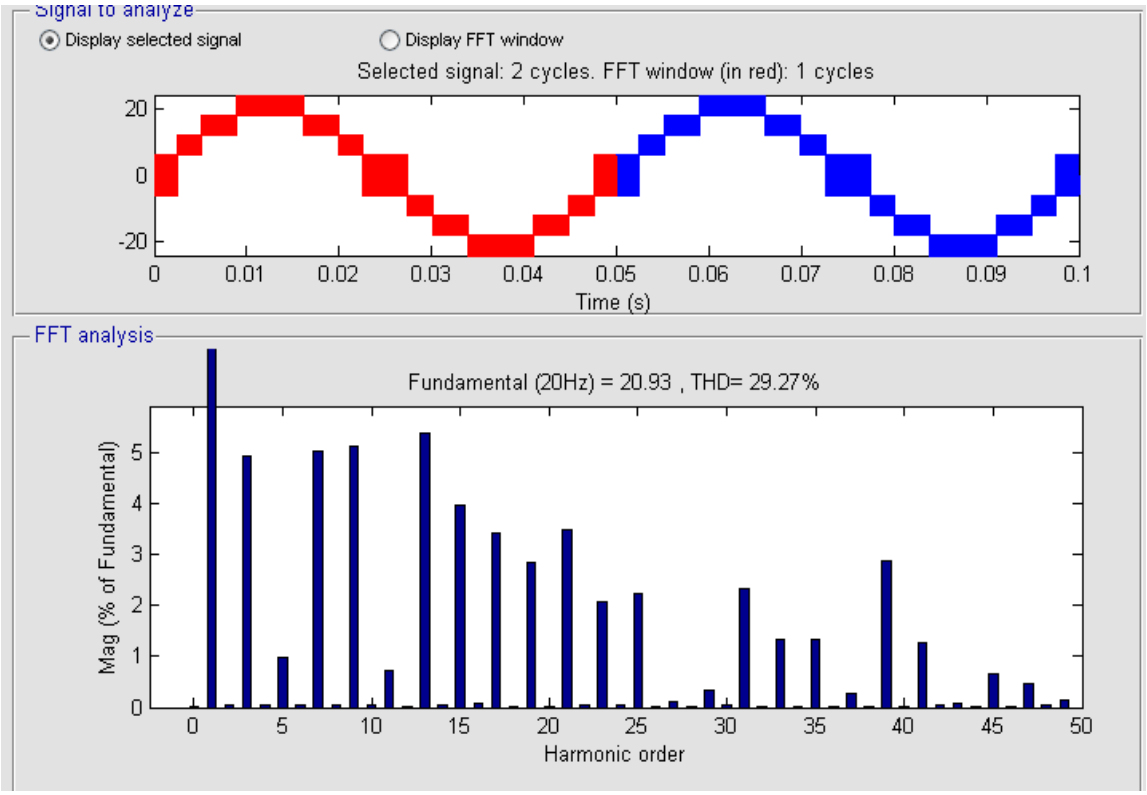

Fig 7 THD value for 8 level inverter

The output obtained in case of an 18 level inverter contains less harmonics and is nearly a sinusoidal waveform. It can be seen that the harmonics for lower order is higher and hence the waveform willnot be a perfect sinusoidal one. As we increase the number of levels, the output will become more perfect sine wave but the increase in levels needs more number of switches which will increase the cost. The THD values obtained for different inverter levels is shown in the table 1.

Number of levels	**THD Values (%)**
2	2259.57
4	101.38
6	45.18
8	29.27
10	21.47
12	16.91
14	13.91
16	11.74
18	10.16

Table 1. THD values for different levels

V. CONCLUSION

In this paper, a control method for an inverter has been proposed and it has been implemented for hybrid cascaded inverter. In this the output can be obtained with less harmonics, therefore it can be implemented for high power applications. Since in this proposed technique, the number of inverter levels can be specified, it has the advantage of application specific which means less harmonic or comparatively more harmonic sine wave can be generated depending upon the requirement. The proposed method is verified by MATLAB/ SIMULINK models.

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