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Three Level Three Phase Cascade Dual-Buck Inverter With Unified Pulsewidth Modulation

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Abstract:- This paper presents a three phase voltage source dual buck inverter using unified PWM technique. This technique enhances the system reliability. It is a hard switching voltage source inverter. This topology uses power MOSFET as the active device and as a result it has lower switching losses and it can be designed at higher switching frequencies to reduce current ripple and size of passive components. The unified PWM technique reduces the computational burden in real time implementations by making use of a digital signal processor. Different PWM methods like Sinusoidal PWM, Space Vector PWM and Discontinuous Space Vector PWM (DSVPWM) can be applied to a three phase dual buck inverter. It does not need dead time and has no shoot through concerns. A three level cascaded dual buck inverter is also controlled using unified PWM technique.

I. INTRODUCTION

The standard half-bridge or full-bridge inverter is a typical voltage source inverter (VSI) with two active switches in one phase leg. It needs dead time to prevent shoot-through problems between the switches in one leg. Because of dead time effect, the output waveforms can be distorted and the equivalent transferred energy of pulse-width modulation (PWM) is reduced. At some fault conditions, even with added dead time, shoot-through is still the reason for dominant failure of the circuit. In addition, with higher dc bus voltage operation, this standard inverter cannot simply employ power MOSFETs as the active switches due to the reverse recovery problem of the body diode of MOSFETs.

To utilize the benefits of power MOSFETs, such as lower switching loss, resistive conduction voltage drop, and fast switching speed which reduces the current ripple and the size of passive components, the dual buck inverter had been proposed. The dual-buck inverter typically consists of two buck inverters with one operating at the positive half-cycle while the other one working at the negative half-cycle. The dual-buck type inverters do not need dead time, and they totally eliminate the shoot-through concerns, thus leading to greatly enhanced system reliability. It can be hard switched because the body diode of MOSFET never conducts, and the external diodes can be independently selected to minimize switching losses.

This paper proposes a three level cascaded dual buck inverter in which two three-phase dual-buck inverter shown in Fig. 1 are connected in series.. It is hard-switching-based, but it can incorporate power MOSFETs as the active switches. The number of switches is the same as that of the standard three-phase voltage source inverter using insulated-gate-bipolar-junction-transistors (IGBTs). It does not need dead time since there is only one active switch per leg. It can be modulated with unified pulse width modulation to further reduce the switching losses and make use of the dc bus voltage completely.

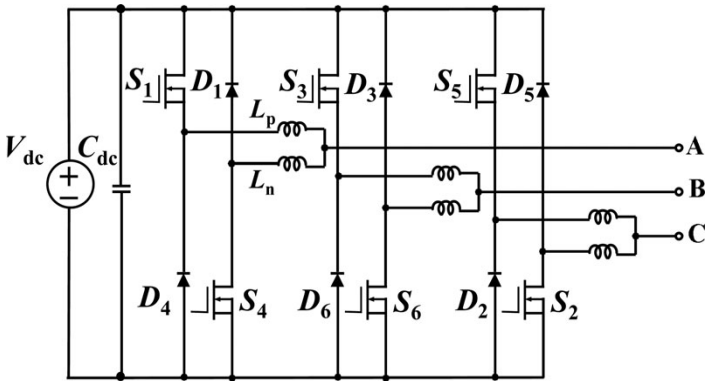


Fig. 1. Three-phase dual buck VSI with MOSFET

A unified pulse width modulation is adopted in order to modulate the three-phase dual-buck inverter. This method has less computational burden compared to traditional space vector PWM (SVPWM) sector

calculation, when implemented by a digital signal processor (DSP). The unified pulse width modulation is modified to use the current reference to generate the gate signals because of the unique operation principle of the three-phase dual-buck inverter. Different pulse width modulation methods are the special cases of the unified technique. It includes sinusoidal pulse width modulation (SPWM), space vector pulse width modulation (SVPWM), and discontinuous space vector pulse width modulation (DSVPWM). This paper presents the basic operation principle of the proposed dual buck inverter and it analyses the unified pulse width modulation technique applied to the three-phase dual-buck inverter and three level three phase cascade dual buck inverter`. It uses the closed-loop controller design with proportional-integral (PI) and proportional (P) controllers.

II. DUAL BUCK INVERTER

The three-phase dual-buck inverter has been shown in Fig. 1.The PWMs for the active switches are determined by the phase output current even though it is a voltage source inverter.

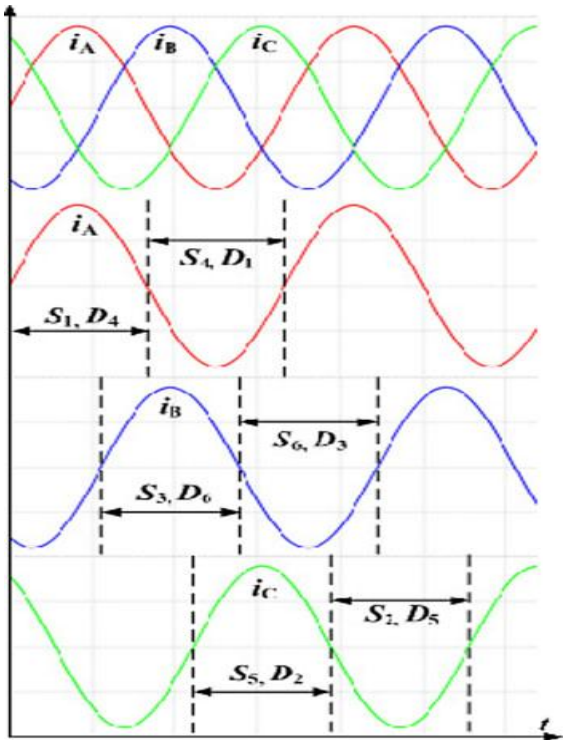


Fig. 2. Relation between phase current and conducting devices.

Fig. 2 shows the relation between the operation of switches and the polarity of phase current. For example take phase A, when i_A is positive, S_1 and D_4 are the conducting devices and when i_A is negative, S_4 and D_1 are the conducting devices. The operation principle is similar for phases B and C.

Shoot-through is no longer possible since there is only one active switch per leg. Therefore, the reliability of the three-phase dual-buck inverter is much higher when compared to traditional voltage source inverters. No dead time is needed because when S1 operates, S4 is always OFF and vice versa. Without the dead-time effect, the output waveforms are more sinusoidal and the energy is transferred more completely. Since the power MOSFET and diode can be selected independently, the system efficiency can be further improved.

III. UNIFIED PWM ANALYSIS

In many industrial applications, control of the output voltage of inverters is often necessary. The most efficient method of the controlling the gain and output voltage is to incorporate pulse width modulation control within the inverters.

In order to modulate the three-phase dual-buck inverter, a unified pulse width modulation is adopted. Unified pulse width modulation method has much less computational burden compared to traditional space vector PWM (SVPWM) sector calculations. Due to the unique operation principle of the three-phase dual-buck inverter, the unified PWM is modified to use the current reference to generate the required gate signals. Different PWM methods can be considered as special cases of the unified pulse width modulation technique, including sinusoidal pulse width modulation (SPWM), space vector pulse width modulation (SVPWM), and

discontinuous space vector pulse width modulation (DSVPWM). By using unified PWM methods, SVPWM and DSVPWM can be equivalently generated using triangle carrier comparison like SPWM. This will greatly reduces computational burden and is very easy to implement by digital signal processor.

Three-phase dual buck inverter is a hard switching VSI even though MOSFETs are used to cut down switching losses. Therefore, it is better to further reduce the switching loss by incorporating discontinuous space vector pulse width modulation.

Traditionally, the space vector PWM methods need to do trigonometric calculation and perform recombination of actual gating times, which is unfavorable for real-time implementation by a digital signal processor. Using unified pulse width modulation methods, space vector PWM and discontinuous space vector PWM can be equivalently generated using triangle carrier comparison like sinusoidal PWM which greatly reduces computational burden and is very easy to implement by DSP. Fig. 4 shows the unified PWM generation block diagram. Based on the current reference polarity, the switch to which PWM is applied is selected. shows the block diagram of unified pulse width modulation generation. The phase duty cycles da, db, and dc are provided by a closed-loop controller. The injected zero sequence duty cycle d_{zs} is generated by the following equation

$$d_{zs}= -[(1-2k_0)+k_0.d_{max}+(1-k_0).d_{min}] \quad (1)$$

Where dmax = max (da, db, dc) and dmin = min (da, db, dc).

k_0 is the pulse width modulation determination factor.

Under this unified PWM scheme when dzs=0, the output pulse width modulation will be sinusoidal pulse width modulation (SPWM). When $k_0 = 0.5$, the output pulse width modulation is space vector pulse width modulation (SVPWM); when k0 follows the relation in (2), the output PWM is discontinuous space vector modulation (DSVPWM).

k0 = 1 , J >0

k0= 0 , J<0 (2)

$J = \max (i_{aref}, i_{bref}, i_{cref}) + \min (i_{aref}, i_{bref}, i_{cref})$.

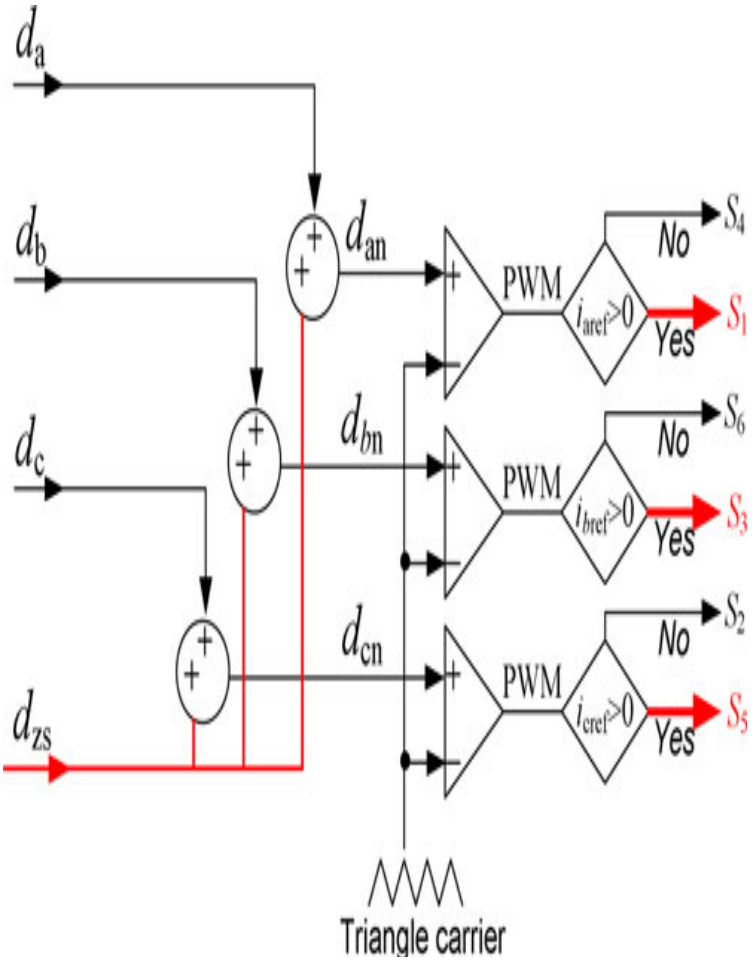
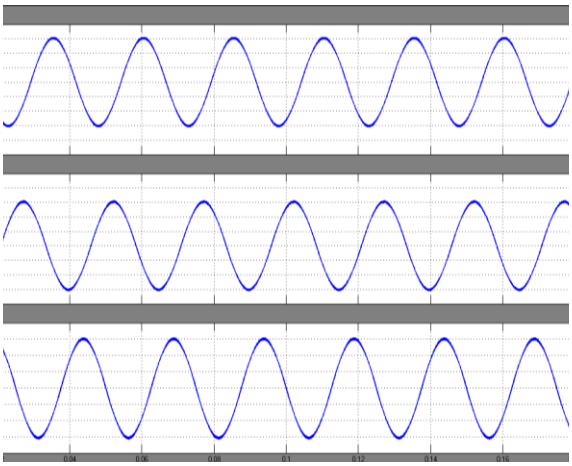


Fig.4. Unified PWM generation block diagram

IV. RESULTS

In normal operation, the dual buck inverter totally eliminates the shoot-through problems as discussed in section II. How ever, the gating signals for S1 and S4 might be high at the same time under some fault conditions. During this condition Lp and Ln are inserted in the shoot-through path through the dc power supply, and it will limit the di/dt of the devices, and thus the failure rate of the circuit is decreased and provide enough time for the protection circuit.



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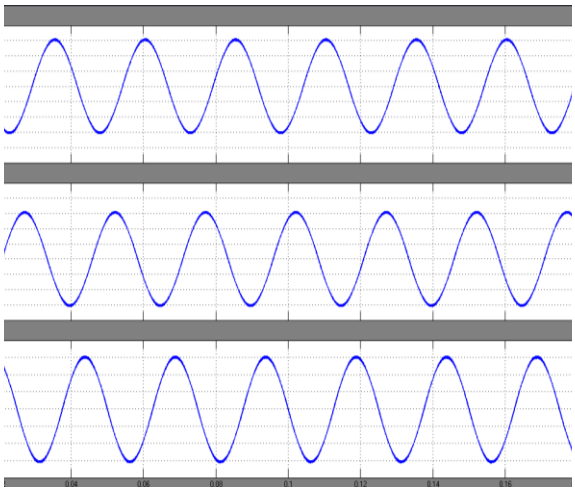

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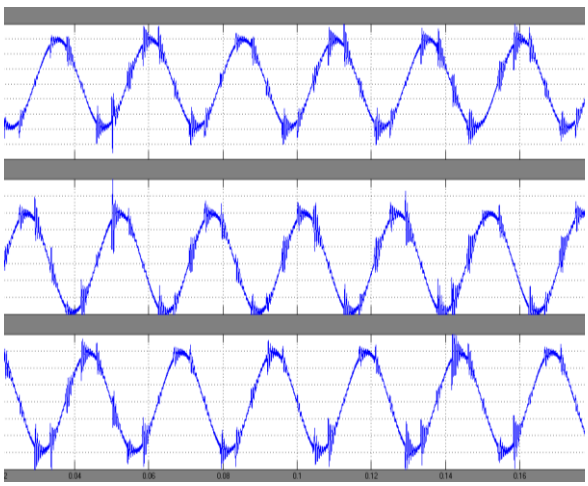
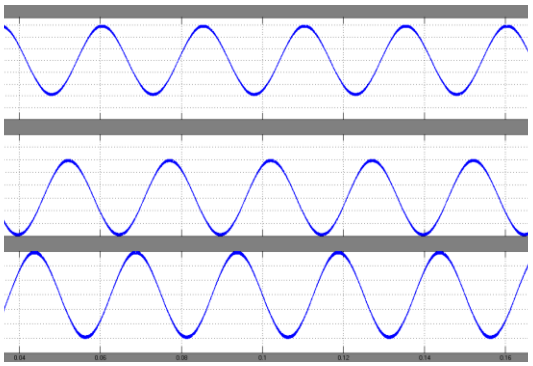
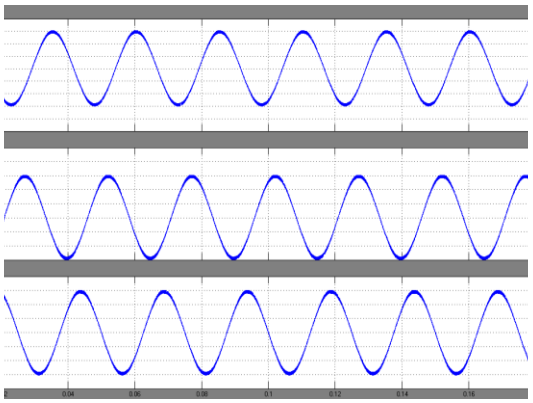


(c)

Fig. 5 Three phase output voltage waveforms at dc bus voltage 380V. (a) SPWM. (b) SVPWM. (c) DSVPWM.



(a)



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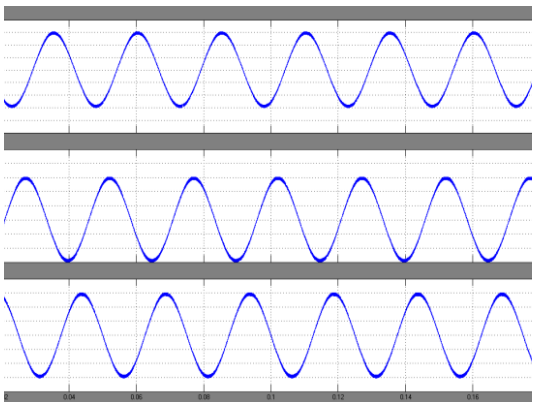

(c)

Fig.6. Three phase output voltage waveforms of 3 level inverter at dc bus voltage 380V. (a) SPWM. (b) SVPWM. (c) DSVPWM.

Fig. 5 shows three-phase output phase-to-neutral voltage waveforms of a three phase dual buck inverter for SPWM, SVPWM, and DSVPWM under dc bus voltage 380 V. The output voltage is 120 V.

Fig.6 shows three-phase output voltage waveforms of a three level cascaded dual buck inverter for SPWM, SVPWM, and DSVPWM under dc bus voltage 380V with duty cycle 0.9. Space vector PWM and discontinuous SVPWM can run at lower bus voltage, with the help of extended duty cycle, further reducing switching losses. By using a multilevel inverter the harmonics is further reduced.

V. CONCLUSION

Three level cascaded three phase dual-buck inverter with unified pulse width modulation has been proposed. The dual buck inverter eliminates the possibility of shoot-through problem and the need for dead-time. Therefore this dual buck inverter improves the reliability. Using unified pulse width modulation the computational load on the digital signal processor. It used power MOSFETs as active switches, and can achieve lower switching losses with the help of using power MOSFETs.

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