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A Review of Evolution comes in Non Volatile Semiconductor memories like SONOS with the role of high k-dielectric material

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***Abstract*: -** SONOS type memories have many advantages of lower operating voltages, excellent endurance and compatibility with standard metal oxide semiconductor (CMOS) technology. However, data retention and operating speed are limitations in such kind of memories. This paper reviews the evolution comes in the basic architecture of non-volatile memory devices like MNOS,SNOS and SONOS with the purpose of using high k-dielectric material in each layer like tunneling layer, charge-trapping layer and blocking layer. Additionally, here we discuss different dielectric materials (HfO_2 or Al_2O_3/oxy-nitride gate dielectrics) and their properties like bias-temperature instabilities, radiation response and annealing characteristics used in such kind of non-volatile semiconductor memories. This will help to understand the contributions of oxide, interface and border-trap charges in charge buildup. This literature survey can provide insight into the fundamental charge trapping properties of high-k dielectrics and help to predict the long-term radiation response and reliability of these devices.

Key Terms: - *Al_2O_3, HfO_2, High-k, MNOS, SNOS, SONOS.*

I. INTRODUCTION

Localized charge-trapping devices based on polysilicon-oxide-nitride-oxide-silicon (SONOS) structures are appealing for non-volatile memories beyond the floating gate technology, due to their integration with standard CMOS technology, low-voltage programming, immunity to irregular charge loss and capability of 2-bit/transistor storage. In addition, SONOS technology-based memories with the NAND-type flash memory array have been proposed as a candidate for replacing the commercial mass data storage disk. Whereas the generation of interface traps during hot carrier injection bias temperature instability is a significant concern of the CMOS reliability. This paper reviews the microstructures of high-*k* dielectrics used as tunneling layers, charge trapping layers and blocking layers in SONOS-type memories, and their impacts on the memory behaviours. The advancement of the memory characteristics by using multilayered structures (multilayered tunneling layer or multilayered charge trapping layer) are also discussed. Finally, this evaluation concludes our perspectives towards the future researches on the high-k dielectrics applicable to SONOS-type non-volatile. The storage of charges in the gate insulator of MOSFET is realized in two ways resulting in subdivision of Nonvolatile semiconductor memory devices into two main types. One is floating gate device in which the charge is stored on a conducting or semiconducting layer surrounded completely by a dielectric, usually thermal oxide. Since this layer acts as completely isolated gate therefore this type of device is referred to as floating gate device. Other is charge-trapping devices in which the charge is stored in discrete trap centers of an suitable dielectric layer [1]. MNOS device (Metal-Nitride-Oxide-Semiconductor) is most successful structure in this category, in which the insulator consists of silicon nitride layer on top of very thin silicon oxide layer. The device state can be read by applying an appropriate "sensing" voltage to the control gate.

II. MNOS

The metal-nitride-oxide-silicon (MNOS) devices were invented in 1967 [2] and were first electrically alterable semiconductor (EAROM). This charge trapping device became another potential candidate of NVM due to its storage capability of charges in discrete traps in the nitride layer. Electrons or holes are injected from the channel region into the nitride by quantum mechanical tunneling through ultra-thin oxide (UTO, typically 1.5 to 3 nm). Charges are stored in deep level traps in Si_3N_4 .Nitride layer is used to increase the density and probability of capturing electrons and holes. These trapped charges cause a significant shift in the threshold voltage of the transistor, Q_T the trapped charge in the nitride layer. In programming process, a large positive bias is applied to the gate [3]. Current conduction is due to electrons that are emitted from the substrate to the gate by the tunneling.

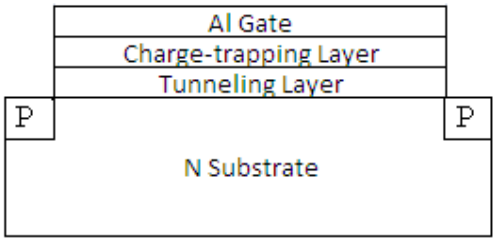

Fig 1: Schematic of MNOS

During erase operation, negative bias is applied to the gate and current conduction is due to tunneling of holes from substrate which neutralize the trapped electrons. The advantages of the MNOS transistor include reasonable speed for programming and erasing, making it a suitable candidate for NVM. Limitations of MNOS are large programming and erasing voltages, data retention and erase/write endurance. These limitations result in narrow threshold voltage window after many cycles of programming and erasing. Therefore MNOS devices are used only in specific applications (such as military). Radiation hardness of MNOS is higher than that of the flash memory.

III. SNOS

The SNOS consists of a silicon nitride layer (20-40 nm) on top of the ultra thin oxide on silicon. The programming of the SNOS is performed as: during the write operation, a high (positive) sub-voltage is applied to the gate with the well grounded. Electrons tunnel from the silicon conduction band into the nitride conduction band through Fowler-Nordheim tunneling process and they are trapped in the nitride trap centre, that leads to positive threshold voltage shift [4,5]. During erase operation the gate is grounded and high positive voltage is applied to well. Holes tunnel directly from silicon valance band into nitride valance band, that leads to negative threshold voltage.

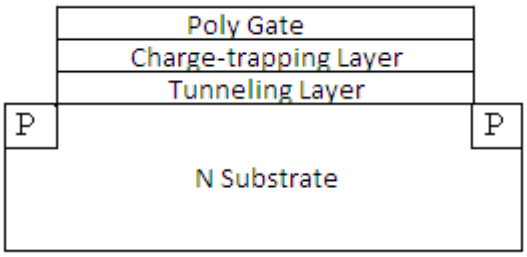

Fig 2: Schematic of SNOS

For proper operation the select transistor is required and gate is grounded in off-state. During read operation we addressed the cell through the select transistor and then we sense the state of the SNOS transistor. Due to back tunneling the charge content within the nitride will be modified through the ultra thin oxide. Memory window is limited by the hole injection from the gate limit, a problem that becomes more austere for thinner nitride layers as charge stored in it is widely distributed. To contend this problem, silicon oxy-nitride layer instead of a pure silicon nitride layer is used but this requires increased programming voltages because of their higher energy barriers. The irradiation causes charge trapped in the nitride to be emitted from the traps and therefore a rapid decay in the threshold voltage. That's why SONOS devices came into existence.

IV. SONOS

By the late 1980s and early 1990s PMOS SONOS structures were demonstrating program/erase voltages in the range of 5-12 volts The device is similar to SNOS transistor except that it has an additional blocking oxide layer placed between the gate and nitride layer, forming ONO (Oxide-nitride-oxide) stack. Usually thickness of this top oxide layer is similar to the bottom oxide layer. The blocking oxide layer prevent injection of electron from the metal to the nitride layer during erase operation. Lower programming voltage as well as better charge retention is achieved by using thinner nitride layer. The reduction of the programming voltages and the absence of thick oxide in scaled SONOS devices have improved their radiation hardness. The operating speed and date retention characteristics are still the bottlenecks to limit the applications of SONOS-type memories.

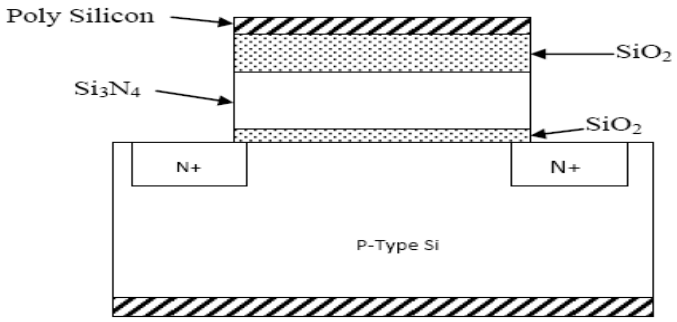

Fig 3: SONOS (Silicon-Oxide-Nitride-Oxide)[6]

Recently, various advances have been done to make a trade-off between the operating speed and the date retention characteristics. Diligence of high-k dielectrics to SONOS-type memories is a prevalent route.

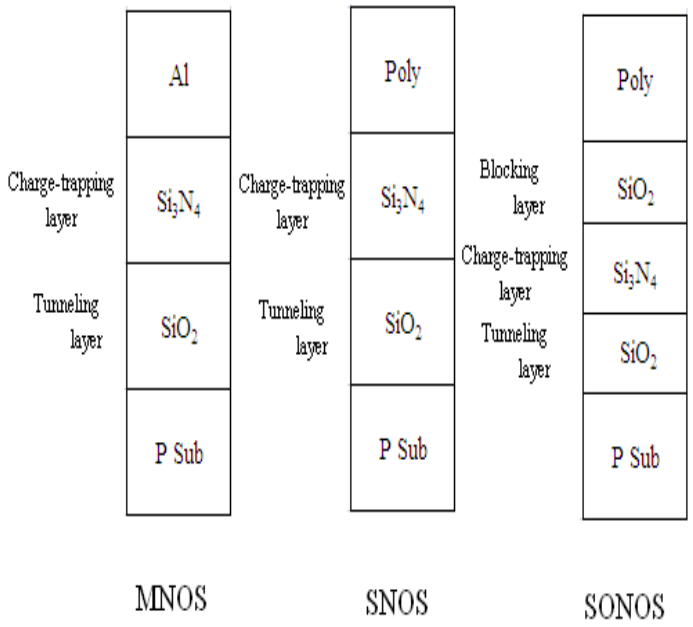

Fig 4: Evolution of SONOS nonvolatile memory device

SONOS Vs general flash memory

1. In general flash memory, charges are stored in the floating gate, whereas in the SONOS, nitride layer is used for charge storage in terms of structure.
2. In general flash memory, floating gate is formed using polysilicon, and any single defect will lead to the discharge of stored memory due to conductive properties of polysilicon gate. Whereas in the SONOS, nitride layer is used instead of polysilicon. Hence, SONOS is less sensitive to polysilicon defect and has improved endurance.
3. In the flash memory, tunnel oxide having a thickness of about 70 Å is formed under the floating gate that limits the low voltage implementation and high speed. Whereas in SONOS the implementation of low-voltage and high speed operation is possible due to the formation of direct tunnel oxide under the nitride.
4. Due to the difference in charge storage mechanism SONOS offers radiation hardness improvements over floating gate EEPROM technology. In SONOS technology charge is stored in the trap centers present in nitride dielectric, and discharge of total charge is not easy. In floating gate memories, charge is stored in conducting floating gates that is separated from the silicon substrate by thin (<100 Å) tunnel oxides leading to rapid charge loss. Heavy ion can discharge floating gate devices. Both these effect limit the radiation hardness of floating gate devices which is not found with SONOS devices.
5. Scaling of floating gate is limited in the lateral (gate-to-gate) direction also. An electric field is there due to the electrons stored on the polysilicon gate. As the geometry contracts, this electric field becomes stronger and may programs or erases adjacent cells unintentionally That limits channel length scaling to 45nm.In SONOS,

the charges do not interfere with adjacent cells as they are electrically trapped in the nitride layer. Hence the scaling limit of SONOS device is not as serious as in Flash memory.

6. SONOS is also advantageous over floating gate, in terms of process complexity and manufacturing steps. Floating gate comprises of two polysilicon gates, two oxide layers (tunnel oxide and thick oxide for the high-voltage pump circuits) and up-to 10 masking steps. As a result cycle time and manufacturing costs increases. SONOS has only one poly gate, one (un-patterned) nitride, one oxide (pump voltages are lower) and three masking steps [7].

V. NEED OF HIGH-K DIELECTRIC

As the thickness of SiO_2 gate dielectrics approaches to 2-3 nm, high leakage current becomes as serious obstacles to future device reliability [8]. In order to overcome these problems, higher permittivity (k) materials, which allows an equivalent capacitance to be achieved using a physically thicker insulating layer, can replace the conventional SiO_2 gate dielectric to realize further scaling down. The program/erase speed can be enhanced by scaling the tunneling layer thickness. However, the date retention capability becomes worse simultaneously due to the reduction of tunneling layer thickness. To solve this issue, the high-k dielectrics have been investigated. Different dielectric materials as HfO_2(25), Al_2O_3(9), La_2O_3 (30), ZrO_2 (25), Ta_2O_5(26), Y_2O_3(15) and combination of these materials as $((HfO_2)_x(Al_2O_3)_{1-x})$, $(HfO_2.Al_2O_3.HfO_2)$ are used depending on application.

Table 1: Function of Layers with choices of materials

Functional Domain	**Purpose**	**Choice of High-k Material**
Tunneling Layer	Tunnels the charge carriers into charge-trapping layer	HfO_2, Ta_2O_5
Charge Trapping Layer	Contains charge trap centers able to hold an electrostatic charge.	HfO_2, Al_2O_3, La_2O_3, ZrO_2
Blocking layer	Prevents tunneling of charge carriers into gate.	Al_2O_3, $((HfO_2)_x, (Al_2O_3)_{1-x})$

Table 2: Properties of high-k dielectric materials:

Properties	**HfO_2**	**Al_2O_3**
Annealing Effect	1. O_2 annealing results in improvement of interfacial quality. [9] 2. N_2 annealing results in improved electrical properties. [9]	RTA annealing at 1150 ^oC results in best insulating property for thin film. [10]
Radiation Response	No measurable effect.[11]	No significant response due to bias-induced electron trapping and radiation-induced hole trapping. [12]
Bias Temperature Instability	Significant BTI effect due to a large number of charge trap centers. [13]	BTI reliability is achieved by using as capping layer. [14]

VI. CONCLUSION

Issues with the conventional floating gate-type nonvolatile semiconductor memories, are reliability, low-power, low-voltage performance with the further scaling of device size. Therefore need arises to replace the conventional floating gate nonvolatile semiconductors memory with charge-trapping devices like SNOS, MNOS and SONOS-type memory device have been investigated widely in the past several years. However, the operating speed and date retention characteristics are bottle necks for SONOS-type memory devices. Utilizing high-*k* dielectrics as the charge trapping layer, tunneling layer and blocking layer in these devices is a predominant approach to realize a trade-off between the operating speed and the date retention time. Properties like annealing, bias temperature instability and radiation response of high-k dielectric material like HfO_2 and Al_2O_3 affects performance of NVM.

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