IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
Vol. 04, Issue 05 (May. 2014), ||V1|| PP 52-60

Fine-Grain Power-Gated Logic for Asynchronous Circuit Using Partial Charge Reuse

[1]Preethibha C,[2] Vijayabhasker R
[1]*Department of Electronics and communication Engineering,Anna University.*
[2]*Department of Electronics and communication Engineering,Anna University.*
[1] *Regional Center of Anna University,Coimbatore,India.*
[2] *Regional Center of Anna University,Coimbatore,India.*

Abstract: - This report introduces a novel low power logic family, called asynchronous fine grain power gated logic (AFPL).Each pipeline stage in the AFPL circuit is made up of efficient charge recovery logic (ECRL) gate, which carry out the logic part of the stage, and a handshake controller, which handles handshaking with the neighboring stages and provide power to ECRL gates.In the AFPL circuit, ECRL gates acquire power and become alive only when performing useful computations, and idle ECRL gates are not powered and thus have negligible power dissipation.The partial charge reuse (PCR) mechanism can be integrated in the AFPL circuit. With the PCR mechanism, part of the charge on the output nodes of an ECRL gate entering the discharge phase can be reused to charge the output nodes of another ECRL gate about to evaluate, reducing the energy dissipation required to complete the evaluation of an ECRL gate. Moreover, the AFPL-PCR adopts an enhanced C-element, called a Sutherland pull-up pull-down, in its handshake controllers such that an ECRL gate in the AFPL-PCR can enter the sleep mode early once its output has been obtained by the downstream pipeline stage.In order to assess the strength of the proposed AFPL, it is carried out in a Kogge-Stone Adder for performance comparison**.**

Index Terms: - *Asynchronous circuit, Low power electronics, C-element, Power gating.*

I. INTRODUCTION

As the feature size continues to contract and the corresponding transistor density increases, power dissipation have become an important concern in nanoscale CMOS VLSI design. Power dissipation in CMOS circuit can be categorized into dynamic dissipation and static dissipation. Dynamic power is the power dissipated when the device is active, and the static power is the power dissipated when the device is powered up but no signals are changing their values. Dynamic power consists of switching power, caused by charging and discharging of load capacitance. Static dissipation results from leakage currents, and the primary source of leakage include sub-threshold leakage, gate leakage, gate induced drain leakage and junction leakage [12].As a threshold potential, channel length and gate oxide thickness continue to shrivel up, leakage dissipation is becoming a substantial contributor to the total power dissipation.Leakage power can contribute every bit much as third of total power.

Several techniques for reducing leakage, loss in CMOS circuits have been offered both at the circuit and process technology levels [12]. At the circuit level, leakage reduction techniques include transistor stacking [2], [9], reverse body biasing [4] - [10], dual threshold CMOS [12] - [15], and power gating [3]-[10]. Among these techniques, power gating is one of the most efficient techniques for leakage reduction. In general, power gating techniques increase the effective resistance of leakage paths by inserting sleep transistors (power gating transistors)between power supply rails and transistor stacks. In the idle mode, the sleep transistors are turned off, turning off the pull-up pull-down networks off from one (or) both power rails, and thus leakage current are inhibited. In the active mode, the sleep transistors are turned on, reconnecting the pull-up pull-down networks to power supply rails.

A digital circuit is synchronous if its design involves the usage of a single clock signal controlling all circuit events.For synchronous circuits, power gating can be gone through in the fine grain or coarse grain manner. The fine grain approach has more opportunities to reduce leakage at run time than the coarse grain power gating approach. Nevertheless, in that respect are several design issues associated with incorporating fine grain power gating in synchronous circuits.

A digital circuit is asynchronous when no clock signal is utilized to hold in any sequencing of events.These circuits employ local handshaking for transferring information between neighboring modules, so they are data driven and active only when performing useful work.Asynchronous circuits can be sorted according to various standards [6].One important measure is established on the delays of wires and gates.The most rich and restrictive delay model is delay-insensitive (DI) model, which works correctly regardless of gate

and wire delay values.The increase of wire delays in some carefully selected forks defines quasi delay-insensitive (QDI) circuit class.Here, signal transition must take place at the same time only at each end point of the mentioned forks. QDI circuits are rather coarse, although other examples such as bundled data are still applied in specific settings.

Asynchronous circuits do not switch when inactive and inherently have the advantage of putting up the equivalent of fine grain clock gating. Although asynchronous circuits in inactive mode have no dynamic dissipation, they still suffer leakage dissipation.Various techniques have been proposed for employing power gating techniques to cut the static power of asynchronous circuits at different layers of granularity [9] -[12]. In [12], when the voltage regulator in an asynchronous on chip (ANOC) node detects no activities on the incoming and outgoing channels, it dilutes down the supply voltage of the asynchronous logic unit implemented with self-controllable voltage level circuit, to reduce the leakage power of the ANOC node. In [9], an asynchronous system is divided into circuit clusters, each cluster controls the power gating of the next few clusters, and a token arriving at a cluster can wake up the next few clusters. Nevertheless, the power down sequence in this system requires complex hardware, such as interleaved counter system [21], to determine whether the line is empty before the power of the pipeline can be turned off.

Asynchronous circuits can be power gated at the gate level of granularity [5], [1]. In [5], each combinational block in the conventional asynchronous four phase bundled data pipeline is equipped with both a header and footer sleep transistor. When the latch controller in a pipeline stage detects valid input data, it absorbs the data in the data latch and turns on the sleep transistor of the associated combinational block, so that the combinational block can wake up and process the input data to generate the output data. When the output data is received by the next pipeline stage, an acknowledge signal is send back to this stage, and the latch controller can turn off the sleep transistor of the associated combinational block to reduce leakage dissipation. This method suffers from the disadvantage that only combinational blocks are power gated, and the other hardware still suffers leakage dissipation. In [5], asynchronous adiabatic logic (AAL) was proposed. Each point in an AAL circuit of an adiabatic gate, which carries out the logic part of the stage, and a control and regeneration (C&R) block, whose output supplies power to the associated adiabatic logic.When the C&R block detects that the input to the adiabatic gate becomes valid, the end product of the C&R block transmits to high, and the adiabatic gate can acquire the ability to evaluate its production.When the C&R block detects that the input to the adiabatic gate becomes empty, the end product of the C&R block goes slow, and the gate becomes idle.The primary disadvantage of this method is the synchronization between neighboring stages is accomplished by a unidirectional control signal, hence the AAL circuit that may hold a diverse propagation delay may have a data token propagation along the pipeline to be overridden by its succeeding data token.

In this report, we suggest a novel low power logic family, called asynchronous fine-grain power gated logic (AFPL). AFPL can achieve fine-grain power gating to mitigate static power dissipation. Moreover, the PCR mechanism and Sutherland pull-up pull-down C element that operates as an event synchronizer can be combined with AFPL to reduce the energy dissipation require to complete the evaluation of a logic block.

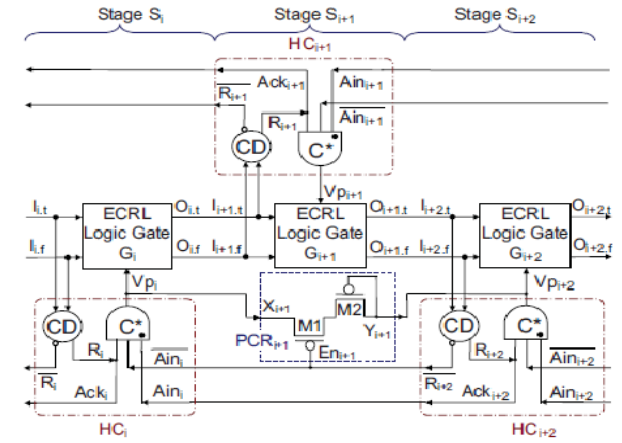
The rest of this report is organized as follows. In Section II, we present the structure of the AFPL pipeline, and describe the logic gates and the handshake controllers used in the AFPL pipeline. Section III presents the PCR mechanism and Sutherland, C-element. Section IV describes the simulation results. Finally, conclusions are made in section V.

II. AFPL

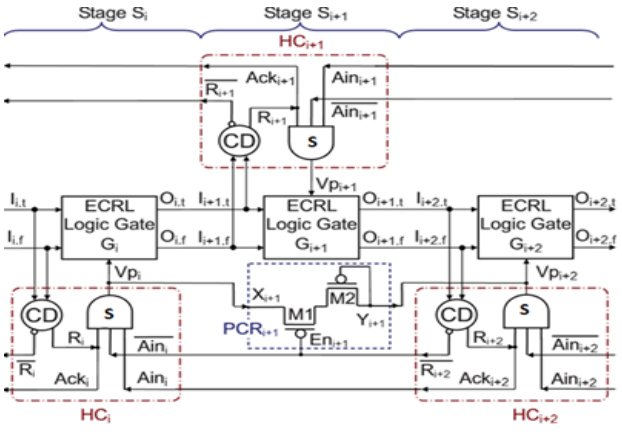
A. Overview

In this section, the proposed AFPL is presented. Fig.1 shows the structure of AFPL pipeline. In AFPL – PCR [see Fig. 1(a)], a pipeline stage, denoted by S_i, is comprised of an efficient charge recovery logic [8] (ECRL) gate G_i, which implements the logic function of the stage and a handshake controller HCi, which handles handshaking with the neighboring stages and provides power to ECRL logic gate G_i. In AFPL-PCR, a pipeline stage denoted by Si, has an additional unit, the PCR unit PCR_{i+1}, which controls charge value between pipeline stages Si and Si_{+2}. The AFPL-PCR with Sutherlandpull-up pull-down C-element [see Fig. 1(b)], which is used as a means to reduce the input power to the ECRL gate, G_i.

It is recognized that the synchronization between modules in an asynchronous system is not achieved by a global clock, but rather by local handshake Signal, request and recognize. In AFPL, the handshake protocol used is the four phase dual rail protocol, in which the request signal is encoded into the data signals. For instance, one-bit information, denoted by d, can be encoded with a pair of wires d.t and d.f. If (d.t, d.f) = (1,0) the codeword (d.t, d.f) is a valid token and represent a logic 1; If (d.t, d.f) = (0,1) the code word (d.t, d.f) is a valid token and represents a logic 0; If (d.t, d.f) = (0,0), the code word (d.t, d.f) is an empty token and represent no data.



(a)



(b)

Fig. 1. AFPL Pipelines. (a)AFPL-PCR Pipeline. (b) AFPL-PCR with Sutherland C.

In the four phase dual – rail protocol, the transferring of data from the sender to receiver involves the following four actions: 1) the sender issues a valid code word on the communication channel ; 2) the receiver acquires the valid code word from the communication channel , and then asserts the acknowledge signal ; 3) the responds by using an empty code word to indicate that the data on the communication channel is no longer valid ; 4) the receiver deasserts the acknowledge signal to complete the communication cycle. Thus, the data stream flowing through the AFPL pipeline is a sequence of alternating valid tokens and empty tokens.

B. ECRL Logic Gate

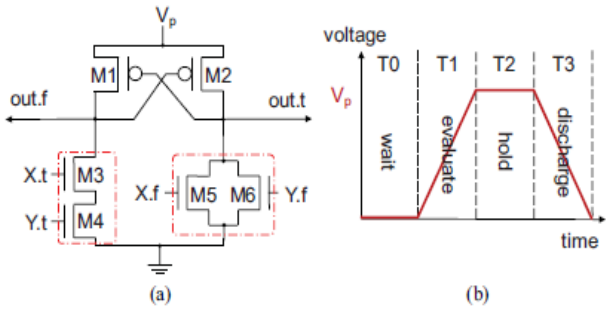


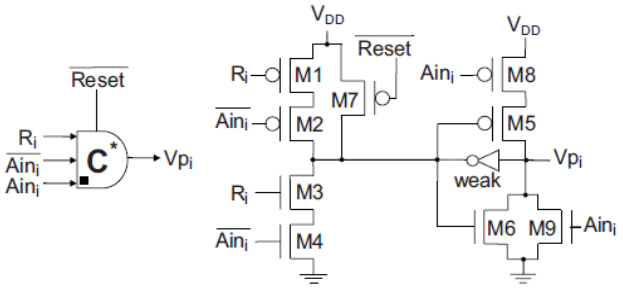
Fig. 2. ECRL logic. (a) ECRL AND/NAND gate.
(b)Operation phases for ECRL

In order to implement the logic function of AFPL, an ERCL gate is used. Fig.2 (a) shows the structure of an ECRL AND/NAND gate. ECRL adopts dual-rail data encoding; that is, each input to an ERCL gate computes both a logic part and its complement.As shown in Fig.2 (a), an ECRL gate acquires power from the power node, denoted by Vp. In the AFPL-PCR pipeline, the power node Vpi is connected to the output of the handshake controller HC_i. That is, the ECRL gates in the AFPL pipeline acquire their power from the handshake controllers instead from a conventional fixed DC power supply. The operation cycle of an ECRL gate comprises four phases, wait, evaluate, hold and discharge. The current operation phase of an ECRL gate Gi is determined by the voltage of the associate power node Vpi. Fig.2 (b) shows the voltage waveform of the power node Vpi. During the wait phase, the power node Vpi is kept at 0V, and gate Gi cannot draw any current from Vpi. Thus, the corresponding gate outputs out.t and out.f are both kept low (i.e., empty tokens) irrespective of the current input values. In the evaluate phase the voltage Vpi ramps up from 0V to VDD, and gate Gi draws current from Vpi and begin to evaluate its outputs. During the hold phase, the voltage of Vp stage at VDD , and outputs out.t and out.f remains valid for the entire hold phase , even if the input become empty. In the discharge phase, the voltage Vp ramps down from VDD to 0V, the charge on the output node is now transferred back to the power node Vpi , and the outputs become empty.

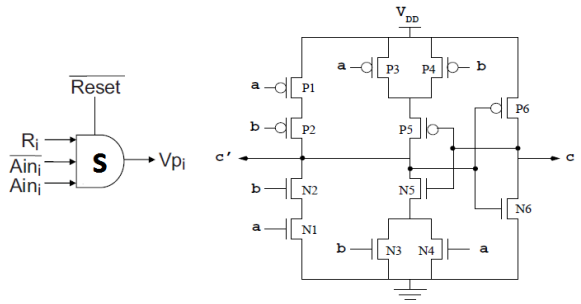
C. Handshake controllers

In the AFPL-PCR pipeline, the handshake controller HCi in stage Si, performs the following tasks:1)Detecting the validity of the inputs to the ECRL logic gates in stage Si; 2)Offering power to the ECRL logic gates in stage Si; 3)Detecting whether the output of stage Sihas been received by the downstream stage Si+2; and 4)Informing the upstream stage Si-2 when Si-2 can remove its output.

As shown in Fig.1(a), a handshake controller is comprised of a completion detector (CD) and a C*-element, the CD in HCi is used to detect whether the input to stage Si represents a valid code word or an empty code word. The output of the CD transits from low to high when the input to stage Si becomes a valid code word, and transition from high to low when the input to the stage Si becomes an empty code word. The input consists of n-bit data, n pairs of wires are taken to encode the input, and the associated CD can be implemented with an input C* element gate and n-two input OR gate .



(a)



(b)

Fig. 3. Structure of the C-elements used in AFPL. (a) C* element. (b) Sutherland C-element.

The output of the C* element in HCi is connected to Vpi, the power node of the ECRL gates in stage Si. A C* element gate is a state- holding device, and its output is set to HIGH when all inputs are HIGH and set to LOW when all inputs are LOW. When the AFPL-PCR starts up, the reset bar signal is utilized to format the output of all C* elements in the AFPL-PCR to low, and thereby all power nodes are set to 0v.That is, every stage in the AFPL pipeline operates in the wait phase in the outset.

The structure of the C* element is shown in Fig.3 (b). The C* elements in HCi has 3 inputs, Ri, Aini bar, Aini. Ri is the request signal from the CD in HCi. Aini and Aini bar are the acknowledgement signal from

HCi+2. After reset, Ri=0, Aini=0 and Aini bar = 1. The transition of Ri and Aini involves the following 4 events.

1)Event req ↑: Ri transits from how to HIGH. This case comes when a valid token arrives at stage Si.

2) Even ack↑: Aini transits from low to high and Aini bar transits from high to low. This event occurs when the valid output of the stage Si has been received by the stage Si+2.

3) Event req↓: Ri transits from high to low. This effect happens when an empty token arrives at stage Si.

4) Event ack↓: Aini transits from high to low and Aini bar transits from low to high. This event occurs when the empty output of stage Si has been received by stage Si+2.

Event ack↑ may occur before or after event req↓ does. Thus, the ECRL logic gates in Si can enter the discharge phase to achieve early discharging as soon as the valid output of stage Si has been received by stage Si+2 without waiting for the next empty token to arrive at Si .

In summary, every stage in the AFPL pipeline repeats the operation cycle comprised of a wait, evaluate hold and discharge phase. The forwarding of a valid token causes a pipeline stage to evaluate, the forwarding of an empty token cause a pipeline stage to discharge.

III. PCR MECHANISM AND SUTHERLAND C-ELEMENT

Fig.1(b) shows the 3 stage pipeline AFPL-PCR with Sutherland C. A more detailed diagram of 6 stage pipeline AFPL-PCR with Sutherland C is illustrated in Fig.4. First ,the AFPL-PCR employs the PCR unit PCR i+1 to control the charge reuse between pipeline stage Si and Si+2 second , the handshake controller HCi in AFPL-PCR employs an enhanced c element, which is called Sutherland C element shown in Fig.3(b), to control the power node Vpi of the associated ECRL gates . This Sutherland C element offers the advantage that an ECRL gate can achieve early discharging if their outputs are no

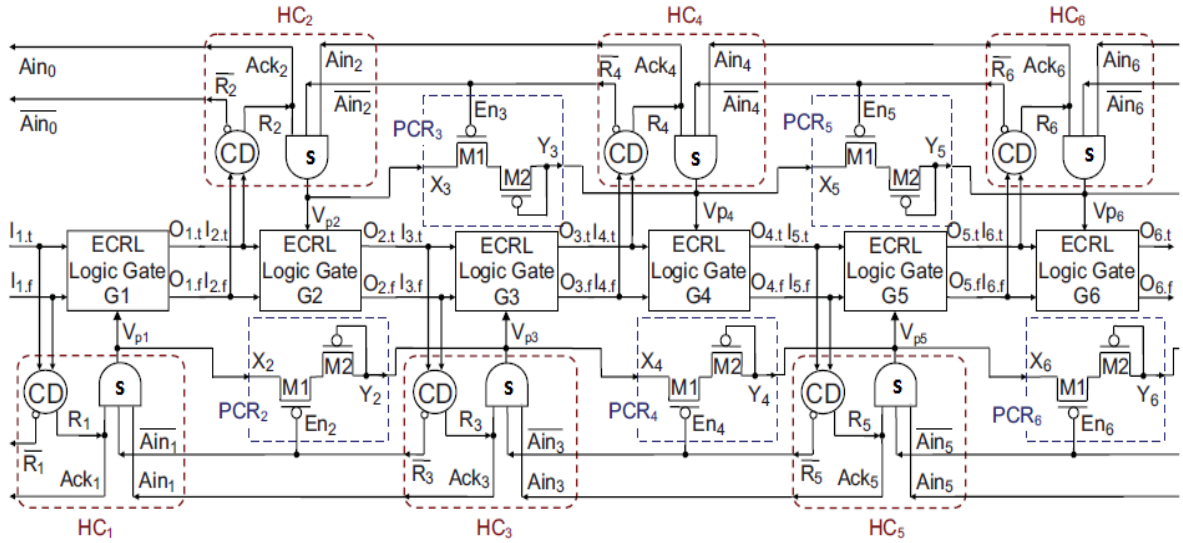


Fig. 4. AFPL-PCR with Sutherland C pipeline in six stages.

longer required without waiting for the next empty token to arrive at this stage.

As shown in Fig.1(b), in the PCR i+1 unit, transistor M2 is used as a diode, which allow the current to flow only in the direction from Vpi to Vpi+2, and transistor M1 is used as a switch, which is turned on when charge reuse is activated.

The operation of AFPL-PCR with Sutherland C is similar to that of AFPL-PCR, except that AFPL-PCR with Sutherland C exploits early discharging to further reduce energy dissipation. This is borne out, since Sutherland C, does not impose any limitation on the size of the transistors. The operation of the Sutherland, C is similar to that of C* element, from the operation of the circuit, we conclude that N1, N2 and N6 are the main pull down transistor, which contribute to output switching, they are of size W. Whereas N3, N4 and N5 only provide the necessary feedback to hold the state of the output when the values of the inputs do not match, hence they are made as small as possible to reduce their loading effect.Similarly, the feedback transistor P3, P4 and P5 have minimum width, while P1 and P2, the normal pull- up transistor have width Wp=2. 5W. For instance, let us suppose the k_{th} valid token T_{vk} has reached, the input of S_{i+2} shown in Fig.1(b). The arrival of T_{vk} at S_{i+2} causes the accompanying actions.

1)Aini (i.e.Ri+2) becoming high causes transistor M8 in the c* element of the HCi to turn off. Power V_{DD} is cut off from power load Vpi, and ECRL gateGi begins to discharge.

2)Eni+1(i.e.Ri+2 bar) becoming low causes transistor Mi in PCRi+1 to turn ON. Because of charge sharing part of

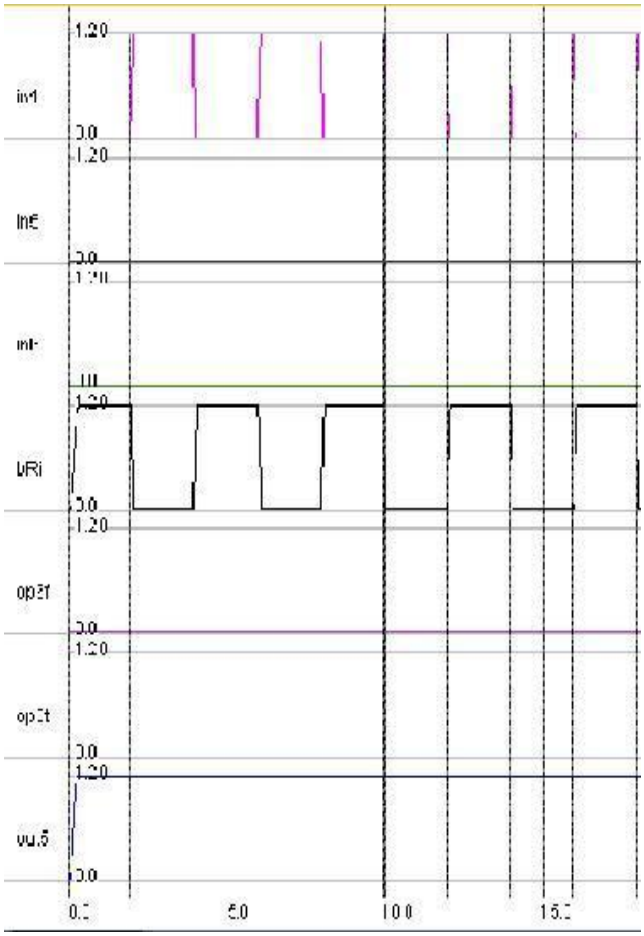


Fig. 5. Simulation Waveforms of AFPL-PCR with Sutherland C pipeline in six stages.

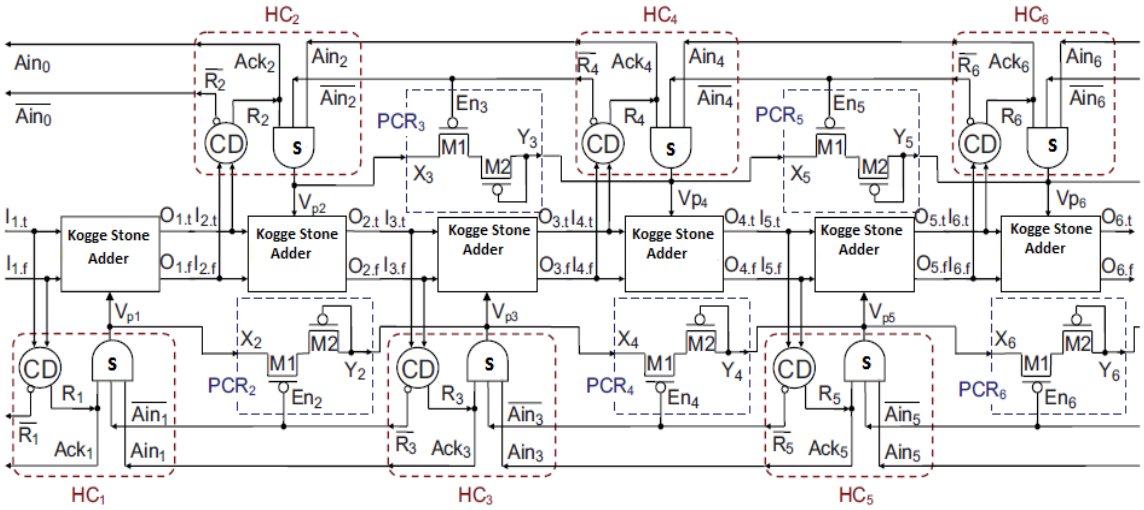


Fig. 6.Kogge Stone Adder with Sutherland C pipeline with six stages.

the charge on the output nodes of gate Gi flows to a power node Vp_{i+2} via Vpi and PCR_{i+1}, causing gate G_{i+2} to enter the evaluate phase. The charge sharing between power nodes Vpi and Vp_{i+2} can happen only when the voltage of Vpi is higher than that of Vp_{i+2} plus|Vtp| and the switch transistor M1 in that of Vp_{i+2} plus |Vtp| and the switch transistor M1 in PCRi+1 is turned on.

3) R_{i+2} becoming high causes a power gating transistor M5 in the C* element of HC_{i+2} to turn on. Power rail Vdd starts offering power to ECRL gate G_{i+2} so that ECRL gate Gi+2 can complete its evaluation.

4) Aini (i.e.R_{i+2}) becoming the HIGH causes the pull down transistor M9 in the C* element of the HCi to turn On. The remaining charge on the output node of gate Gi is discharged to the ground, and thereby gate Gi enters the sleep mode.

Note that the Sutherland C element has the same logic function as that of the C* element, but they are dissimilar in terms of timing. In summary, in the AFPL-PCR pipeline with Sutherland C, the arrival of the valid token at stage s_{i+2} forces stages Si to discharge and turn on the switch in PCR_{i+1}. Portion of charge along the output nodes and gate GI are reused to charge the output nodes and gate G_{i+2} to reduce energy dissipation. The use of Sutherland C makes it possible to synchronize the discharging of gate Gi with a evaluating of gate G_{i+2} and to have gate Gi enter the sleep mode early to further reduce static power dissipation.

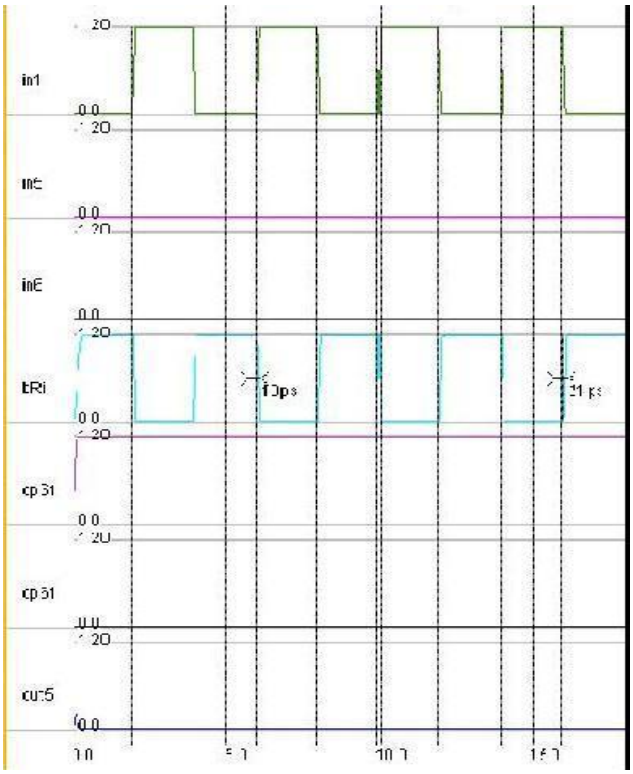


Fig. 7. Simulation Waveforms of Kogge Stone Adder with Sutherland C pipeline in six stages.

TABLE I PERFORMANCE ESTIMATES OF VARIOUS PIPELINED CIRCUITS

Circuit Module	Number Of Transistors Used	Delay(ns)	Power (Watts)
AFPL with PCR (3 stage)	**68**	**0.00099**	**2.499**
AFPL with Sutherland C(3 stage)	**56**	**0.000662**	**1.655**
AFPL with PCR (6stage)	**136**	**0.0022**	**5.453**
AFPL with Sutherland C(6 stage)	**118**	**0.002**	**5.07**
Kogge Stone Adder with C*(6 stage)	**100**	**0.00132**	**3.355**
Kogge Stone Adder with Sutherland C(6 stage)	**118**	**0.000184**	**0.462**

IV. SIMULATION RESULTS

In order to assess the strength of the proposed AFPL, we have used AFPL-PCR and AFPL-PCR with Sutherland, C to implement an Kogge-stone adder for performance comparison. The simulations were performed with microwind using the transistor model of predictive technology.PCR is the ratio of the amount of charge that the ECRL gate acquires from the PCR unit to the total amount of charge that the ECRL gate requires to complete its evaluation. The higher PCR is, the low amount of charge the ECRL gate acquires from the power rail, and the small amount of energy taken out from the power supply to complete the evaluation of the ECRL gate is required.The power consumption for various circuits is shown in Table I.

V. CONCLUSION

This report has proposed the AFPL. In the AFPL circuit, the idle logic blocks are not powered and thus have negligible leakage power dissipation. Most of the power is reduced during runtime by the use of fine-grain power gating.

To eliminate the requirement for additional pipeline latches and to avoid the occurrence of short circuit current from VDD to ground, the AFPL circuit employs ECRL logic. By the use of PCR mechanism, part of charge on the output nodes of a discharging ECRL gate can be reused to charge another ECRL logic gate which is about to evaluate, reducing energy dissipation required to complete the evaluation of an ECRL logic gate.

The use of enhanced C-element such as Sutherland pull-up pull-down in the handshake controller of AFPL-PCR pipeline allows the ECRL logic gate to enter the sleep mode early to reduce leakage dissipation once its output has been received by the downstream pipeline stage.

Compared with AFPL-PCR implementation of the kogge stone adder, the implementation of the same with the Sutherland C can reduce static power dissipation by 90% when the input data ranges from 30 to 900MHz.Although the AFPL-PCR implementation with Sutherland C has the advantage of lower power dissipation, it suffers from the problem of sustainable throughput rate. Thus, the kogge stone adder has a performance loss of 30%.

Simulation results shoes that the AFPL-PCR circuit is robust to process, supply voltage, and temperature variations.

REFERENCES

[1] M. Arsalan and M. Shams,"Asynchronous Adiabatic logic," in Proc.IEEE Int.Symp.Circuits Syst.May 2007,pp.3720-3723.

[2] Z. Chen, M. Johnson, L. Wei, and K. Roy, "Estimation of standby leakage power inCMOS circuits considering accurate modeling of transistor stacks," in Proc. Int. Symp. Low Power Electron. Design, 1998, pp. 239–244.

[3] K. Ishida, K. Kanda, A. Tamtrakarn, H. Kawaguchi, and T. Sakurai, "Managing subthreshold leakage in charge-based analog circuits with low-VTH transistors by analog T-switch (AT-switch) and super cut-off CMOS (SCCMOS)," IEEE J. Solid-State Circuits, vol. 41, no. 4, pp.859–867, Apr. 2006.

[4] H. Jeon, Y.-B. Kim, and M. Choi, "Standby leakage power reduction technique for nanoscale CMOS VLSI systems," IEEE Trans. Instr.Meas., vol. 59, no. 5, pp. 1127–1133, May 2010.

[5] T. Lin,K-S. Chong,B-H.Gwee, and J.S. Chang," Fine-grained power gating for leakage and short ciruit power reduction by using asynchronous logic," in Proc.IEEE Symp.Circuits Syst.,May 2009,pp.3162-3165.

[6] MatheusMoreria, Bruno Oliveria, Fernando Moraes, Ney Calazans, "Impact of C-Elements in Asynchoronous Circuits" in Proc. Int. Symp. Quality Electronic Design, March 2012, pp. 437-443.

[7] Meng-Chou Chang, Member, IEEE, and Wei-Hsiang Chang "Asynchronous Fine-Grain Power-Gated Logic",IEEE vol.21,No.6,June 2013.

[8] Y. Moon and D. K. Jeong, "An efficient charge recovery logic circuit," IEEE J. Solid-State Circuits, vol. 31, no. 4, pp. 514–522, Apr. 1996.

[9] S. Narendra, S. Borkar, V. De, D. Antoniadis, and A. Chandrakasan,"Scaling of stack effect and its application for leakage reduction," in Proc. Int. Symp. Low Power Electron. Design, 2001, pp. 195–200.

[10] M. Nomura, Y. Ikenaga, K. Takeda, Y. Nakazawa, Y. Aimoto, and Y. Hagihara,c "Delay and power monitoring schemes for minimizing power consumption by means of supply and threshold voltage control in active and standby modes," IEEE J. Solid State Circuits, vol. 41, no. 4, pp. 805–814, Apr. 2006.

[11] C. Ortega, J. Tse, and R. Manohar, "Static power reduction techniques for asynchronous circuits," in Proc. IEEE Symp. Asynchronous CircuitsSyst., May 2010, pp. 52–61.

[12] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep submicrometer CMOScircuits," Proc. IEEE, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[13] M.Shams, J. C. Ebergen, and M. I. Elmarsy, "Modeling and comparing CMOS implementations of the C-element", IEEE Transactions on Very Large Scale Integration, 6(4), pp.567-367, Dec 1998.

[14] Y.Thonnart, E.Beigne,A.Valentian, and P.Vivet,"Automatic power regulation based on an asynchronous activity detection and its application ANOC node leakage reduction," in Proc.IEEE Symp. Asynchronous Circuits Syst., pp.48-57, Apr.2008.

[15] L. Wei, Z. Chen, K. Roy, M. C. Johnson, Y. Ye, and V. K. De, "Design and optimization of dual threshold circuits for low-voltage low-power applications," IEEETrans. Very Large Scale Integr. (VLSI) Syst., vol. 7, no. 1, pp. 16–24, Mar. 1999.

AUTHOR PROFILE

C.Preethibha working as an assistant professor in the department of Electronics & Communication Engineering at Park College of engineering and technology, Coimbatore, India. She completed her B.E in 2005 with first class from S.K.R Engineering College,Chennai. She is pursuing her M.E in Regional Center of Anna University,Coimbatore.Her field of interest are VLSI Design,VLSI Systems and Communication Systems.

Dr.R.VijayaBhasker working as an Assistant Professor in the department of Electronics & Communication Engineering at Regional Center of Anna University, Coimbatore. He completed his B.E in EEE,M.E in Power Electronics and Drives and his Ph.D in Electrical Engineering.His field of interest are Power Electronics and drives,VLSI Design,VLSI Systems and Control Systems.