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AC-DC Matrix Converter Based On Cockcroft-Walton Voltage Multiplier

Adinath Jain, Simith E
Asst Prof, Dept of electrical and electronics RV College of engineering Bangalore, India
Dept of electrical and electronics RV College of engineering Bangalore, India

Abstract: **-** A single-phase step-up ac–dc matrix converter based on Cockcroft–Walton CW) voltage multiplier is explained in this paper. Here we are using a four bidirectional- switch matrix converter in between the CW circuit and ac source, the modern topology gives high quality of line conditions, adjustable output voltage, and low output ripple. The proposed matrix converter is operated with two independent frequencies. One of the frequencies is associated with Power Factor Correction (PFC) control, and the other frequency is to set the matrix converters output frequency. Here we are simulated 50V/12W converter for measurement and analysis. The measured system efficiency and power factor is improved and output voltage ripple is reduced at full load condition. A 10V AC to 50V DC laboratory prototype of the converter is built for test, measurement, and evaluation.

Index Terms**: -** *Cockcroft–Walton voltage multiplier (CW), high step-up ac–dc converter, power factor correction (PFC).*

I. INTRODUCTION

High voltage dc power supplies are commonly used in science, military, industries, medicine, such as test equipment, X-ray systems, dust-filtering, insulating test, and electrostatic coating [1]–[3]. Using the advantages of low voltage stress on the diodes and capacitors, high voltage ratio, compactness, and cost efficiency, the conventional Cockcroft–Walton (CW) voltage multiplier is commonly used for high-voltage dc applications. A conventional CW voltage multiplier is shown in Fig. 1. The well-known CW voltage multiplier is made by joining a number of diode–capacitor ladder stages with each stage containing two capacitors and two diodes. Theoretically, an *n*-stage CW voltage multiplier dc output voltage is equal to the value of 2*n* times of the magnitude of the ac voltage source under no-load condition. Due to non ideal characteristics of the circuit components the dc output voltage is practically less than the theoretic value [1], [3], [4]. Some drawback of CW multiplier is, under heavy-load condition, the CW multiplier intrinsically presents not only poor output voltage regulation but also high output ripple with line frequency. In some applications, for getting higher voltage gain we use line frequency transformers with high step-up ratio to cooperate with the CW voltage multiplier. However, sourced by the utility ac source, the transformers lead to inefficiency of bulk and cost, and the ripple problem still unsolved [5]. Inheriting the merits of the high-frequency switching techniques, many advanced CW circuits have been developed for saving the volume of the transformers, smoothing the output ripple, and regulating the output voltage. In [6]–[8], some voltage-fed modified CW topologies are discussed, which provides not only high voltage gain but also simplicity of implementation, were proposed. Nevertheless, among these topologies, the high frequency transformer with high turns ratios causes large winding capacitance and leakage inductance, which leads to high current and voltage stresses and higher switching losses on the switches. Moreover, operating in discontinuous conduction mode (DCM), these topologies incur more losses, stress, and electromagnetic interference (EMI) problems. In [9], parallel, series and hybrid resonant converters incorporated with high-step up and high frequency transformer were proposed to energize a CW circuit, in which the non ideal components of the transformer were under consideration. However, these converters were supplied only by dc sources. In [10]–[12], soft switching techniques were applied to resonant-type CW circuits to reduce switching losses on power switches for enhancing efficiency. In [15], a modified topology ,with integrated multiphase boost converter and voltage multiplier, was proposed for high step-up conversion and high-power applications as well. In this topology, all capacitors in the voltage multiplier had identical voltage rating. Moreover, some non isolated high step up dc–dc converters with low-voltage dc input were proposed for renewable energy applications [16]–[18].

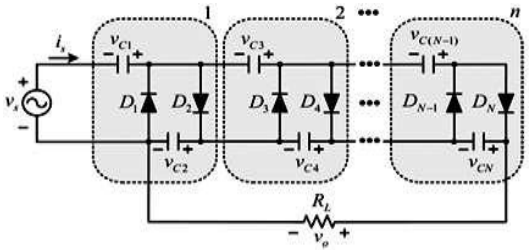


Figure 1: Conventional Cockcroft-Walton voltage multiplier

II. PRINCIPLE OF OPERATION OF THE CONVERTER

The topology is mainly composed of a single phase matrix converter cascaded with a traditional *n*-stage CW voltage multiplier, as shown in Figure 2. The single phase matrix converter forms with four bidirectional switches that are divided into two sets denoted as (*Sc* 1, *Sc* 2) and (*Sm*1, *Sm*2). The proposed converter is energized by a line-frequency ac source with a series inductor for boost operation. Two anti-series insulated gate bipolar transistors with freewheel diode are used as a bidirectional switch. The matrix converter employs two independent frequencies. One of the frequencies applies to two of the four switches to perform PFC function, and the other applies to the rest of the two switches to determine the output frequency of the matrix converter. The latter frequency determines the output frequency of the matrix converter and, then, can be used to smooth the ripple voltage in the dc output. Even deploying bidirectional switches, the proposed converter can adopt PFC control methods of conventional ac–dc boost converters just with some modifications. Therefore, one voltage control loop and an inner current control loop are added to the proposed converter which modifies the original switching signal to trigger the four bidirectional switches properly.

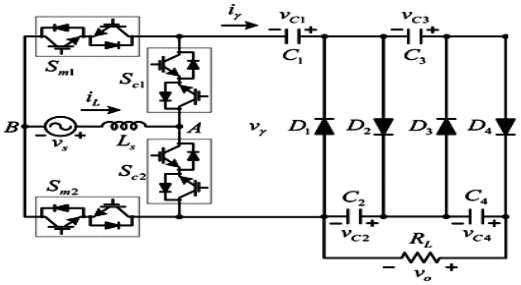


Figure 2: AC-DC converter with CW voltage multiplier and Matrix converter

In order to simplify the analysis of circuit operation, a two stage CW voltage multiplier is used in the AC-DC converter, as shown in Fig 2. Before analyzing, some assumptions are made as follows:

□ □ All of circuit elements are ideal and there is no power loss in the system.

□ □ All the capacitors in the CW voltage multiplier are sufficiently large, and thevoltage drop and ripple of each capacitor can be ignored under a reasonable load condition. Thus, the voltages across all capacitors are equal, except the first capacitor which voltage is one half of the others.

□ □ The proposed converter operates in Continues Conduction Mode and under steadystate condition.

According to the second assumption, each capacitor voltage in the CW voltage multiplier is given by

$$v_{ck} = \begin{cases} vc \quad for & k = 1 \\ 2vc \quad for\ k = 2,3,4 \ldots . n \end{cases} \quad \ldots\ldots\ldots (1)$$

where *vCk* is the voltage of the *k*th capacitor, *VC* is the maximum peak value of terminal voltage of the CW voltage multiplier under steady-state condition, and $N = 2n$.

For an *n*-stage CW voltage multiplier, the output voltage is equal to the total voltage of all even capacitors, which can be expressed as

$$Vo = NVC \qquad (2)$$

where *Vo* is the steady-state dc output voltage.

Substituting (2) into (1), each capacitor voltage can be rewritten as

$$v_{ck} = \begin{cases} vo/N \quad for & k = 1 \\ 2vo/N \quad for\ k = 2,3,4 \ldots . n \end{cases} \qquad (3)$$

According to the polarity of the ac source and the switching state of *Sc*1, there are four operation modes of the proposed converter, denoted as modes I–IV. Moreover, combining with boost operation, each mode has two circuit states. Fig.3 shows the two circuit states of mode I, which provides positive $i\gamma$ during positive-half cycle of the ac source, and Fig. 4 shows the two circuit states of mode II, which provides negative

iγ during negative-half cycle of the ac source. For simplicity, the circuit states of modes III and IV are not presented, and they can be obtained by changing the directions of *iγ* and *iL* from Figs. 3 and 4, respectively. Obviously, *Sm*1 and *Sm*2 work as boost switches while *Sc* 1 and *Sc* 2 control the direction of *iγ* , i.e., the output frequency of the matrix onverter. Basically, *Sc* 1 (*Sm*1) and *Sc* 2 (*Sm*2) should be operated in complimentary mode and the operating frequencies of *Sc* 1 and *Sm*1 are defined as *fc* and *fm*,
respectively, where *fc* is called alternating frequency and *fm* is called modulation frequency.

III. Modes of Operation

Mode 1

State 1: During state1, *Sm*1 and *Sc*1 are turned ON, the boost inductor is charged by the input source, *iγ* is zero due to no current path, the even-group capacitors *C*4 and *C*2 supply to the load *RL* , and the odd-group capacitors *C*3 and *C*1 are floating (Figure 3a).

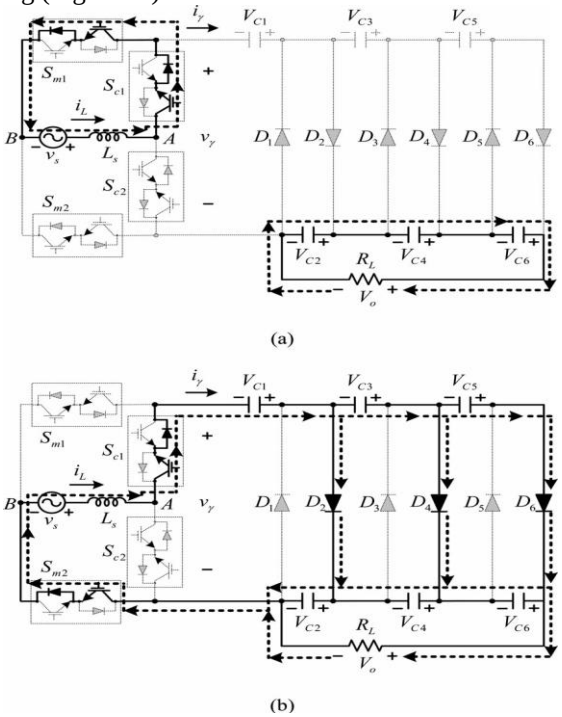


Fig. 3. Circuit states and conducting paths of the proposed converter at mode I. (a) State 1. (b) State 2.

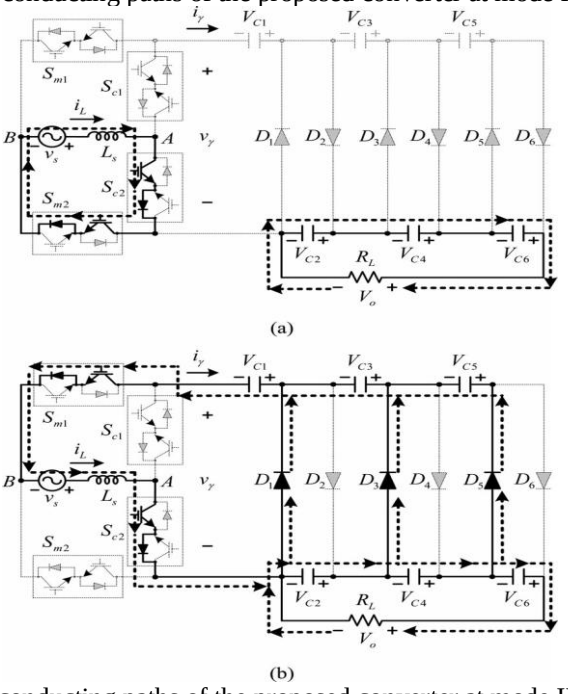


Fig. 4. Circuit states and conducting paths of the proposed converter at mode II. (a) State 1. (b) State 2.

State 2: During state2, *Sm*2 and Sc1 are turned ON, the boost inductor and input source transfer energy to the CW circuit by positive $i\gamma$ flowing through one of the even diodes (Figure 3b).

Mode 2

State 1: During state1, *Sm*2 and *Sc*2 are turned ON, the boost inductor is charged by the input source, $i\gamma$ is zero due to no current path, the even-group capacitors *C*4 and *C*2 supply to the load *RL* , and the odd-group capacitors *C*3 and *C*1 are floating (Figure 4a).

State 2: During state2, *Sm*1 and *Sc* 2 are turned ON, the boost inductor and input source transfer energy to the CW circuit by negative $i\gamma$ flowing through one of the odd diodes (Figure 4b).

The circuit behaviours of modes III and IV can be obtained by similar processes but with opposite directions of both $i\gamma$ and .

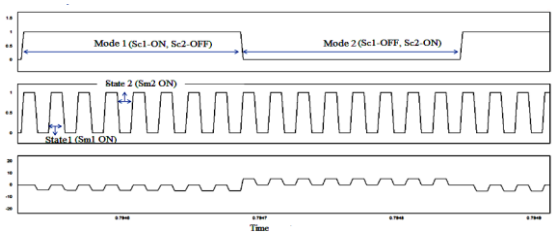


Figure 5: Switching pulses and during mode 1 & 2.

IV. DESIGN CONSIDERATIONS

Here the current ripple in the line current is used to design the value of the boost inductor, and the output ripple voltage caused by both line frequency and alternating frequency is discussed, in which the relation between the size of the capacitors and the value of the ripple is derived and will be used to determine the value of the capacitance. Moreover, the voltage and current stresses on capacitors, switches, and diodes will be considered as well. The system specifications of the prototype used in simulation is summarized in Table 3.1

Table 3.1: Specifications of the prototype

Output power, Po	12W
Output voltage, Vo	50V
Input line voltage ,Vs	10V
Line frequency , fs	50Hz
Modulation frequency , fm	60 kHz
Alternating frequency , fc	3.75 kHz
Resistive load ,RL	150 Ω
Number of Stages , n	2

Determination of parameters

Generally, the maximum peak-to-peak ripple of the line current is used to design the value of the boost inductor, and with the use of area of product method we will get the inductor value as 1mH.

The dc output ripple of the proposed converter is used as a criterion to design the value of the capacitance in the CW voltage multiplier and here we are getting the capacitor value as 1000μF.

Maximum voltage stress on each switch is 13.125V Maximum switch current is 6.2A

Maximum diode voltage is 26.25V

Maximum diode current is 6.2A

V. SIMULATION RESULTS

The component list and their specifications used for simulation are given in table 4.1

Table 4.1: Simulation Parameters

Component Specification	**Symbol**	**Value/Specification**
Input voltage	Vs	10V AC
Output Voltage	Vo	50V DC
Boost Inductor	Ls	1mH
Power switches	Sm1,Sm2 Sc1,Sc2	MOSFET
Capacitors	C1, C2, C3, C4	1000**μ**F/200V
Diodes	D1, D2 D3, D4	200V/10A
Load Resistor	RL	150 Ω

VI. OPEN LOOP SIMLATION

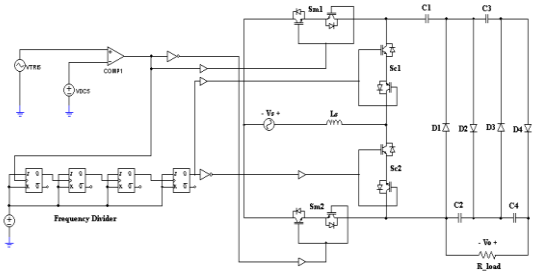


Figure 6: PSIM model of the converter for n=2

Figure 6 shows the open loop simulation diagram in PSIM. The AC input voltage is applied to the Matrix converter which operates with two independent frequencies. The output from Matrix converter is applied to a conventional two stage Cockcroft Walton voltage multiplier. The output voltage is observed across the load resistor.

Figure 7 shows the open loop switching pulses for the bi-directional switches of the matrix converter. Pulses for Sc1and Sc2 are at 3.75k Hz and pulses for Sm1 and Sm2 are at 60k Hz.

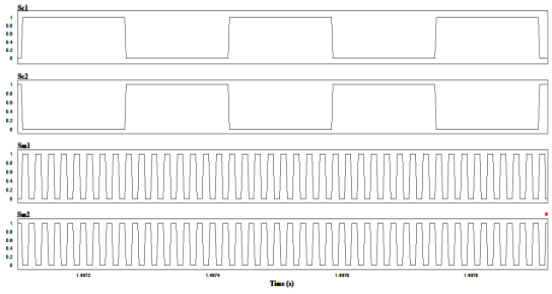


Figure 7: Switching pulses for Sc1,Sc2, Sm1and Sm2

Figure 8 shows the AC input voltage and current of the converter. RMS values of voltage and current are 10V and 7.06A respectively. At lower values of source voltage, inductor does not have enough energy to increase or decrease the current. This will introduce some distortion in the input current.

Vs= 10V, Is=7.06 A (rms)

Input power factor = 0.798

Total Harmonic distortion = 37.23%

Is,peak = 10A

Figure 4.4 shows the Harmonic of the input current. From the spectrum, it is clear that third order harmonics are present in the input current.

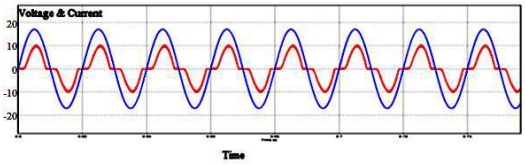


Figure 8: Input voltage and current

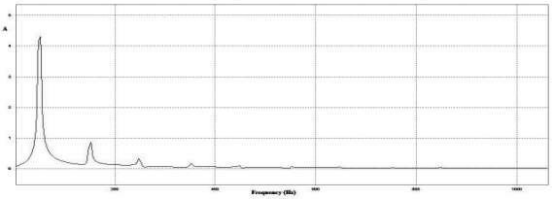


Figure 9: FFT Spectrum of input current

Figure 10 shows the DC output voltage and current. Average value of voltage and current is 50V and 0.26A respectively. Ripple in the output voltage is 2.5V.

Vo = 50V, Io = 0.26A

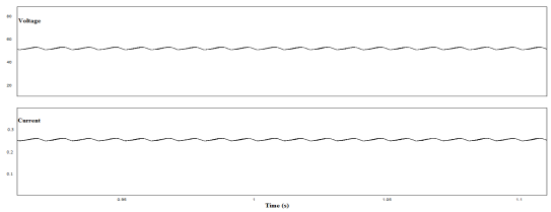
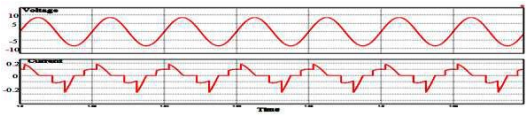


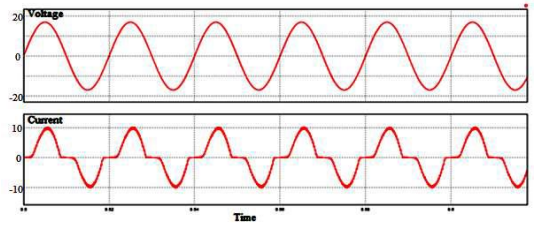
Figure 10: Output voltage and current

For comparison, a conventional two-stage voltage source CW multiplier with the identical input voltage and power was simulated along with the new converter topology. An ac source with 10 $Vrms$ was supplied to the conventional CW circuit. Figure 11 shows the simulated waveforms of the conventional CW circuit (Figure 11a) and the proposed converter at fc = 3.75 kHz (Figure 4.6b). The conventional CW circuit incurs high distorted line current, poor power factor, and high output ripple, while the proposed converter provides significantly good line conditions and rather low output ripple.



(a) For conventional CW voltage multiplier

THD =76.5 %
Input power factor =0.35



(b) At fc= 3.75 kHz

Figure 11: Simulated waveforms of Vs and Is for CW multiplier and proposed converter

VII. CLOSED LOOP SIMULATION

The control circuit of the converter consists of an outer current control loop for output voltage regulation and an inner current control loop for power factor correction. Figure 12 presents a block diagram of the control system for the converter, which includes a proportional-integral (PI) controller, to regulate the output voltage. The reference value iL,ref for the inner current loop is obtained from the multiplication between the output of the voltage controller and the absolute value |Vs(t)|. A hysteresis controller provides a fast control for the inductor current iL, resulting in a practically sinusoidal input current. The harmonics in the input current can be reduced by reducing the hysteresis width. Figure 13 shows the closed loop circuit diagram in PSIM.

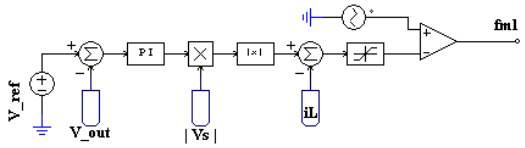


Figure 12: Control circuit

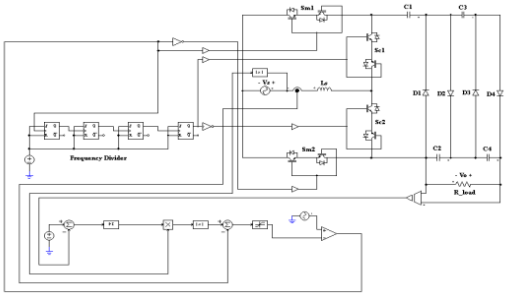


Figure 13: Closed loop Circuit Diagram

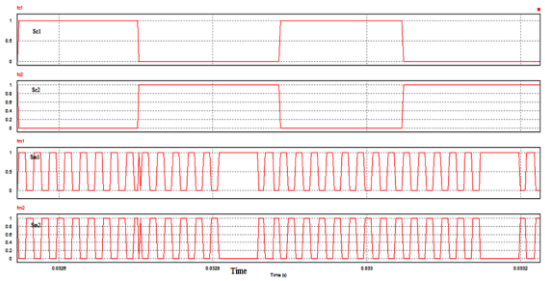


Figure 14: Closed loop switching pulses

Fig 14 shows the switching pulses for the four bi-directional switches of the matrix converter. Switching pulses for Sc1 and Sc2 are at 3.9k Hz and switching pulses for Sc1 and Sc2 are at 60kHz

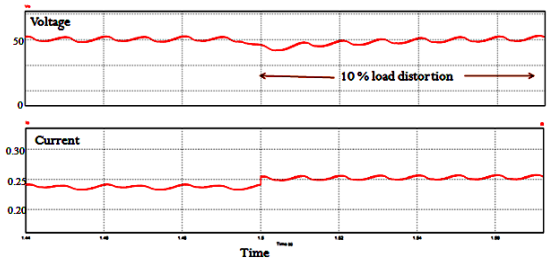


Figure 15: Voand Io when load distortion occurs.

Figure 15 shows the output voltage and current for 10% load variation. For 10% increase in load at 1.49 sec. the output voltage dipped to 38 V and at 0.5 sec, it attains original value 50V, with a ripple of 2.5 V.

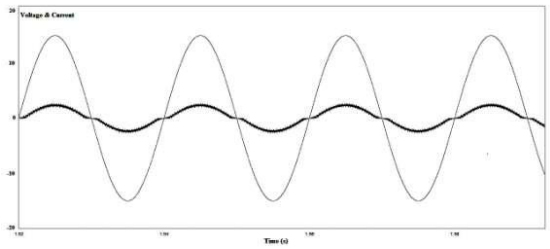


Figure 16: Input voltage and current in closed loop

Figure 16 shows the input voltage and current of the converter in closed loop. It is clear from the Figure that distortion in the input current is removed in closed loop and input power factor is improved.

Total Harmonic Distortion = 7.25%

Input power factor = 0.9

Is,peak = 4.5A

Figure 17 shows the FFT Spectrum of the input current. From Figure it is observed that harmonic distortion in the input current is reduced. Third order harmonics are eliminated from the input current.

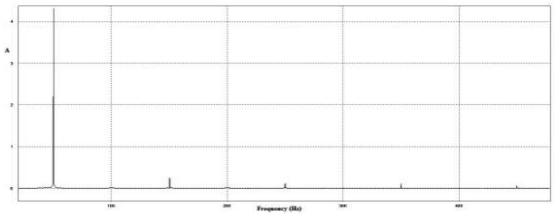


Figure 17: FFT Spectrum of Input current in closed loop

VIII. CONCLUSION

From the simulation results it is observed that with closed loop control, for 10% increase in load at 1.49 sec. the output voltage dipped to 38 V and at 0.5 sec, it attains original value 50V, with a ripple of 2.5 V. Supply power factor is found to be 0.925,

with peak supply current Is,peak as 4.A. From the FFT analysis, it is found that the third order harmonic is reduced by 75% and the THD is found to be 7.25%. The simulation results are tabulated in Table 5.1.

Converter \ Parameter			Input Power factor	THD (%)	Output Voltage Ripple
Conventional CW voltage Multiplier			0.38	76.5 %	32 V
Converter Based on CWVM and Matrix Converter	Open Loop	f_c =938 Hz	0.75	40.18 %	14 V
		f_c =1835 Hz	0.78	38.12 %	5.4 V
		f_c = 3750Hz	0.798	37.23	2.5 V
	Closed Loop (f_c = 3750Hz)		0.925	7.25	2. 5 V

Table 5.1 : Simulation Results

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