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Analysis and Reduction of Power using Gating Techniques Near Subthreshold Region

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Abstract: The sub-threshold and gate leakage power consumption in deep submicron CMOS systems are projected to become a significant part of the total power dissipation. This paper presents several dual-threshold voltage techniques for reducing standby power dissipation while still maintaining high performance. A dual-mode logic gate, for selectable operation in either of static and dynamic modes, includes: a static gate which includes at least one logic input and a logic output; a mode selector, configured for outputting a turn-off signal to select static mode operation and for outputting a dynamic clock signal to select dynamic mode operation and a switching element associated with the mode selector static gate, comprising a first input connected to a constant voltage, a second input for inputting the mode selection signal from the mode selector, and an output connected to a logic output of the static gate. The switching elements switches the logic gate operation from static to dynamic mode, by applying the appropriate signal to the switching element. As transistor sizes scale down and levels of integration increase, leakage power has become a critical problem in VLSI designs. In this paper, an industry-standard technique known as power-gating is explored, whereby transistors are used to disconnect the power from idle portions of a chip.This paper discusses the evolution of full adder circuits in terms of lesser power consumption high speed. The power gating techniques are implemented to design a full adder by reducing the number of transistors which also leads to the reduction of chip size.

Keywords: *Dual Mode Logic, Sub-threshold, Power Gating*

I. INTRODUCTION

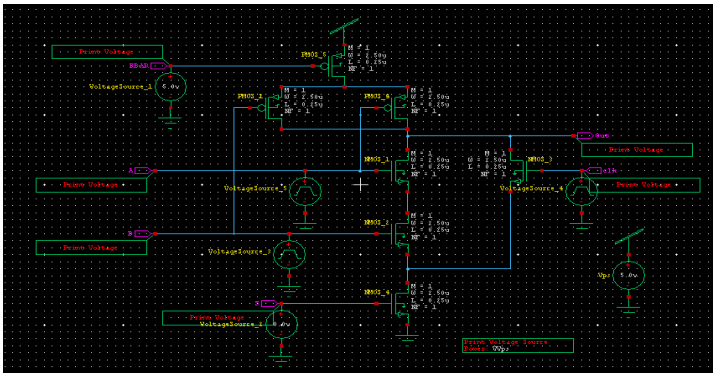
The power consumption has become a primary focus in the VLSI design. There are number of portable applications requiring small area low power high throughput circuitry. The sub-threshold logic technique is the main area for low power applications. The supply voltage of the sub-threshold region is less than the threshold voltages of the transistors so the static and dynamic power can be reduced. The dual mode logic (DML), which operates in the sub-threshold region. The DML logic can be operated in two modes: static CMOS like mode and dynamic np - CMOS- like mode. In the static mode the dual mode logic gate features very low power dissipation with moderate performance while in dynamic mode they attain higher performance, though with huge power dissipation. Low power utilization to be the most important for design of microprocessors and system mechanism addition is one of the fundamental arithmetic operations. It is used in many VLSI systems such as application specific DSP architectures and microprocessors.

II. POWER GATING TECHNIQUES

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing standby or leakage power, power gating has the benefit of enabling Iddq testing. Shutting down the blocks can be accomplished either by software or hardware. Driver software can schedule the power down operations. Hardware timers can be utilized. A dedicated power management controller is another option. An externally switched power supply is a very basic form of power gating to achieve long term leakage power reduction.

2.1.Sleep Method

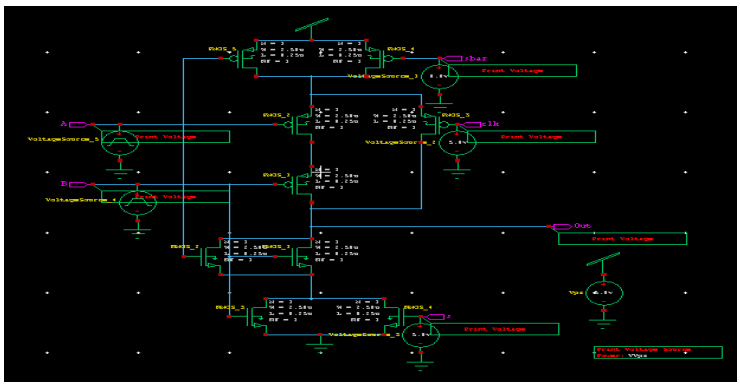
The Sleep method is the basic power gating method. The sleep transistors isolate the logic networks and the sleep transistor technique or the sleep method dramatically reduces leakage power during sleep mode. Fig.1 shows Type B Dynamic DML NAND with sleep gating technique.



Fig(1): Type B dynamic NAND sleep method

2.2.Sleepy Stack Method

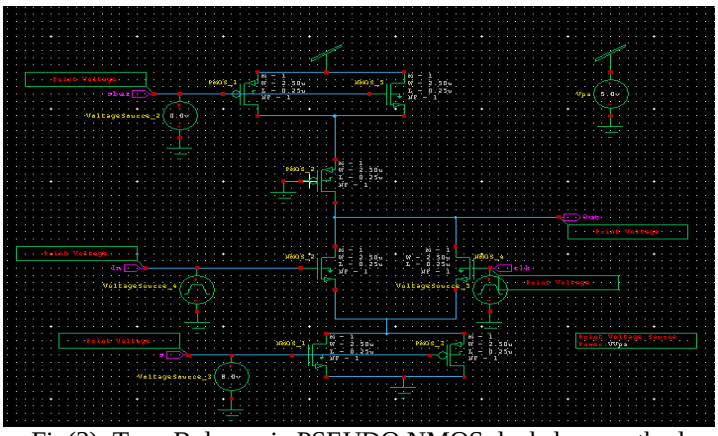
The sleepy stack approach merges the sleep and stack approaches. The sleepy stack technique splits the existing transistors into two half Size transistors like the stack approach. The activity of the sleep transistors in the sleepy stack method is same as the activity of the sleep transistors in the sleep method. The sleep transistors are turned on during the active mode and they are turned off during the sleep mode. Fig.2 shows Type A static NOR gate with Sleepy Stack Gating Technique.



Fig(2): Type A static NOR sleepy stack method

2.3.DualSleep Method

The Dual sleep approach has the advantage of using the two extra pull up and two extra pull down transistors in sleep mode either in OFF state or in ON state. In normal mode when S=1 the pull down NMOS transistor is in ON state and in the pull up network the PMOS sleep transistor is in ON state since S‟=0. During sleep mode state S is forced to 0 and hence the pull down NMOS transistor is in OFF state and PMOS transistor is in ON state and in the pull up network, PMOS sleep transistor is OFF while NMOS sleep transistor is ON. So in sleep mode state a PMOS is in series with an NMOS both in pull up network and pull down network which reduces the power dissipation. Fig.3 shows Type B Dynamic PSEUDO NMOS with Dual Sleep Gating Technique.



Fig(3): Type B dynamic PSEUDO NMOS dual sleep method

The NAND Dual mode logic gate is compared in terms of power consumption for different gating techniques like sleep method, sleepy stack method and dual sleep method in Table 1.

Gating Techniques / Modes	NAND SLEEP			NAND SLEEPY STACK			NAND DUAL SLEEP		
	0-2 v	2-5 v	5-50 v	0-2 v	2-5 v	5-50 v	0-2 v	2-5 v	5-50 v
Conventional	26 uW	42 uW	230 mW	200 uW	460 uW	270 mW	330 uW	820 uW	940 mW
Type A static	28 uW	44 uW	280 mW	350 uW	740 uW	310 mW	500 uW	1.2 mW	1000 mW
Type A dynamic	38 uW	60 uW	280 mW	330 uW	700 uW	310 mW	480 uW	1.1 mW	1000 mW
Type B static	320 uW	620 uW	290 mW	380 uW	840 uW	330 mW	350 uW	880 uW	900 mW
Type B dynamic	300 uW	640 uW	290 mW	370 uW	800 uW	340 mW	350 uW	840 uW	900 mW

Table(1): Comparison between NAND DML gates with different gating techniques

The NOR Dual mode logic gate is compared in terms of power consumption for different gating techniques in Table 2.

Gating Techniques / Modes	NOR SLEEP			NOR SLEEPY STACK			NOR DUAL SLEEP		
	0-2 v	2-5 v	5-50v	0-2 v	2-5 v	5-50v	0-2 v	2-5 v	5-50v
Conventional	180 uW	340 uW	190 mW	170 uW	370 uW	190 mW	320 uW	780 uW	190 mW
Type A static	230 uW	460 uW	320 mW	270 uW	580 uW	320 mW	400 uW	920 uW	320 mW
Type A dynamic	220 uW	440 uW	320 mW	230 uW	450 uW	320 mW	370 uW	900 uW	320 mW
Type B static	180 uW	350 uW	160 mW	160 uW	350 uW	160 mW	330 uW	780 uW	160 mW
Type B dynamic	180 uW	350 uW	160 mW	160 uW	370 uW	160 mW	330 uW	780 uW	160 mW

Table(2): Comparison between NOR DML gates with different gating techniques

The Pseudo nMOS logic is compared in terms of power consumption for different gating techniques in Table 3.

Gating Techniques / Modes	PSEUDO NMOS SLEEP			PSEUDO NMOS SLEEPY STACK			PSEUDO NMOS DUAL SLEEP		
	0-2 v	2-5 v	5-50 v	0-2 v	2-5 v	5-50 v	0-2 v	2-5 v	5-50 v
Conventional	130 uW	240 uW	170 mW	15 uW	25 uW	170 mW	270 uW	700 uW	170 mW
Type A static	10 uW	15 uW	240 µW	200 uW	450 uW	240 µW	340 uW	860 uW	240 µW
Type A dynamic	19 uW	30 uW	500 µW	170 uW	400 uW	500 µW	320 uW	840 uW	500 µW
Type B static	8 uW	12 uW	200 µW	82 uW	210 uW	200 µW	280 uW	680 uW	200 µW
Type B dynamic	16 uW	25 uW	400 µW	100 uW	240 uW	400 µW	280 uW	680 uW	400 µW

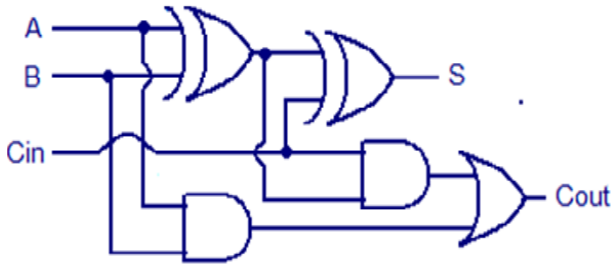
Table(3): Comparison between PSEUDO NMOS DML gates with different gating techniques

III. FULL ADDER CIRCUITS

A one-bit full adder adds three one-bit numbers, and it is written as A, B, and C_{in}. A and B are the operands, and C_{in} is a bit carried in from the previous less significant stage. The full adder is a component in a cascade of adders, which adds 8, 16, 32, etc. bits binary numbers. The circuit produces a two-bit outputs. The outputs are carry and sum typically represented by the signals C_{out} and *S*. The expression for sum and carry can be represented as,

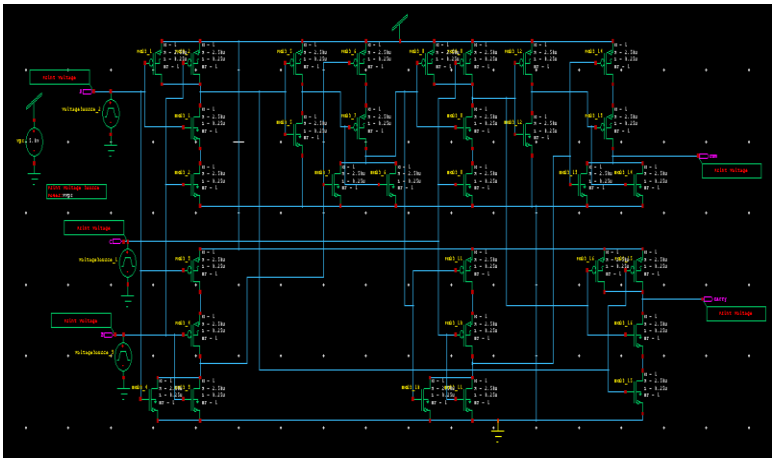
$$\text{Sum} = A \oplus \text{B} \oplus \text{C}$$
$$Carry = (A.B) + (C\ (A \oplus B))$$

The full adder consists of two half adders and one OR gate. The circuit diagram for one bit full adder is shown in fig.4.



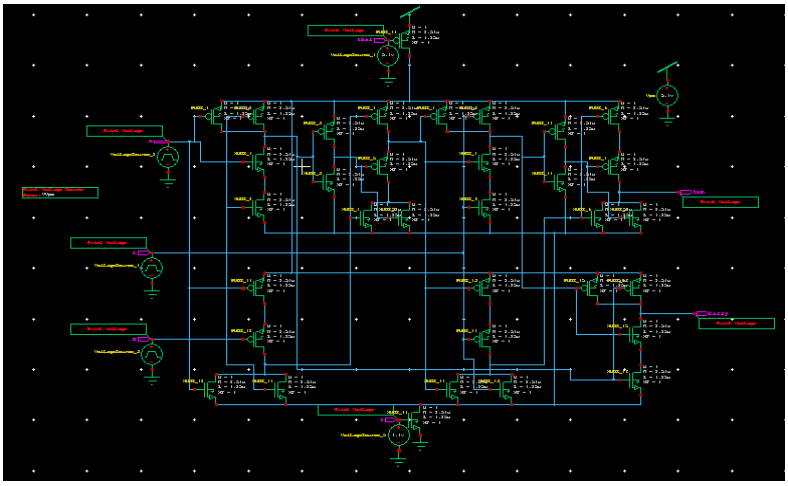
Fig(4): 1-bit Full Adder

The conventional full adder is a basic full adder and it consists of 32 transistors. The schematic of conventional full adder is shown in Fig.5.



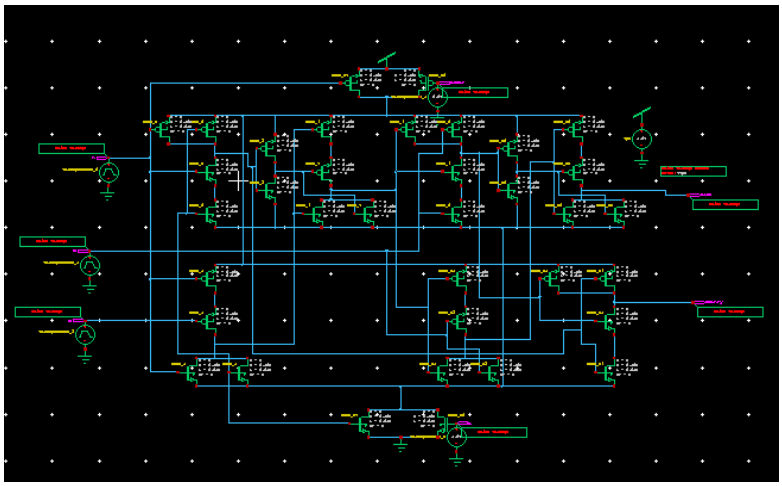
Fig(5): Schematic of Conventional Full Adder

The full adder sleep method consists of 34 transistors. The power gating technique is used to reduce the leakage power by placing the sleep transistor between actual ground rail and circuit ground. The low leakage NMOS is used as a sleep transistor. The sizing of the transistor reduces the standby leakage current to a very great extent. The major drawback of sleepy technique is it cannot retain the values when it enters into sleep mode, since there will be no supply the output values cannot be retained. For combinational circuits it will be fine but for sequential circuits it will fail as they depends on previous outputs. The schematic of full adder sleep method is shown in Fig.6.



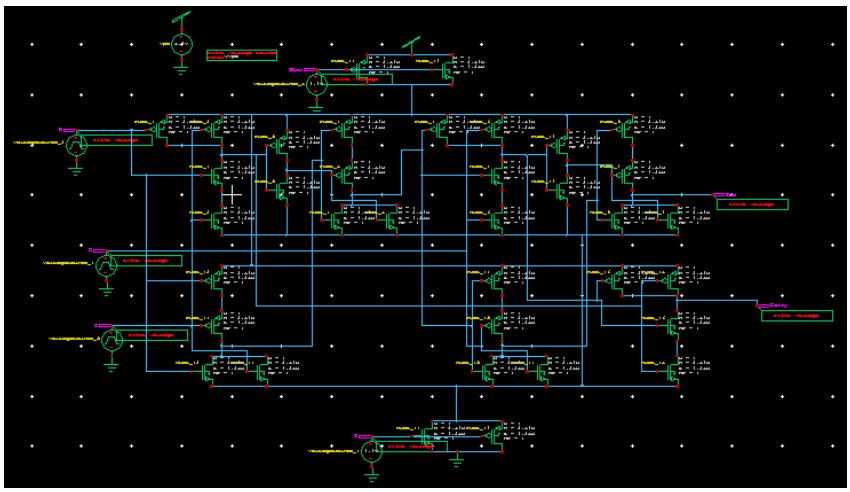
Fig(6): Schematic of Full Adder Sleep method

The full adder sleepy stack method consists of 36 transistors. The drawback of sleep method is avoided by using sleepy stack method. In active mode the dissipation of power is active power. The active power consists of dynamic power as well as static power. so it is named as an active power. In static mode the both header and footer switches will be off there will be no V_{dd} supply and ground connected to the circuit. So the power dissipation will be very less. The schematic of full adder sleepy stack method is shown in fig.7.



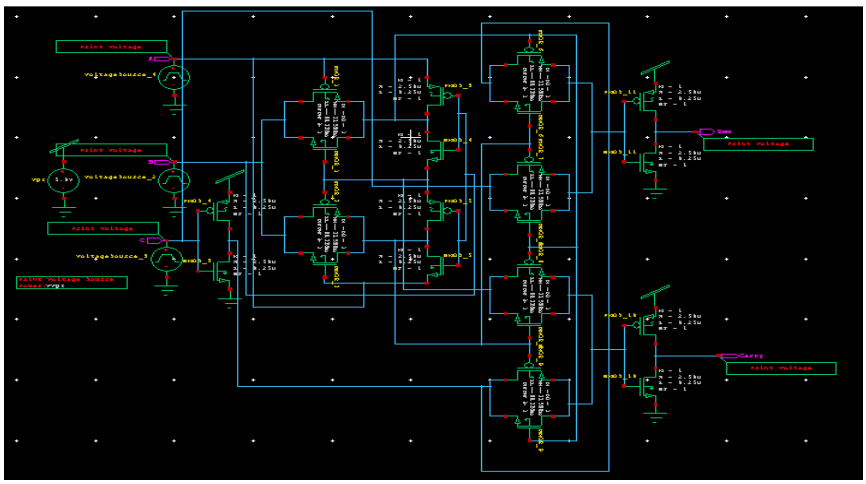
Fig(7): Schematic of Full Adder Sleepy Stack method

The full adder dual sleep method consists of 36 transistors. Two sleep transistors in every NMOS or PMOS block are used. One sleep transistor is in ON state and alternative is in OFF state. Once more in OFF state a block containing each PMOS and NMOS transistors are utilized in order to scale back the outflow power. The schematic of full adder dual sleep method is shown in fig.8.



Fig(8): Schematic of Full Adder Dual Sleep method

The transmission gate full adder consists of 22 transistors. The transmission gate full adder enforced with minimum number of transistors compared to conventional full adder design. The consecutive connected PMOS and NMOS arrangement act as a switch and is thus referred to as transmission gate. A transmission gate or analog switch is an electronic element that will selectively block or pass a signal level from the input to the output. The schematic of transmission gate full adder is shown in fig.9.



Fig(9): Schematic of Transmission Gate Full Adder

The power analysis of different gating techniques is shown in Table 4.

Circuit	Power (mW)
Conventional Full Adder	30
Full Adder Sleep method	0.7
Full Adder Sleepy Stack	9.4
Full Adder Dual Sleep	3.1
Full Adder Transmission Gate	12

Table (4): Power analysis of different Power Gating Techniques

IV. CONCLUSION

The result obtained leads to the conclusion that while operating in the dynamic mode, sub threshold DML gates achieve an improvement in speed compared to a standard CMOS, while dissipating more power and in the static mode, a reduction of power dissipation is achieved, at the expense of a decrement in performance. The different methods of power gating applied to the DML logic have reduced the power dissipation.

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