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Design And Simulation of Three-Phase Diode Clamped And Improved Inverter Fed Asynchronous Motor Drive With Three-Level Configurations

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Abstract: - This paper presents the study of Three-phase Three-Level inverter topology fed Asynchronous motor drive. Three-level configurations are realized by Diode clamped and Improved multilevel inverter topologies. The poor quality of voltage and current of a conventional inverter fed induction machine is due to the presence of harmonics and hence there is significant level of energy losses. The Multilevel inverter configurations are used to reduce the harmonics by means of synthesizing the output waveforms. The inverters modes of operations are discussed under single phase one leg voltage circuit analysis. The three-phase asynchronous motor is analysed under a split-single phase asynchronous motor. The higher levels can be modulated by comparing a sinusoidal reference signal and multiple triangular carrier signals by means of pulse width modulation technique. The simulation of three-phase three-level inverters fed induction motor model are done using Matlab/Simulink. The results of rotor currents, stator currents, rotor speed, electromagnetic torque and three-phase output voltages are plotted. Furthermore, the numbers of circuit component counts in different inverter topologies are obtained.

Keywords: *Asynchronous motor, Multilevel Inverter, Pulse width modulation, Speed, Three-phase, Torque.*

I. INTRODUCTION

Nowadays, there are many applications for multilevel inverter topologies, such as Flexible AC Transmission Systems (FACTS), High Voltage Direct Current (HVDC) transmission, electrical drives such as speed control of three-phase water pump, conveyor systems, machine tools, and Dispersed Generation (DG) systems. A multilevel inverter is a power electronic device built to synthesize a desired AC voltage from several levels of DC voltages. Such inverters have been the subject of research in the recent years where the DC levels were considered to be identical in that all of them were capacitors, batteries, solar cells, etc. In Recent Years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [1], [2]. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with staircase waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig. 1 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions.

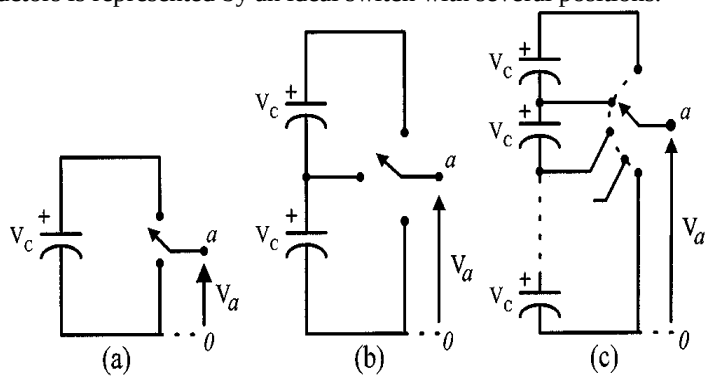

Fig. 1 One phase leg of an inverter with (a) two-level, (b) three-level, and (c) n-level.

A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor and the voltages are zero and V_C (see Fig. 1(a)), while the three-level inverter generates three voltages as zero,V_C, $2V_C$ (see fig. 1(b)) and n-level inverter generates zero, V_C, $2V_C$, $3V_C$… (n-1) V_C (see fig. 1(c)).

Considering that m is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load is K

$$K=2m-1 \quad (1)$$

and the number of steps p in the phase voltage of a three-phase load in wye connection is

$$p=4m-3 \quad (2)$$

The term multilevel starts with the least member which is three-level inverter as introduced by Nabae I t. [3]. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion with high switching losses. However, a high number of levels increases the control complexity and introduces voltage imbalance problems. Three different topologies have been proposed for multilevel inverters: diode-clamped (neutral-clamped) [3]; capacitor-clamped (flying capacitors) [1], [4]; and cascaded H-bridge with separate dc sources [1], [5]. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multi-carrier sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination, and space-vector modulation (SVM).

II. THREE-PHASE MULTILEVEL INVERTER TOPOLOGIES

A. Diode-clamped multilevel inverter:

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. One phase of a three-level diode clamped inverter is shown in Fig. 2.

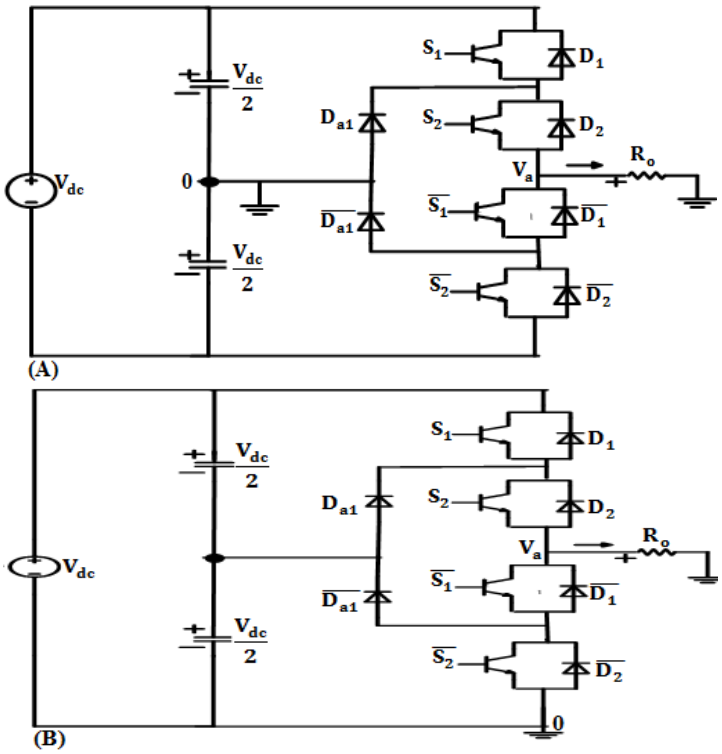

Fig. 2 One Phase of three-Level diode clamped inverter topology

As it is shown in the circuit above, in this type of multilevel we have only one DC-source and the DC-bus is split into n-level by n-1 capacitors. Here n= 3 and we have two capacitors. Fig. 2(A) represents half-wave circuit topology for three-level diode clamped inverter. Consequently, the output phase voltage has the following: $\frac{V_{dc}}{2}$, 0, -$\frac{V_{dc}}{2}$,. To explain how the staircase voltage is synthesized in fig. 2(A) above, the neutral point *0* is considered as the output phase voltage reference point. There are two switch combinations to synthesize two level voltages across V_a and 0. Firstly, for voltage level $V_{a0} = \frac{V_{dc}}{2}$, turn on all upper switches S_1 and S_2, secondly, for voltage level $V_{an} = -\frac{V_{dc}}{2}$, turn on all lower switches $\bar{S}_1$and $\bar{S}_2$and finally, for voltage level Van = 0,

turn on two middle switches S_2 and $\bar{S}_1$. Fig. 2(B) represents full-wave circuit topology for three-level diode clamped inverter. The output phase voltage has three-levels with negative reference: $\frac{V_{dc}}{2}$, V_{dc}, 0. To explain how the staircase voltage is synthesized in fig. 2(B) above, the neutral point *0* is considered as the output phase voltage reference point. There are two switch combinations to synthesize two level voltages across V_a and 0. Firstly, for voltage level $V_{a0} = \frac{V_{dc}}{2}$, turn on two middle switches S_2 and $\bar{S}_1$, secondly, for voltage level $V_{an} = V_{dc}$, turn on all upper switches S_1 and S_2, and finally, for voltage level $V_{an} = 0$, turn on all lower switches $\bar{S}_1$and $\bar{S}_2$. Fig. 2(B) represents full-wave circuit topology for three-level diode clamped inverter. There are two clamping diodes (D_{a1} and $\bar{D}_{a1}$) and four anti-parallel diodes (D_1 , D_2, $\bar{D}_1$ and $\bar{D}_2$). These clamping diodes clamp the switching voltage to half level of the dc-bus voltage. The neutral point 0 is considered as the reference point [6]. To produce a three-level voltage, two switch combinations must be used. Although each active switching device is only required to block a voltage level of $\frac{V_{dc}}{(n-1)}$, the clamping diodes must have different voltage rating for reverse voltage blocking [7]. So if diodes with same voltage rating as the active devices are used, the number of required diodes for each phase will be 2(2n-3) and the number of power switches are given by 2(n-1). This number represents a linear increment and when n is sufficiently high, the number of diodes required will make the system impractical to implement and if the inverter runs under PWM, the diodes reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications [7]. Fig. 2(B) above can be extended to three-phase circuit configuration by interconnection of another two-phase circuit to get V_b andV_c, and the control logic circuit is achieved by phase-shifting phase -A by 120° and 240° respectively.

B. **Improved multilevel inverter:** This inverter topology consists of a diode embedded bidirectional switches, half H-bridge convectional inverter circuit and two bank capacitors.

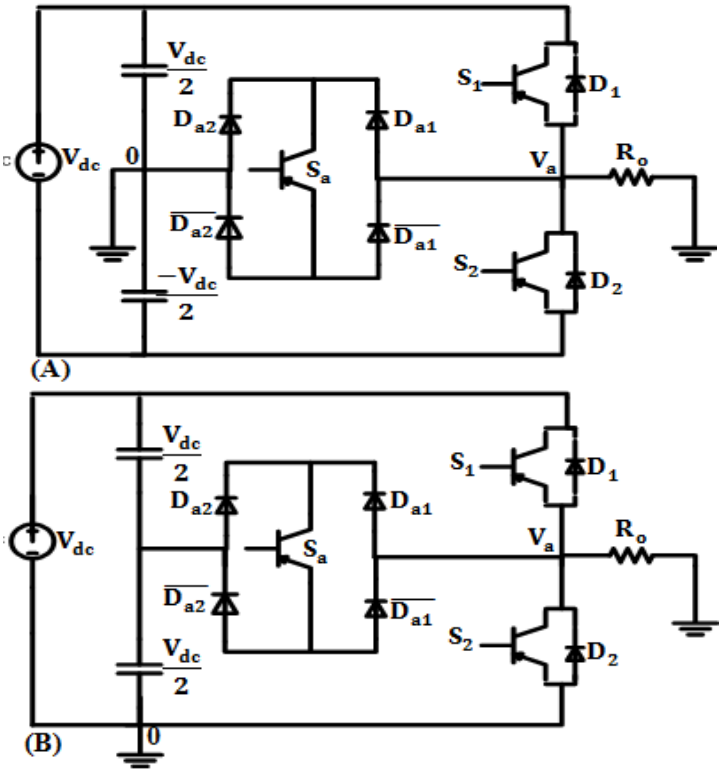

Fig. 3. One Phase of three-Level Improved inverter topology.

As it is shown in the circuit above, in this type of multilevel we have only one DC-source and the DC-bus is split into n-level by n-1 capacitors. Here n= 3 and we have two capacitors. Fig. 3(A) represents half-wave circuit topology for three-level improved inverter. Consequently, the output phase voltage has the following: $\frac{\mathbf{V_{dc}}}{\mathbf{2}}$, 0, -$\frac{\mathbf{V_{dc}}}{\mathbf{2}}$,. To explain how the staircase voltage is synthesized in fig. 3(A) above, the neutral point *0* is considered as the output phase voltage reference point. The output voltage can be synthesized as follows: Firstly, for voltage level $\mathbf{V_{a0}} = \frac{\mathbf{V_{dc}}}{\mathbf{2}}$, turn on the upper switch $\mathbf{S_1}$, secondly, for voltage level $\mathbf{V_{an}}$ = -$\frac{\mathbf{V_{dc}}}{\mathbf{2}}$, turn on lower switch $\mathbf{S_2}$ and finally, for voltage level $\mathbf{V_{an}}$ = 0, turn on the middle switch $\boldsymbol{S_a}$. Fig. 2(B) represents full-

wave circuit topology for three-level improved inverter. The output phase voltage has three-levels with negative reference: $\frac{\mathbf{V_{dc}}}{\mathbf{2}}$, $\mathbf{V_{dc}}$, 0. Furthermore, fig. 3(B) depicts full-wave three-level improved inverter topology with output voltage of 0, $\frac{\mathbf{V_{dc}}}{\mathbf{2}}$, and $\mathbf{V_{dc}}$. Thus, the proposed inverter synthesizes one and half levels of the dc bus voltage. To obtain the maximum positive output voltage $\mathbf{V_{a0}} = \boldsymbol{V_{dc}}$, $\boldsymbol{S_1}$ is turned ON, to obtain the half-positive output voltage $\mathbf{V_{a0}} = \frac{\mathbf{V_{dc}}}{\mathbf{2}}$, $\boldsymbol{S_a}$ is turned ON and, $\mathbf{V_{a0}} = 0$, when $\boldsymbol{S_2}$ is turned ON. If diodes with same voltage rating as the active devices are used, the number of required diodes for each phase will be 2(2n-3) and the number of power switches are given by n, where n is the number of the inverter output voltage level.

III. THREE-PHASE ASYNCHRONOUS MOTOR

Asynchronous machines are widely used in industries. Induction motors have their characteristic during starting and fault conditions [8]. At this study a kind of squirrel cage asynchronous machine from the library of MATLAB/Sims Power is used as a load for our multilevel inverters. Synchronous speed of Asynchronous Motor varies directly proportional to the supply frequency. Hence, by changing the frequency, the synchronous speed and the motor speed can be controlled below and above the normal full load speed. The voltage induced in the stator, E is directly proportional to the product of slip frequency and air gap flux. The Asynchronous Motor terminal voltage can be considered proportional to the product of the frequency and flux, if the stator voltage is neglected. Any reduction in the supply frequency without a change in the terminal voltage causes an increase in the air gap flux. Asynchronous motors are designed to operate at the knee point of the magnetization characteristic to make full use of the magnetic material. Therefore the increase in flux will saturate the motor. This will increase the magnetizing current, distort the line current and voltage, increase the core loss and the stator copper loss, and produce a high pitch acoustic noise. While any increase in flux beyond rated value is undesirable from the consideration of saturation effects, a decrease in flux is also avoided to retain the torque capability of the motor. Therefore, the pulse width modulation (PWM) control below the rated frequency is generally carried out by reducing the machine phase voltage, V, along with the frequency in such a manner that the flux is maintained constant. Above the rated frequency, the motor is operated at a constant voltage because of the limitation imposed by stator insulation or by supply voltage limitations [9]. In this paper split-phase single-phase Asynchronous Motor is used as inverter load throughout the simulation process.

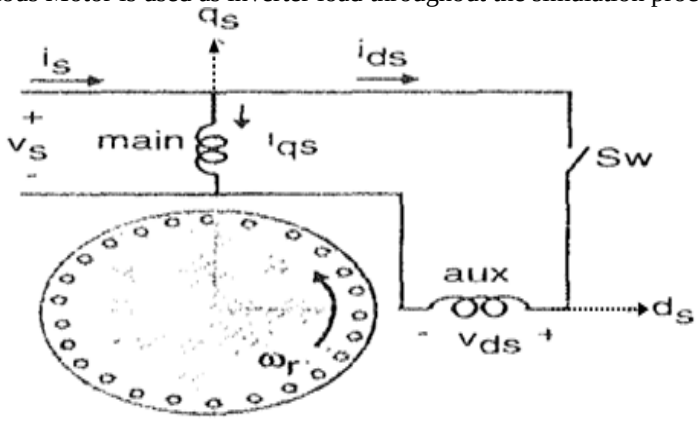

Fig. 4. Split-phase Single-phase Asynchronous Motor.

A three-phase symmetrical induction motor upon losing one of its stator phase supplies while running may continue to operate as essentially a single-phase motor with the remaining line-to-line voltage across the other two connected phases. When the main winding coil is connected in parallel with ac voltage, as in the split-phase single-phase asynchronous motor of fig. 4, the current of the auxiliary winding, $\boldsymbol{i_{ds}}$, leads $\boldsymbol{i_{qs}}$ of the main winding. For even a larger single-phase induction motor, that lead can be further increased by connecting a capacitor in series with the auxiliary winding, this arrangement brings about a Capacitor-start single-phase asynchronous motor. Fig. 4 shows that the motor has two windings: the main (running) winding and the auxiliary (starting) winding. This motor is modeled in two parts: Electrical part which is represented by a fourth-order state-space model and, mechanical part which is represented by second-order system. All electrical variables and parameters are referred to the stator. This is indicated by the prime signs in the machine equations given below. All stator and rotor quantities are in the stator reference frame (d-q frame).

Electrical System Part Analysis:

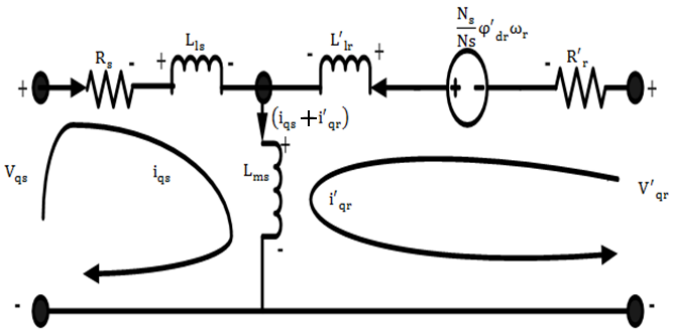

Fig. 5 Main winding (q-axis) circuit diagram

$$\mathbf{V_{qs} = R_s i_{qs} + \frac{d}{dt}\varphi_{qs}} \quad (3)$$

Where, $\boldsymbol{\varphi_{qs} = (L_{ls} + L_{ms})i_{qs} + L_{ms}i'_{qr}}$

$$\mathbf{V'_{qr} = R'_r i'_{qr} + \frac{d}{dt}\varphi'_{qr} - \frac{N_s}{Ns}\omega_r\varphi'_{dr}} \quad (4)$$

Where, $\boldsymbol{\varphi'_{qr}}$=$\mathbf{(L'_{lr} + L_{ms})i'_{qr} + L_{ms}i_{qs}}$

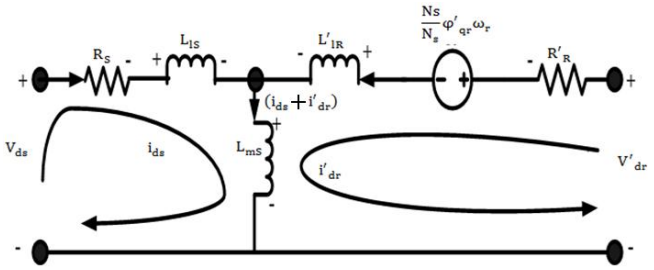

Fig. 6 Auxiliary winding (d-axis) circuit diagram

$$\mathbf{V_{ds} = R_S i_{ds} + \frac{d}{dt}\varphi_{ds}} \quad (5)$$

Where, $\boldsymbol{\varphi_{ds} = (L_{lS} + L_{mS})i_{ds} + L_{mS}i'_{dr}}$

$$\mathbf{V'_{dr} = R'_R i'_{dr} + \frac{d}{dt}\varphi'_{dr} + \frac{Ns}{N_s}\omega_r\varphi'_{qr}} \quad (6)$$

Where, $\boldsymbol{\varphi'_{dr} = (L'_{lR} + L_{mS})i'_{dr} + L_{mS}i_{ds}}$

$$\mathbf{T_e = p(\frac{Ns}{N_s}\varphi'_{qr}i'_{dr} - \frac{N_s}{Ns}\varphi'_{dr}i'_{qr})} \quad (7)$$

Mechanical System part Analysis

$$\boldsymbol{\frac{d}{dt}\omega_m = \frac{1}{2H}(T_e - F\omega_m - T_L)} \quad (8)$$

$$\boldsymbol{\frac{d}{dt}\theta_m = \omega_m} \quad (9)$$

It is vital to note that the reference frame fixed in the stator is used to convert voltages and currents to the dq frame, this enables for easier model analysis of the system. The following relationships describe the ab-to-dq frame transformations applied to the single phase asynchronous machine.

$$\begin{bmatrix} f_{qs} \\ f_{ds} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}\begin{bmatrix} f_{as} \\ f_{bs} \end{bmatrix} \quad (10)$$

$$\begin{bmatrix} f_{qr} \\ f_{dr} \end{bmatrix} = \begin{bmatrix} \cos\theta_r & -\sin\theta_r \\ -\sin\theta_r & -\cos\theta_r \end{bmatrix}\begin{bmatrix} f_{ar} \\ f_{br} \end{bmatrix} \quad (11)$$

The variable f can represent either voltage, current or flux linkage. The single phase asynchronous machine block parameters as shown in fig. 7 are defined as follows (all quantities are referred to the stator):

Table 1 Definition Of Symbols In Asynchronous Motor Model

Para-meters	Definitions	units
$\mathbf{R_s, L_{ls}}$	Main winding stator resistance and leakage inductance	
$\mathbf{R_S, L_{lS}}$	Auxiliary winding stator resistance and leakage	$\boldsymbol{\Omega\ and}$ H

	inductance	
$\mathbf{R'_r, L'_{lr}}$	Main winding rotor resistance and leakage inductance	
$\mathbf{R'_R, L'_{lR}}$	Auxiliary winding rotor resistance and leakage inductance	
$\mathbf{L_{ms}}$	Main winding magnetizing inductance	H
$\mathbf{L_{mS}}$	Auxiliary winding magnetizing inductance	
$\mathbf{V_{as}, i_{as}}$ $\mathbf{V_{bs}, i_{bs}}$ $\mathbf{V_{qs}, i_{qs}}$ $\mathbf{V_{ds}, i_{ds}}$ $\mathbf{V'_{qr}, i'_{qr}}$ $\mathbf{V'_{dr}, i'_{dr}}$	Main winding stator voltage and current Auxiliary winding stator voltage and current q-axis stator voltage and current d-axis stator voltage and current q-axis rotor voltage and current d-axis rotor voltage and current	V and A
$\boldsymbol{\varphi_{qs}, \varphi_{ds}}$	Stator q and d-axis fluxes	V.s
$\boldsymbol{\varphi'_{qr}, \varphi'_{dr}}$	Rotor q and d-axis fluxes	V.s
$\boldsymbol{\omega_m}$	Rotor angular velocity	Rad/sec
$\boldsymbol{\theta_m}$	Rotor angular position	rad
p	Number of pair poles	
$\boldsymbol{\omega_r}$	Electrical angular velocity ($\boldsymbol{\omega_r * p}$)	Rad/sec
$\boldsymbol{\theta_r}$	Electrical rotor angular position ($\boldsymbol{\theta_r * p}$)	rad
$\boldsymbol{T_e}$	Electromagnetic torque	Nm
$\boldsymbol{T_m}$	Shaft mechanical torque	Nm
J	Combined rotor and load inertia coefficient. Set to infinite to simulate locked rotor	Kg.m^2
F	Combined rotor and load viscous friction coefficient	Nms
H	Combined rotor and load inertia constant. Set to infinite to simulate locked rotor	sec
Ns	Number of auxiliary winding's effective turns	turns
$\boldsymbol{N_s}$	Number of main winding's effective turns	Turns

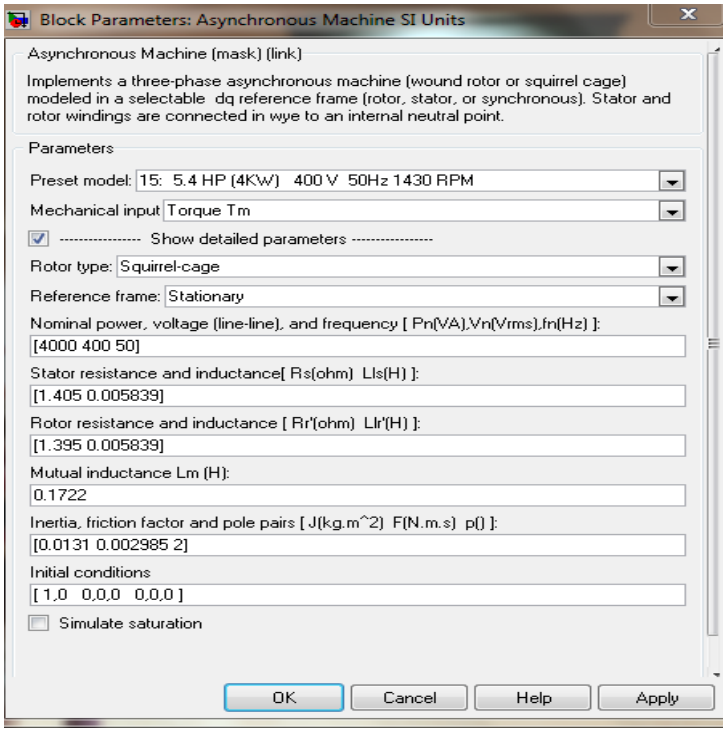

Fig. 7 A three-phase Squirrel-cage asynchronous motor parameter.

IV. MATLAB SIMULINK SIMULATION RESULTS

Multilevel inverter fed asynchronous motor drive is implemented in MATLAB/ SIMULINK which is shown in fig. 8. The MATLAB/ SIMULINK model of diode clamped and improved three-phase multilevel inverter using three-level configuration topology is shown in fig. 8. The logic algorithm for firing each of the circuit topology is embedded in the logic circuit and also different inverter configurations are also embedded in the diagram with a name as multilevel invereter topology. Voltmeter is attached between the inverter output terminal and motor input terminal, this helps to measure the inverter ouput readings and machine input voltages.

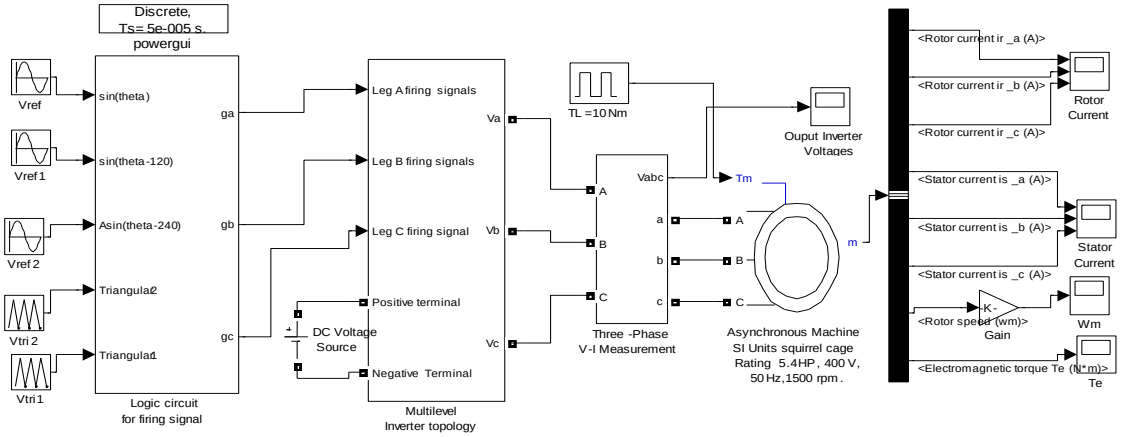

Fig. 8 Matlab/Simulink model of Multilevel Asynchronous Motor drive.

Diode clamped three phase three-level inverter output voltage after feeding to synchronous motor is shown in fig. 9. The stator main and rotor winding output currents with respect to three-phase are shown in fig. 10. The variation of speed and torque are also shown. The inverter output voltage which serves as the machine input voltage is also plotted in fig.10. The machine starts at no load and then at t=0.20secs, once the machine has reached its steady state, the load torque is increased to its nominal value (10 N.m) in 1.0 sec. The speed increases and settles at 1500 rpm without torque load and drops to 1450 rpm when loaded with torque load.

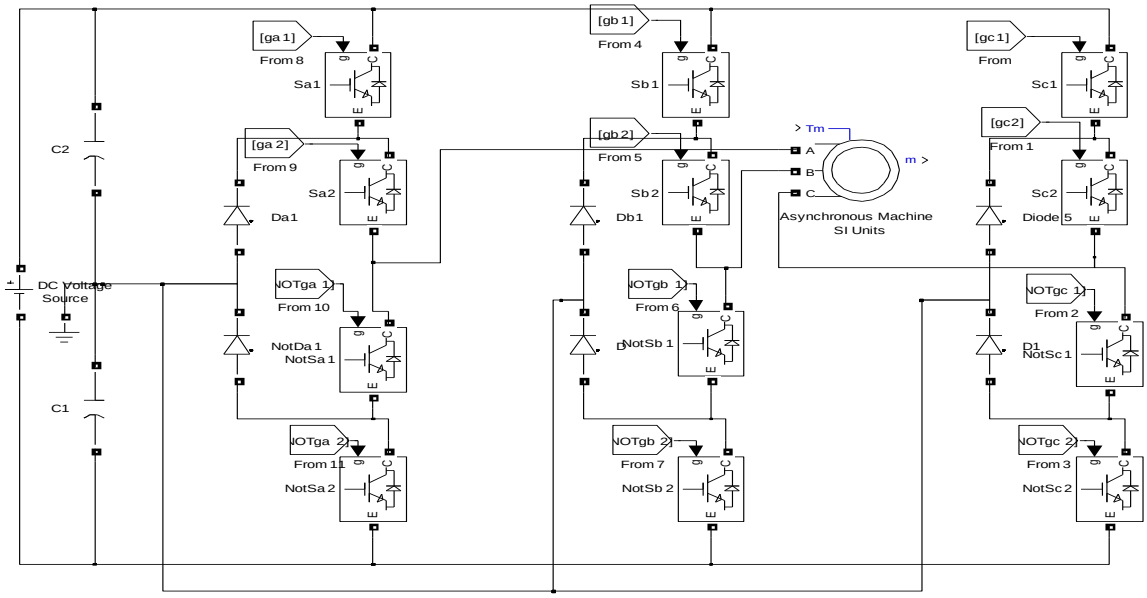

Fig. 9 Matlab/Simulink model of Diode clamped Three-phase Three-level Inverter.

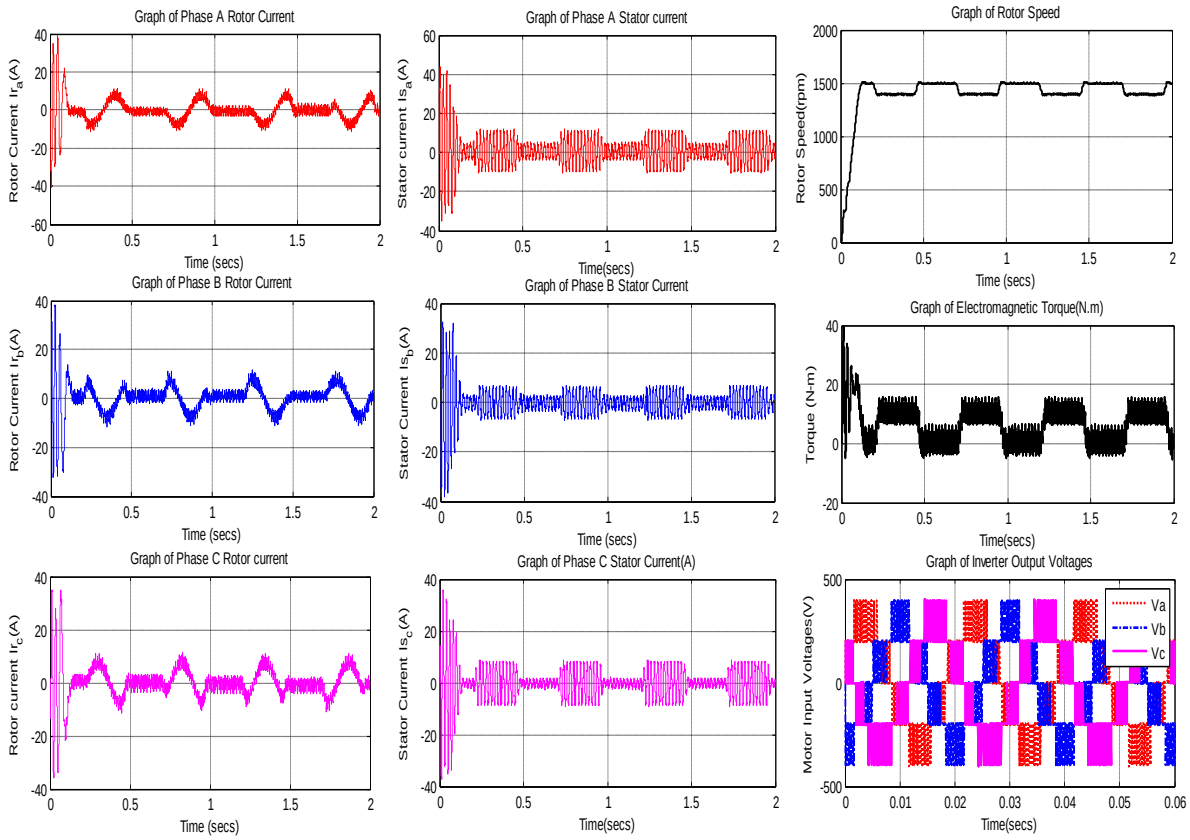

Fig. 10a Diode Clamped Multilevel Inverter Topology Simulation Results.

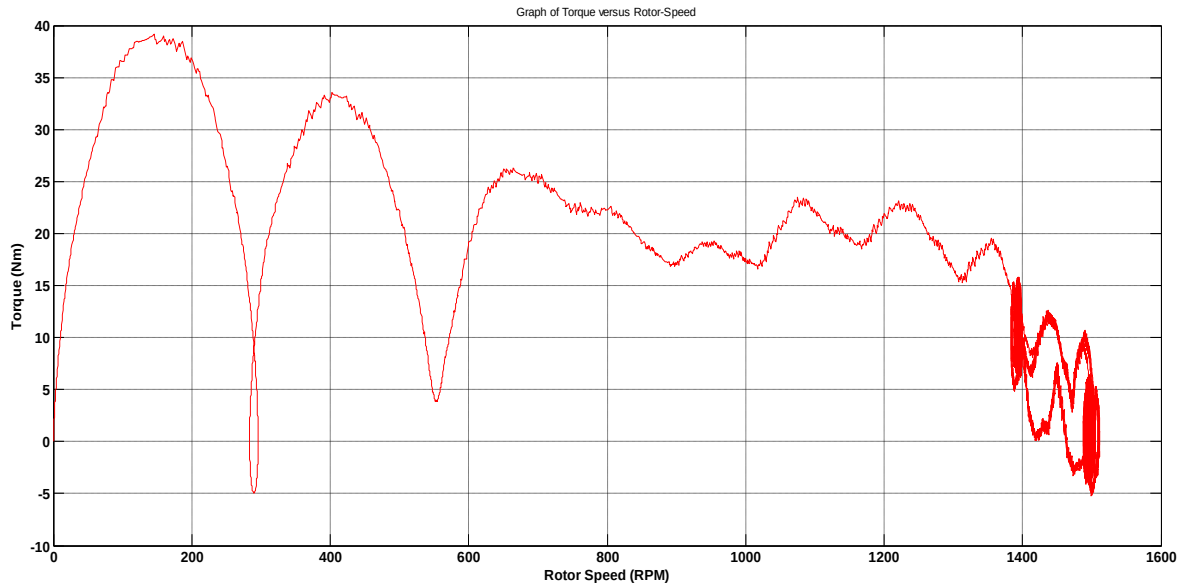

Fig. 10b A Waveform for Torque versus Rotor Speed

An Improved three phase three-level inverter output voltage after feeding to asynchronous motor is shown in fig. 11. The stator main and rotor winding output currents with respect to three-phase are shown in fig. 12. The variation of speed and torque are also shown. The inverter output voltage which serves as the machine input voltage is also plotted in fig.12. The machine starts at no load and then at t=2.0secs, once the machine has reached its steady state, the load torque is increased to its nominal value (10 N.m) in 1.0 sec. The speed increases and settles at 1500 rpm without torque load and drops to 1450 rpm when loaded with torque load.

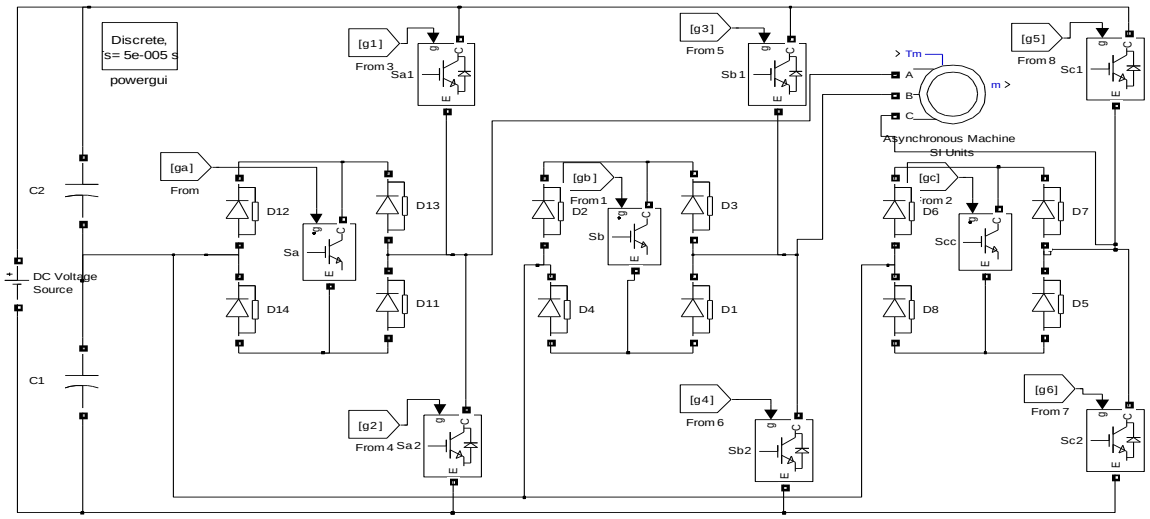

Fig. 11 Matlab/Simulink model of An Improved Three-phase Three-level Inverter.

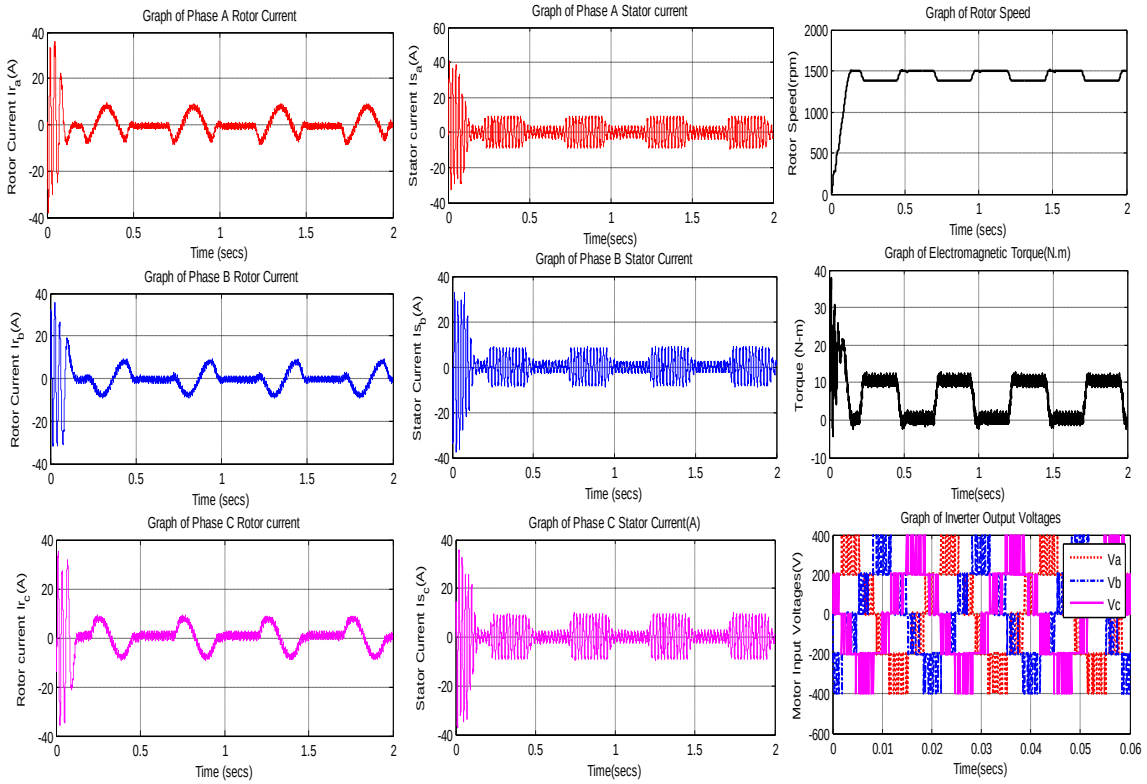

Fig. 12a An Improved Multilevel inverter topology simulation results.

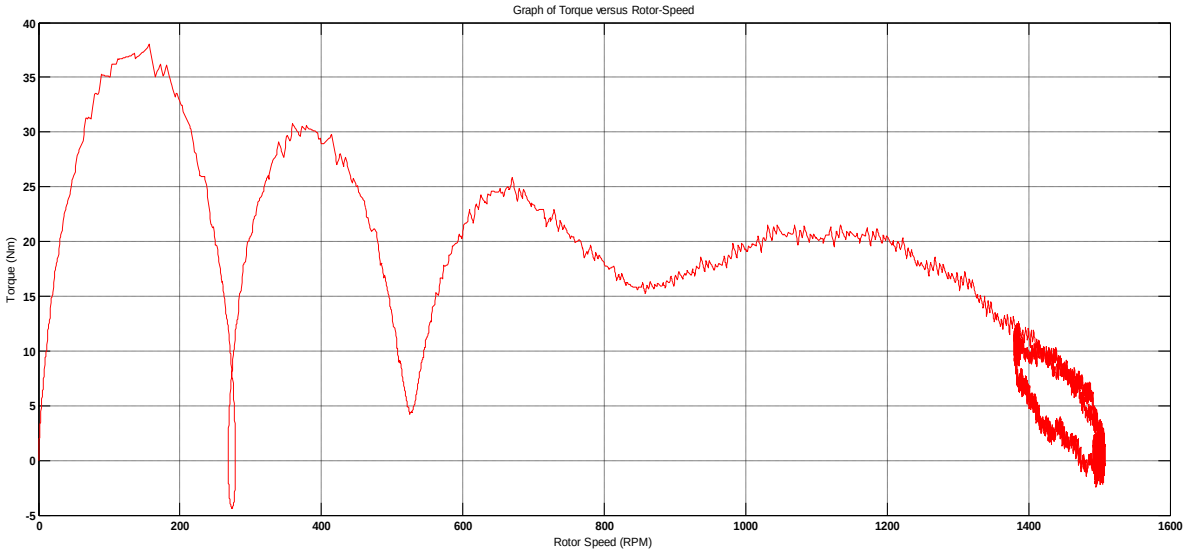

Fig. 12b Waveform for Torque versus Rotor Speed

4.1 NUMBER OF COMPONENT COUNT.

The number of required three-phase multilevel inverter components according to output voltage levels (N) is illustrated in table 2. Analysis from Table 2 clearly shows that the numbers of components in this proposed configuration are lower than any other configuration.

Table 2: NUMBER OF COMPONENTS FOR THREE-PHASE MULTILEVEL INVERTER

Inverter Type/components	Diode Clamped	Flying Capacitor	Cascaded H-bridge	Improved
Main Switches	$\mathbf{3(3N-5)}$	$\mathbf{3(3N-5)}$	$\mathbf{3(3N-5)}$	$\mathbf{3N}$
Main Diodes	$\mathbf{3(3N-5)}$	$\mathbf{3(3N-5)}$	$\mathbf{3(3N-5)}$	6
Clamping Diodes	$\mathbf{6(N-2)}$	0	0	$\mathbf{12(N-2)}$
DC bus Capacitor/isolate supplies	$\mathbf{N-1}$	1	$\mathbf{N-1}$	$\mathbf{N-1}$
Flying capacitors	0	$\mathbf{2(N-2)}$	0	0
Total Numbers	$\mathbf{2(17N-26)}$	$\mathbf{20N-33}$	$\mathbf{19N-31}$	$\mathbf{16N-7}$

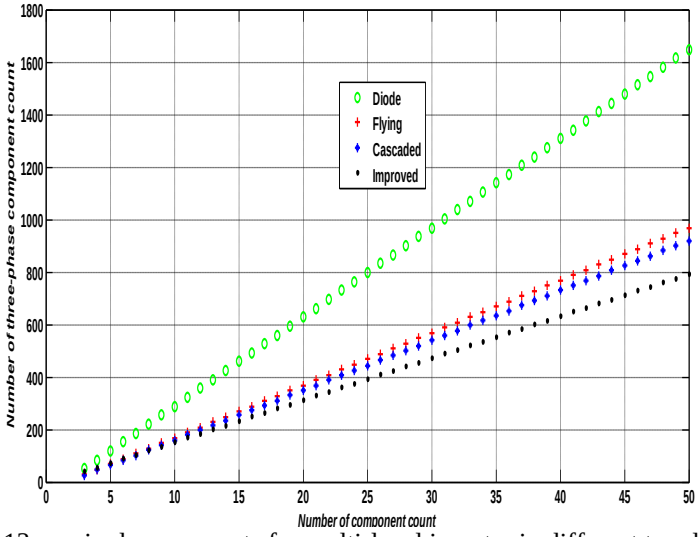

Fig. 13 required components for multi-level inverter in different topology.

V. CONCLUSION

The Diode clamped and Improved multilevel inverter topologies were simulated in MATLAB simulation platform and their output performances were obtained. The circuit performance was tested by three-phase asynchronous motor load. It was observed that their outputs displayed similar performance. In the required circuit components count, it is also observed that the Improved inverter topology shows significantly reduced number of component count, when compared with other inverter topologies. As a result of this the cost, weight and size of the improved inverter power circuit has to be reduced.

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APPENDIX

FIG.8 LOGIC FIRING SIGNALS

```
function [ga1,ga2,gb1,gb2,gc1,gc2]=
fcn(SIN,SIN1,SIN2,T1,T2)
if (SIN >T1)
   ga1=1;
else
   ga1=0;
end
if (SIN >T2)
   ga2=1;
else
   ga2=0;
end

%Phase b programme
%SIN1=(SIN-2*pi/3);
if (SIN1 >T1)
   gb1=1;
```

```
else
   gb1=0;
end
if (SIN1 >T2)
   gb2=1;
else
   gb2=0;
end

% phase c programme
%SIN2=(SIN-4*pi/3);
if (SIN2 >T1)
   gc1=1;
else
   gc1=0;
end
if (SIN2 >T2)
   gc2=1;
else
   gc2=0;
end
```

FIG.10a SIMULATION RESULT

```
x=Xout;
T=x(:,1);
figure(1)
subplot(3,3,1)
plot(T,x(:,2),'r')
xlabel('Time (secs)')
ylabel('Rotor Current Ir_a(A)')
title('Graph of Phase A Rotor Current')
grid on
subplot(3,3,2)
plot(T,x(:,5),'r')
xlabel('Time(secs)')
ylabel('Stator current Is_a(A)')
title('Graph of Phase A Stator current')
grid on
subplot(3,3,3)
plot(T,x(:,8),'k','linewidth',2.0)
xlabel('Time (secs)')
ylabel('Rotor Speed(rpm)')
title('Graph of Rotor Speed')
grid on
subplot(3,3,4)
plot(T,x(:,3),'b')
xlabel('Time (secs)')
ylabel('Rotor Current Ir_b(A)')
title('Graph of Phase B Rotor Current')
grid on
subplot(3,3,5)
plot(T,x(:,6),'b')
xlabel('Time (secs)')
ylabel('Stator Current Is_b(A)')
title('Graph of Phase B Stator Current')
grid on
subplot(3,3,6)
plot(T,x(:,9),'k','LineWidth',2.0')
xlabel('Time(secs)')
ylabel('Torque (N-m)')
title('Graph of Electromagnetic Torque(N.m)')
grid on
subplot(3,3,7)
plot(T,x(:,4),'m')
xlabel('Time (secs)')
ylabel('Rotor current Ir_c(A)')
title('Graph of Phase C Rotor current')
grid on
subplot(3,3,8)
plot(T,x(:,7),'m')
xlabel('Time(secs)')
ylabel('Stator Current Is_c(A)')
title('Graph of Phase C Stator Current(A)')
grid on
subplot(3,3,9)
plot(T,x(:,10),':r','linewidth',2)
xlabel('Time(secs)')
ylabel('Motor Input Voltages(V)')
title('Graph of Inverter Output Voltages')
grid on
hold on
plot(T,x(:,11),'-.b','linewidth',2)
hold on
plot(T,x(:,12),'m','linewidth',2)
Legend('Va','Vb','Vc')
figure(2)
plot(x(:,8),x(:,9),'r','linewidth',1)
xlabel('Rotor Speed (RPM)')
ylabel('Torque (Nm)')
title('Graph of Torque versus Rotor-Speed')
grid on
```