IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
Vol. 05, Issue 08 (August. 2015), ||V2|| PP 15-29

Design and Characteristics of a Two-level VSC with a Third-Harmonic Injection Bus-clamping SVM– *Detailed Study*

Hadi H. Alyami
Department of Electrical and Computer Engineering
Faculty of Graduate Studies and Research
University of Alberta, Canada

***Abstract*: -** At present, power electronics-based technologies are widely penetrating the power systems in an effort towards "smart-oriented" operational systems. Voltage-sourced converters (VSCs) are such power electronics-based technologies that currently seem rather to preponderate in many promising applications including FACTs, HVDC grids, DGs and VSDs. VSCs are found in a plethora of structures ranging from a simple half-bridge to an advanced modular topology and in order to exploit all their possible inherent features, a number of modulation strategies have been established. This paper investigates holistically the 3Φ two-level VSC with a 3rd harmonic injection bus-clamping space-vector modulation. It is essentially envisioned to further [7]-[8] studies, which compare two common VSC topologies, by including the abovementioned bus-clamping topology. The modulation strategy implemented through the principle of the equivalence linear triangle-comparison-based PWM with a bus-clamping SVM, mainly the MAX and MIN bus-clamping schemes. The resultant asynchronised SV-PWM has been investigated with a passive RL load and an active asynchronous vector-controlled motor with the aid of Simulink® simulated models.

***Index Words*: -** *Voltage Sourced Converter (VSC), SVPWM, Bus-clamping control strategy, THD%, Induction motor*

I. INTRODUCTION

The current global growth in energy demand drives power systems to the forefront where as a matter of support power electronics (PEs) systems are a vital key in those systems. At present, the development in power systems encompasses the entire systems from power generation along to utilisation, supporting the diffusion towards "smart-oriented" power systems. The "smart-oriented" concept in power systems can be described by Fig. (1), where power exchange among the different systems and sub-systems is unidirectional.

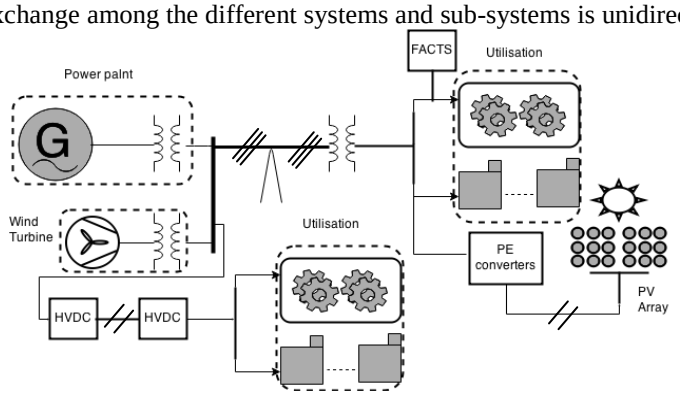


Figure (1) Simple smart-oriented power grid structure

Therefore, the drawbacks that are stemmed from the conventional power systems –which are
• Systems are sensitive to voltage and frequency instabilities because of dynamic network reconfigurations and load variations,
• Employment of demand-side control strategies that are useful for eliminating the risk of failures and blackouts, and hence increasing the overall efficiency, are not possible, and
• Integration of renewable energies and energy storage technologies seemingly require a complete makeover
– can be effectively mitigated as of Fig. (1) operation. However, new requirements [2] arise for
• Higher power handling capability to meet the growing demand in energy along with the diffusion towards electric-based transit,
• Higher power quality and reliability to support power security,
• Higher efficiency to minimize the power dissipation especially during power transmission,
• Higher flexibility to ensure highly configurable system that allows smooth integration of new subsystems, and

• Lower environmental impact through renewable energies penetration, which supports power sustainability.

These requirements have stimulated new power-related operational concepts such as FACTs, DGs and HVDC grids and also encouraged highly decentralised subsystems that are smart grids, active networks and micro-grids, wherein altogether VSC is a key operational part.

The 3Φ VSCs encapsulate the ability of PEs converters to exchange power among systems in such a way that the power is being inverted if the average power flows from a DC source to an AC source and is being rectified if vice versa. They can be classified on their power ratings into (i) two-level VSCs, (ii) multi-level VSCs or (iii) multi-module VSCs [2]. The two-level VSC is the viable option, due to its simplicity and reliability, if the voltage requirement is not principally higher than $7kW$, or else the multi-level VSCs, or even the multi-module VSCs, are the options for higher voltage applications. Although the multi-level VSCs seem infinite as more series-connected power switches are scintillatingly added, practical limitations brought forward such as poor form factor, simulating-gating requirements and unequal distribution of power switches conduction. Therefore, multi-module concept mitigates the high voltage requirements through deploying VSCs in modules, for example, the MMC structure that are incorporated in many High-voltage applications such as the meshed HVDC grids [12]. However, based in the literature, the two-level and three-level (NPC) VSCs are the common used topologies in power systems and industrial applications; though, they pose some disadvantages. For instance, the high power withstanding capability required for the two-level VSCs used in medium/high voltage applications and the natural point equalisation issues in the NCP VSCs [6]. These shortcomings; nevertheless, can be mitigated externally, through auxiliary circuitries, or internally, through advanced control strategies. The SV-PWM is the most widely adopted controlling strategy; owning to its ability in reducing harmonics and switching losses and maximising the DC-link voltage utilisation, compared to its counterpart SPWM [13].

In wide-ranging, this paper studies and simulates a three phase two-level VSC, inversion mode, with a bus-clamping SV-PWM strategy. This strategy is, also so-called discontinues DPWM, categorised into a number of modulation schemes where the DPWM-MAX and DPWM-MIN schemes are investigated in terms of their THD performance. Subsequently, they are compared to the study in [7], which compared the three phase two-level and NPC VSCs with the conventional SV-PWM. The modulation schemes are further validated in a typical vector-controlled asynchronous motor and the mechanical and electrical parameters waveforms are observed.

II. TWO-LEVEL VS. NCP

Fig. (2) illustrates a single phase "pole" of the two-level and three-level (NPC) VSCs, where two more identical poles are interconnected in parallel to form a three phase converter.

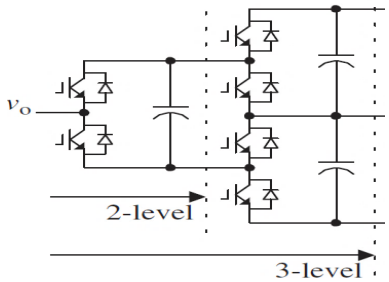


Figure (2) Single phase half-bridge block of 2-level and 3-level VSCs

Their level-denoted terms reflect the fact that the two-level only fluctuates between $\frac{V_{DC}}{2}$ and $\frac{-V_{DC}}{2}$, whereas the three-level fluctuates among $\frac{V_{DC}}{2}$, zero and $\frac{-V_{DC}}{2}$. Although the three-level waveform quality is almost 42% less-distorted, the required power switches are doubled [2]. On contrary, the voltage stress on the power switches are doubled in the two-level and it exacerbates with high voltage operation. Despite NPC VSC still suffers from unequal ON-state distribution. It can be concluded that the output voltage waveforms of either configuration are independent of the load current and its direction, but are dependent of the DC-link voltage, which is valved by the power switches conduction pattern. The SV-PWM is the common power switches control strategy that provides15.5% higher of the DC-link voltage utilisation than SPWM provides [5].

III. PRINCIPLE OF SV-PWM AND CARRIER-BASED MODULATIONS

It is known that the three phase two-level VSC can act in a unidirectional way – inversion and rectification modes – where the inversion mode is the concern in this paper. Therefore, the average power flow is DC/AC. The three phase two-level VSC acts in an inversion-wise is depicted in Fig. (3) and is normally referred to as 3Φ voltage source inverter (VSI). This topology is widely used in grid-connected and industrial applications such as HVDC systems and variable speed drives. As such, it is required to invert the fixed DC

source into a three phase variable magnitude and frequency source. The circuit itself is totally not applicable to achieve this operational behaviuor without the aid of a controlling strategy.

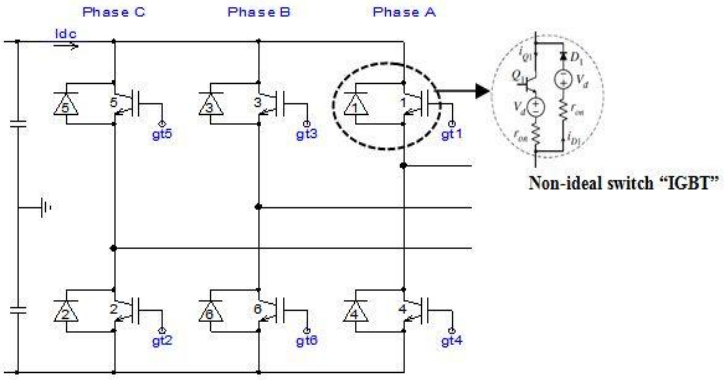


Figure (3) Simple structure diagram of the three phase two-level VSC

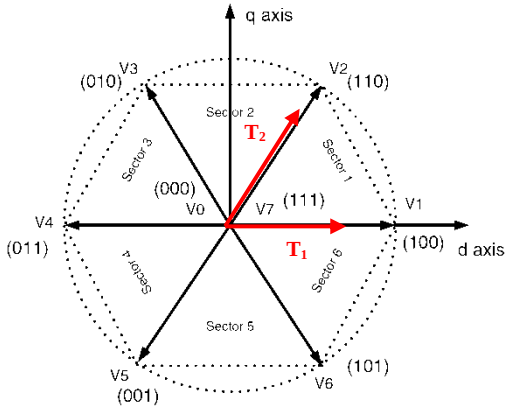


Figure (4) Space vector diagram of the three phase two-level VSC

Commutation among the switches states, which are normally diode crossed IGBTs, is complementary; therefore, eight switching states are possible [2].The switching states can be obtained by a number of modulation strategies, where carrier-based PWM and SVPWM are the dominant. The latter dispenses better performance in terms of the DC-link utilisation and the quality of the synthesised output voltage waveform. A case of point is 15% more of the DC-link voltage and 33% less of communication per switching cycle and thus less switching losses and better harmonic performance.

The switching states from SV-PWM stand view is shown in Fig. (4) and tabulated in table (1).

Table (1) Switching states and line voltages of the three phase two-level VSC

	Space Vector	Switching States	On-state Switch	Line Voltage		
				V_{ab}	V_{bc}	V_{ca}
Zero Vectors	$\vec{V}0$	000	Q1, Q3, Q5	0	0	0
	$\vec{V}7$	111	Q4, Q6, Q2	0	0	0
Active Vectors	$\vec{V}1$	100	Q1, Q6, Q2	$V_{DC}/2$	0	$-V_{DC}/2$
	$\vec{V}2$	110	Q1, Q3, Q2	0	$V_{DC}/2$	$-V_{DC}/2$
	$\vec{V}3$	010	Q4, Q3, Q2	$-V_{DC}/2$	$V_{DC}/2$	0
	$\vec{V}4$	011	Q4, Q3, Q5	$-V_{DC}/2$	0	$V_{DC}/2$
	$\vec{V}5$	001	Q4, Q6, Q5	0	$-V_{DC}/2$	$V_{DC}/2$
	$\vec{V}6$	101	Q1, Q6, Q5	$V_{DC}/2$	$-V_{DC}/2$	0

The angle between any two adjacent space vectors is 60°, where the envelope of the hexagon created by the active vectors is the locus of the maximum output voltage. Principally, when employing space vector, the three rotating time-varying quantities are sinusoidal having same amplitude and frequency with 120° phase-shift. As such, the space vectors shown in table (1) can be mapped into the dq-frame through applying Eq. (1)-(2).

$$V_d(t) = m_d(t)\frac{V_{DC}}{2} \quad [1]$$

$$V_q(t) = m_q(t)\frac{V_{DC}}{2}, \quad [2]$$

where$m$ is defined in [3] as $m_a = \frac{\sqrt{3}\,V_{ref}}{V_{DC}}$, and voltage reference, which is sampled once in every sub-cycle, as $\vec{V}_{ref} = \vec{V}_{ref}\, e^{j\theta}$. Thus, as $\vec{V}_{ref}$ revolves among the sectors shown in Fig. (5) different switching states for certain durations are achieved in such a way that, for sector *1*, $\vec{V}0$, $\vec{V}1$, $\vec{V}2$ and $\vec{V}7$ can be used. Dwell time for the corresponding active vectors can be given by for linear modulation range

$$\left.\begin{aligned} T_1 &= \frac{\sqrt{3}\,T_s\,V_{ref}}{V_{DC}}\,Sin\left(\frac{\pi}{3}-\theta\right) \\ T_2 &= \frac{\sqrt{3}\,T_s\,V_{ref}}{V_{DC}}\,Sin\,(\theta) \\ T_0 &= T_s - T_a - T_b \end{aligned}\right\} \text{For } 0 \le \theta \le \frac{\pi}{3} \quad [3]$$

These expressions can also be written as follows in terms of modulation index (m_a)

$$\left.\begin{aligned} T_1 &= T_s m_a\,Sin\left(\frac{\pi}{3}-\theta\right) \\ T_2 &= T_s m_a\,Sin\,(\theta) \\ T_0 &= T_s - T_a - T_b \text{ for } \vec{V}0 \text{ and } \vec{V} \end{aligned}\right. \quad [4]$$

where T_s is the sampling time. The division of the duration T_0 between $\vec{V}0$ and $\vec{V}7$ is a degree of freedom in SV-PWM; as such, this division in $T_s/2$ is equivalent to inserting a common-mode component to the 3Φaverage branch voltage [7]. This is moreover corresponding to the triple-n frequency addition to the fundamental sinusoidal waveforms in carrier-based PWM over a fundamental cycle. Therefore, this theoretical equivalence between the two modulation strategies is assessed to implement SV-PWM with 3rd harmonic injection based on the carrier-based PWM theory during which V_{ref} is attainable as three phase sinusoidal modulating waveforms or as a voltage vectors.

IV. CARRIER-BASED SVPWM

In a carrier-based PWM, three phase sinusoidal modulating waveforms, that are,

$$\left.\begin{aligned} V_{Am} &= V_m\cos(\omega t) \\ V_{Bm} &= V_m\cos\left(\omega t - 2\frac{\pi}{3}\right) \\ V_{Cm} &= V_m\cos\left(\omega t - 4\frac{\pi}{3}\right) \end{aligned}\right. \quad [5]$$

are employed for the modulating signal, V_m, and compared with a high frequency triangular waveform, ω. Inserting a common-mode component m_{cm} to Eq. (5) yields

$$\left.\begin{aligned} V^*_{Am} &= V_m\cos(\omega t) + m_{cm} \\ V^*_{Bm} &= V_m\cos\left(\omega t - 2\frac{\pi}{3}\right) + m_{cm} \\ V^*_{Cm} &= V_m\cos\left(\omega t - 4\frac{\pi}{3}\right) + m_{cm} \end{aligned}\right. \quad [6]$$

m_{cm} can be any odd triple-n frequency and is normally a third harmonic component 3ω.The resultant modulation strategy is a carrier-based SV-PWM and is depicted in Fig. (5) [2]-[3].

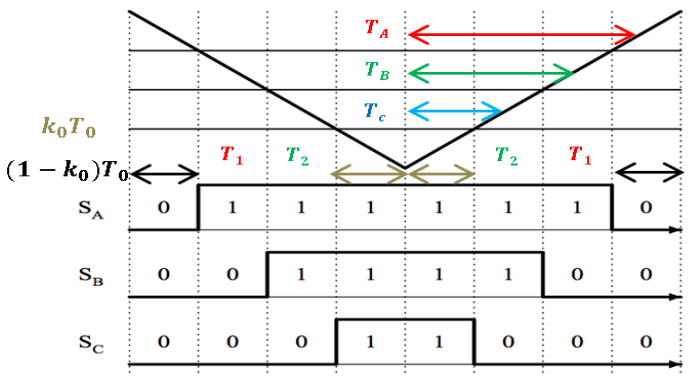


Figure (5) Space-vector modulation through triangle-comparison-based method for the continuous SVM (7 segments)

It is clear that the zero vectors $\vec{V}0$ and $\vec{V}7$ are distributed equally each sub-cycle, ${}^{T_s}/_{2}$; as such, if $\vec{V}7$ is assumed to be k_0T_0, $\vec{V}0$ would be $(1-k_0)T_0$. Mapping Eq. (4) into their signals in Fig. (5) gives

$$\begin{aligned} T_A &= k_0T_0 + T_2 + T_1 \\ T_B &= k_0T_0 + T_2 \\ T_C &= k_0T_0, \end{aligned} \quad [7]$$

which correspond to the dwell times for sector *1*. Based on the *Equal Voltage-Second* theory, time intervals T_1 and T_2 correlate to $V_{ab}^* = V_a^* - V_b^*$ and $V_{bc}^* = V_b^* - V_c^*$ applied over a complete cycle, T_s.

$$\begin{aligned} T_1V_{DC} &= V_{ab}^*\ T_s \\ T_2V_{DC} &= V_{bc}^*\ T_s \\ T_0 &= T_s - T_1 - T_2, \end{aligned} \quad [8]$$

where the generic voltage reference vector can be expressed by

$$\vec{V}^* = \frac{2}{3}\left(V_a^* + \vec{\theta}V_b^* + \vec{\theta}^2V_c^*\right). \quad [9]$$

V_a^*, V_b^* and V_c^* need to be set in order to define $\vec{V}^*$ sector; therefore, implementing SV-PWM out of carrier-based triangle-comparison. The triangle waveform, shown in Fig. (5), can be defined as

$$\frac{V_t}{V_{tp}} = \left(\frac{2}{T_s}t - 1\right) \text{ where } 0 \le t \le T_s, \quad [10]$$

whereV_t and V_{tp} are the instantaneous and peak magnitudes of the triangle waveform respectively. Substituting for T_A, T_B and T_C in Eq. (8) into t in Eq. (10), and normalising all voltages to the base voltage, $V_{base} = V_{tp} = \frac{V_{DC}}{2}$, the corresponding normalised reference voltages (or modulation functions), that are $V_{a,b,c}^{**} = \frac{V_{a,b,c}^{**}}{(0.5\,V_{DC})}$, can be obtained [7].

$$V_{a,b,c}^{**} = V_{a,b,c}^{**} + v_{zs}^*, \quad [11]$$

where $V_{a,b,c}^{**} \in V_a^*$, V_b^* and $V_c^*$and v_{zs}^* is the reference zero sequence voltage and is given by

$$v_{zs}^* = -[(1-2k_0) + k_0v_a^* + (1-k_0)v_c^* \quad [12]$$

New set of normalised reference voltages, $v_{a,b,c}^{**}$, is obtained,which can be incorporated as inputs modulating functions. Additionally, it is noticeable that v_{zs}^* comprises DC component, $1-2k_0$; thus, for a balanced system that is $v_a^* + v_b^* + v_c^* = 0$, with a conventional SV-PWM, v_{zs}^* would be as follows

$$v_{zs}^* = -0.5(v_a^* + v_c^*) = 0.5v_b^* \quad [13]$$

Eq. (9)-(13) consider sector *1*; nevertheless, similar procedure conducts for all sectors. To simplify the algorithm by eliminating the need for the explicit sector identification, v_{max}^*, v_{mid}^* and v_{min}^* are set to designate the level values of $v_{a,b,c}^{**}$. Eq. (12) consequently becomes

$$v_{zs}^* = -[(1-2k_0) + k_0v_{max}^* + (1-k_0)v_{min}^*, \quad [14]$$

when $0 \le k_0 \le 1$, and Eq. (5) becomes

$$v_{zs}^* = -0.5(v_{max}^* + v_{min}^*) = 0.5v_{mid}^*, \quad [15]$$

when $k_0 = 0$. These expressions can be schematically represented with the aid of Simulink® as

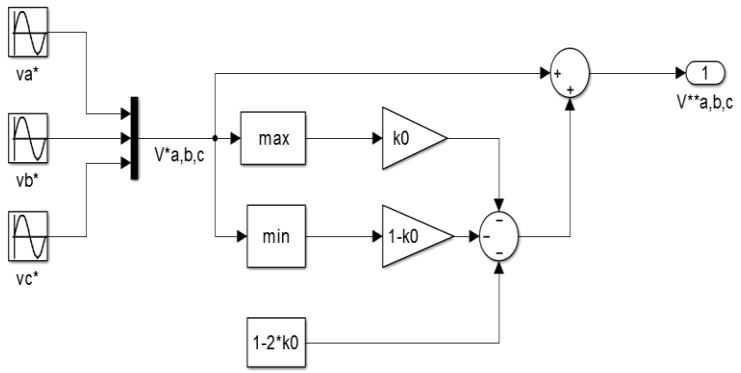


Figure (6) Block diagram of Eq. (9) and (10)

The resultant 3Φ reference voltages are shown in Fig. (7).

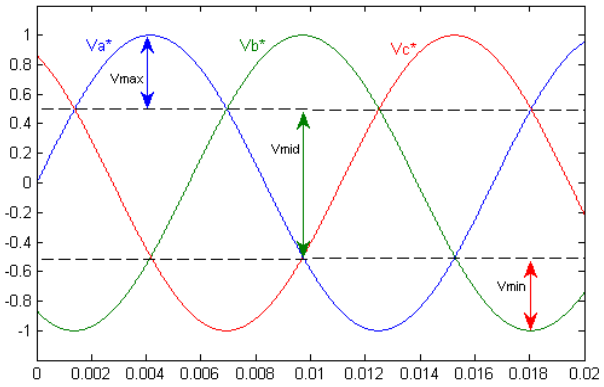


Figure (7) Three phase reference signals

It is then apparent that based on the value of k_0, three possible schemes of SV-PWM can be obtained from the model in Fig. (6), and they are:

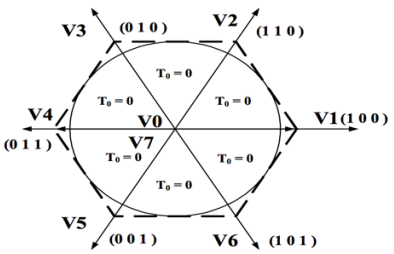
- SV-PWM when $k_0 = 0.5$
- DPWM-MAX when $k_0 = 1$
- DPWM-MIN when $k_0 = 0$

V. DISCONTINIUOS PWM (DPWM)

The bus-clamping SV-PWM (DPWM) is a popular SV modulation strategy that can dispense better harmonic performance than the conventional SV-PWM. The fact that during one complete T_s, either $\vec{V}0$ or $\vec{V}7$ is entirely clamped to the positive or negative bus DC-link explains the bus-clamping terminology. Thus, one pole of the inverter remains unmodulated during one switching interval. When zero voltage [OOO] is eliminated, the pole voltage is tied to the positive rail and when zero voltage [PPP] is eliminated, the pole voltage is tied to the negative rail. The number of switching states is accordingly condensed to *two-third* compared with the continuous SV-PWM and hence switching losses are eliminated significantly. For this reason, this strategy is also called minimum-loss SVM and based on the switching sequence switching losses can be reduced to 50% compared with the continuous SV-PWM. This fact qualifies DPWM to a higher power handling capacity without the need for cooling system. There are plethora schemes of DPWM in the literature, which only differ in their switching sequence patterns, namely the distribution of the zero space vectors and the duration of their clamping-state [3]. The common schemes are

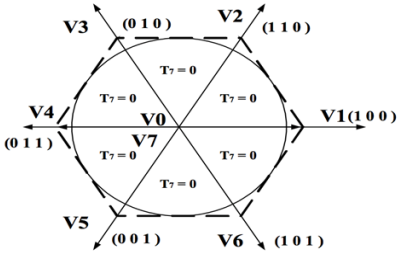
- DPWM-MAX: this scheme is achieved when zero voltage [OOO] is eliminated ($T_0 = 0$).
- DPWM-MIN: this scheme is achieved when zero voltage [PPP] is eliminated ($T_7 = 0$).

The corresponding hexagon planes for the forgoing schemes are depicted in Fig. (8).



DPWM-MIN

Sectors	Switching sequence pattern with dwell times for DPWM-MIN				
	$T_0/2$	$T_1/2$	T_2	$T_1/2$	$T_0/2$
1	$\vec{V}0$	$\vec{V}1$	$\vec{V}2$	$\vec{V}1$	$\vec{V}0$
2	$\vec{V}0$	$\vec{V}3$	$\vec{V}2$	$\vec{V}3$	$\vec{V}0$
3	$\vec{V}0$	$\vec{V}3$	$\vec{V}4$	$\vec{V}3$	$\vec{V}0$
4	$\vec{V}0$	$\vec{V}5$	$\vec{V}4$	$\vec{V}5$	$\vec{V}0$
5	$\vec{V}0$	$\vec{V}5$	$\vec{V}6$	$\vec{V}5$	$\vec{V}0$
6	$\vec{V}0$	$\vec{V}1$	$\vec{V}6$	$\vec{V}1$	$\vec{V}0$



DPWM-MAX

Sectors	Switching sequence pattern with dwell times for DPWM-MAX				
	$T_0/2$	$T_1/2$	T_2	$T_1/2$	$T_0/2$
1	$\vec{V}7$	$\vec{V}2$	$\vec{V}1$	$\vec{V}2$	$\vec{V}7$
2	$\vec{V}7$	$\vec{V}2$	$\vec{V}3$	$\vec{V}2$	$\vec{V}7$
3	$\vec{V}7$	$\vec{V}4$	$\vec{V}3$	$\vec{V}4$	$\vec{V}7$
4	$\vec{V}7$	$\vec{V}4$	$\vec{V}5$	$\vec{V}4$	$\vec{V}7$
5	$\vec{V}7$	$\vec{V}6$	$\vec{V}5$	$\vec{V}6$	$\vec{V}7$
6	$\vec{V}7$	$\vec{V}6$	$\vec{V}1$	$\vec{V}6$	$\vec{V}7$

Figure (8) Space vector diagrams and their corresponding mapping tables of the three phase two-level VSC [Five-segment pattern]

The space vector voltages shown in Fig. (9) can be mapped into different switching sequence patterns, where Type-I and Type-II patterns are considered. These types of switching sequence patterns are based on the five-segment sequenced patterns, where the zero vector voltage is split equally each sub-cycle [6]. The complete switching sequences for all sectors for both types are tabulated in Fig. (8). Although the switching patterns are different, they can be achieved from either sequence with only changing the value of k_0. This accomplishes higher freedom of the controlling strategy.
Sector *1* of the hexagon plane for both types can be mapped as shown in Fig. (9).

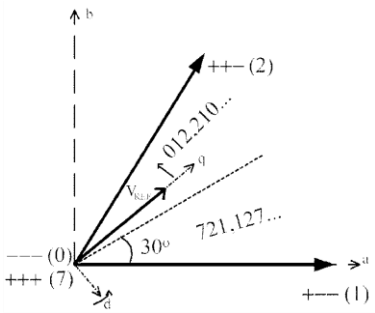


Figure (9) Bus-clamping PWM techniques for MIN and MAX schemes in Fig. (9)

The switching sequences patterns on the tables of Fig. (8)assure the limitation of the switching frequency that is $f_{sw} = 4\,N f_s$ [7]. However, the output voltage waveform lacks the antisymmetry of the voltage curve; as such, even harmonic ($2kf_s$) appears (asynchronised PWM).
The three phase average pole voltages are determined by the DC-link voltage magnitude and the dwell time durations and are expressed as

$$V_{A,ave} = V_{DC}\frac{2}{T_S}(T_1 + T_2 - T_0) \quad \textbf{[16]}$$
$$V_{B,ave} = V_{DC}\frac{2}{T_S}(-T_1 + T_2 - T_0)$$
$$V_{C,ave} = V_{DC}\frac{2}{T_S}(-T_1 - T_2 - T_0)$$

It should be noted that the negative and positive DC-link voltages are assumed $\mp V_{DC}$. On the other hand, since $T_1 + T_2 - T_0 = {}^{T_S}/_{2}$, Eq. (8) becomes

$$V_{A,ave} = 2\,V_{DC}\left(\frac{2}{T_S}\,T_1 + \frac{2}{T_S}T_2 - T_0\right) \quad \textbf{[17]}$$
$$V_{B,ave} = 2\,V_{DC}\left(\frac{2}{T_S}\,T_2 - \frac{2}{T_S}\right)$$
$$V_{C,ave} = -V_{DC}$$

Similar procedure can be followed to express the average pole voltages for the other sectors.

Now, the equivalent principle of implementing DPWM through the carrier-based triangle-comparison for both switching sequence types can be accomplished. The schematic block diagram shown in Fig. (10) illustrates the proposed control strategy of the equivalent principle with a zero-sequence injection (3rd harmonic).

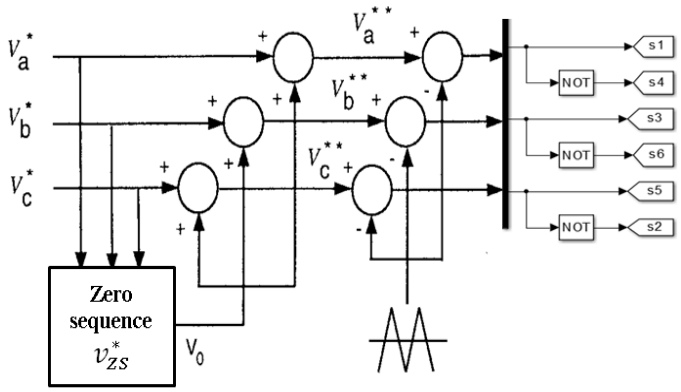


Figure (10) SV-PWM triangle-based block diagram

VI. SWITCHING PATTERNS EVALUATION OF DPWM-MAX AND DPWM-MIN

The switching patterns shown in the tables in Fig. (8) can be generated by the schematic diagram in Fig. (10). They are six gating signals corresponding to the six power switches in Fig. (3). The signals are generated with a complementary-manner commutation so that two signals with opposite gating assign for each valve.

The simulated switching sequence waveforms forming the gating signals are shown in Fig. (11)-(12) for DPWM-MIN and DPWM-MAX for their zero space vectors respectively. The behaviour of the bus-clamping is obvious, that is, in DPWM-MIN each signal suppresses a continuous period of $\frac{2\pi}{3}$ each per-cycleof the fundamental frequency clamping to zero, while similar manner for DPWM-MAX but clamping to 1. This bus-clamping behaviour means $1/3$ less switching losses compared with the conventional SV-PWM. Thus, this modulation strategy is optimal for applications require high switching frequency. Table (2) compares the abovementioned bus-clamping schemes with the conventional SV-PWM.

Table (2) The three phase two-level VSC with SV-PWM and DPWM comparison

Switching Pattern	Conventional SVPWM (7-segemnt)	DPWM-MIN and DPWM-MAX
Commutation in T_s	6	2
Switching losses%	100	33
THD%	55	70

Table (2) assures that if the switching losses for a 3Φtwo-level VSC with SV-PWM assumed to be 100%, incorporating DPWM for the same VSC would reduce the switching losses to 33%. However, the switching losses reduction becomes at the cost of a higher THD%.

VII. PERFORMANCE EVALUATION OF DPWM-MAX AND DPWM-MIN

Ref [2]-[7] conducted a holistic comparison between the three phase two-level and NPC VSCs and both with the conventional SV-PWM. Despite the increasing complexity and cost, the comparisons showed a slant towards NPC VSCs because of their higher efficiency and power handling capacity and lower switching losses. This paper, however, endeavors to further the comparisons in [2]-[7] by including the three phase two-level with DPWM switching patterns shown in Fig. (8).

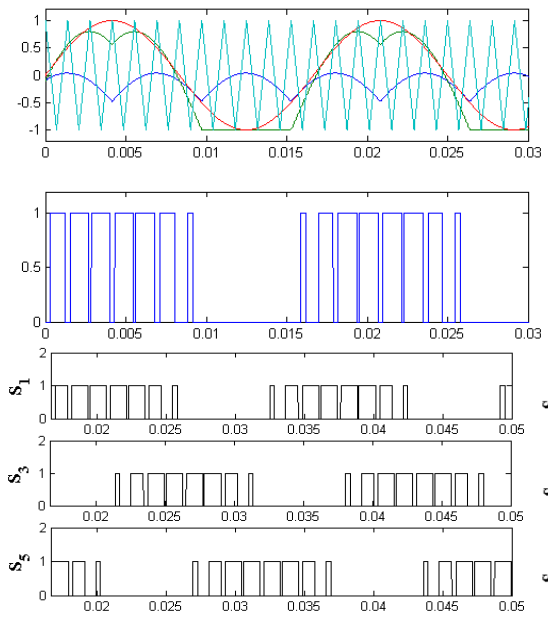


Figure (11) Simulated modulating and gating signals for DPWM-MIN

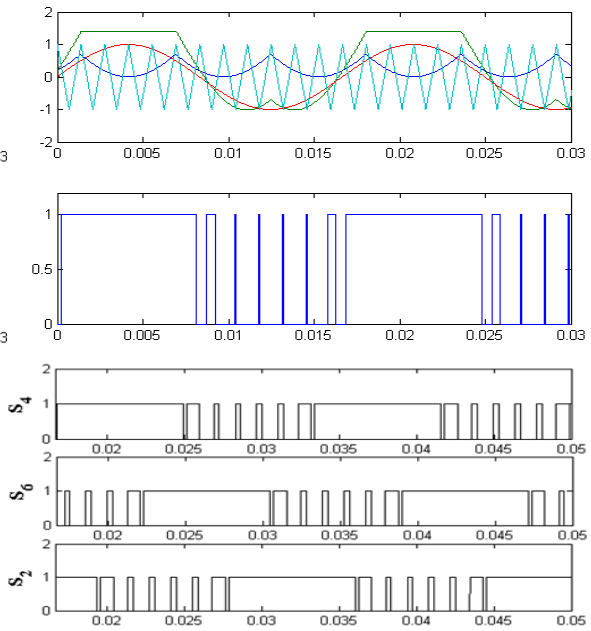


Figure (12) Simulated modulating and gating signals for DPWM-MAX

The VSC under study has similar specifications used in Ref [7] that are summerised in table (3).They confirm that the modelled VSC operates at the inversion mode and is feeding a passive RL load; as such, the rated DC input voltage, V_{DC}, and the RL values need to be determined (Appendix).

Table (3) System specifications for the studied VSC

Inverter Topology	**Two-level VSC (Inversion-mode) shown in Fig (1)**
Rated Inverter Output Power	1MVA
Rated Inverter Output Voltage	4160V (fundamental line-to-line voltage, rms)
Rated Inverter Output Current	138.8A (fundamental, rms)
Rated DC Input Voltage	Constant DC to be calculated
Load	At 60 HZ,the RL load has the impedance of $1.0p.u$ with a lagging displacement power factor of 0.9.
Switching Devices	Ideal IGBTs (no power losses or forward voltage drops)

The simulated waveforms showing the nature of DPWM-MIN and DPWM-MAX for a VSI feeding an RL load are depicted hereinafter. Simulation accounts for V_{AB} and i_A waveforms behaviour and quality under different operation conditions, which are:

- V_{AB}andi_A waveforms are repeated with fundamental frequencies being changed between $60Hz$ and $30Hz$ and modulation indices between0.8 and 0.5.
- Sampling time is consistently being $1/720$.
- Ideal switch operation assumed, whereby no conduction or switching losses are considered and dead-time is not counted in.

The switching frequency is recommended to be 90% higher than the fundamental frequency to assure a linear process of PWM so that during one complete cycle,T_s, the modulating signal can be considered constant.Consequently, $f_{sw}$for $s_1$in Fig. (10) is $570Hz$, which is also the carrier frequency in this case. However, increasing f_{sw} also contributes in an asyncronised PWM due to $m_f = {f_1}/{f_{sw}} \geq 21$.

The simulation results illustrate the modulation index and fundamental frequency effects on the output line voltage,V_{AB}, and on the output phase "A" line current i_A . The effects led to the conclusion that for a consistent fundamental frequency, harmonic contents are inversely proportional to the modulation index are also directly proportional to the fundamental frequency. The harmonic performances for all simulated waveforms are summarised in table (4). In essence, harmonic contents reduced when modulation indices increased from 0.5to 0.8. Nevertheless, harmonic contents increased at one modulation index but fundamental frequency gave rise from $30Hz$to $60Hz$.

Table (4) Simulation results for THD% performance for DPWM schemes

		DPWM-MIN		**DPWM-MAX**	
$f_1 Hz$	m	THD% V_{AB}	THD% i_A	THD% V_{AB}	THD% i_A
60	0.5	125.65	18.84	124.83	17.85
60	0.8	78.41	11.05	81.34	11.17
30	0.5	124.67	17.32	124.50	16.34
30	0.8	77.24	9.82	81.11	10.70

Table (4) assures that during $30Hz$ operation, the dominant harmonics appear as sidebands with higher harmonic roders, which can be filtered out. Nonethless, the dominant harmonic orders appear with lower harmonic orders during $60Hz$ operation. Additionally, sub-harmonics appear significantly at $60Hz$.

Observably, harmonic spectra for all conditions showed that large amount of harmonics were odd-ordered. Additionally, as indicated earlier, the line voltage produced by the conventional SV-PWM inverter contains even-order harmonics. However, in the inverter-fed medium-voltage drives, these harmonics may not have a significant impact on the operation of the motor in a case of point. The spectra also reflected that simulated waveforms were not half-wave symmetrical;

$$f(\omega t) \neq -f(\omega t + \pi).$$

Accordingly, even-order harmonic also appeared. It can also be noted that in all cases the carrier-to-fundamental ratio has increased, to at least partially reflect the increase in the switching frequency. In addition, the roll-off in magnitude of the sideband harmonic components was somewhat slow.

At this instant, it should be clear that discontinuous switching patterns lead to a suboptimal harmonic performance compared tothe continuous modulation arrangements in terms of the number and magnitude of carrier sidebands that are generated. Nonetheless, the advantage of these modulation strategies arises from the reduction in the number of the switch transitions per phase "leg" that can be achieved over each fundamental cycle. This reduction makes it possible to increase the carrier frequency for each variation by approximately 3/2 compared with the continuously switched regular or naturally sampled PWM, while still maintaining the same number of device switch transitions for each phase "leg" over a fundamental cycle. Lastly, it is abovious that the

selection of zero space vectors had minimal effects in the waverforms quaility as shwon in table (4). Thus, it is not necessery to spread the simulation bridth over all types; as such, only DPWM-MIN furtherexamined.

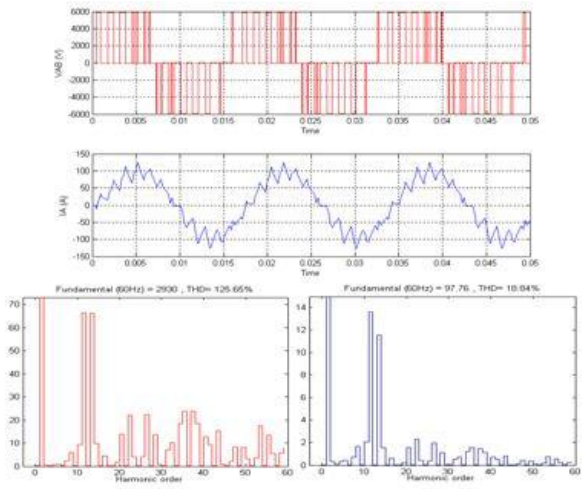


Figure (13) Simulated waverforms and THD% for DPWM-MIN (60 Hz, 0.5)

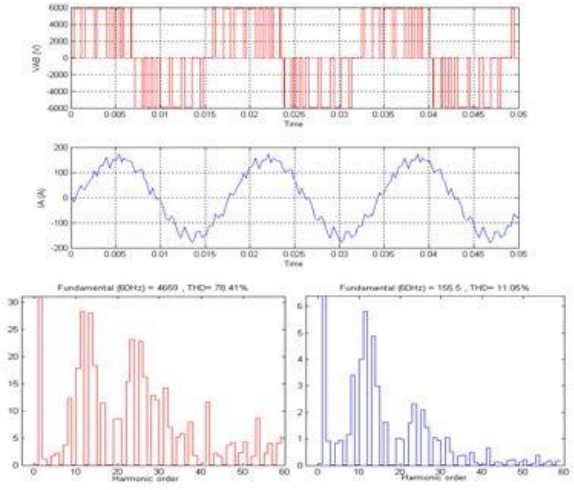


Figure (14) Simulated waverforms and THD%for DPWM-MIN (60 Hz, 0.8)

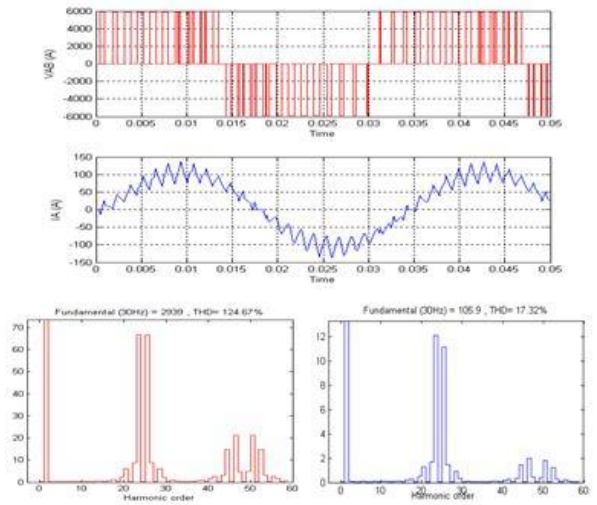


Figure (15) Simulated waverforms and THD% for DPWM-MIN (30 Hz, 0.5)

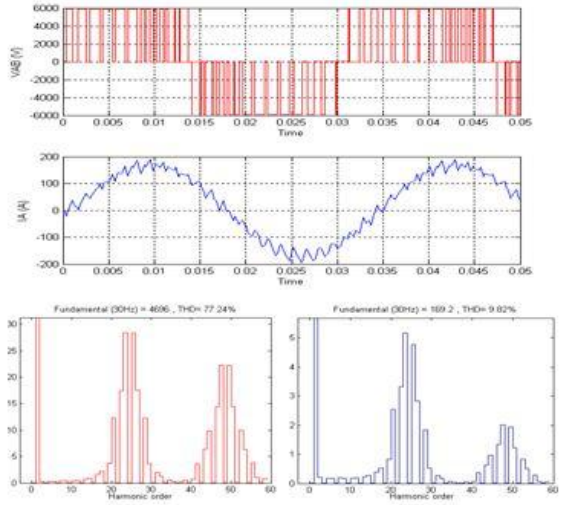


Figure (16) Simulated waverforms and THD%for DPWM-MIN (30 Hz, 0.8)

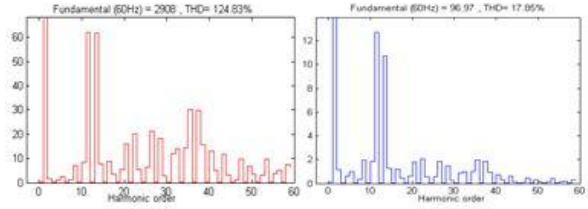


Figure (17) THD% perforamnce for DPWM-MAX (60 Hz, 0.5)

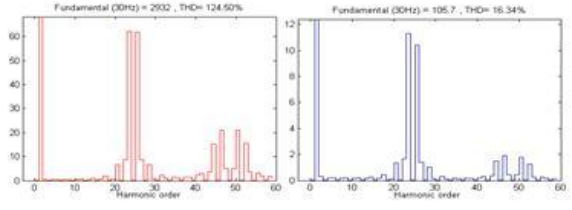


Figure (18) THD% perforamnce for DPWM-MAX (60 Hz, 0.8)

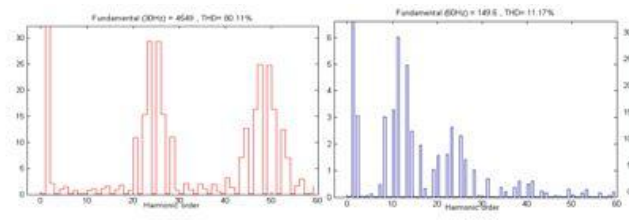


Figure (19) THD% perforamnce for DPWM-MAX (60 Hz, 0.5)

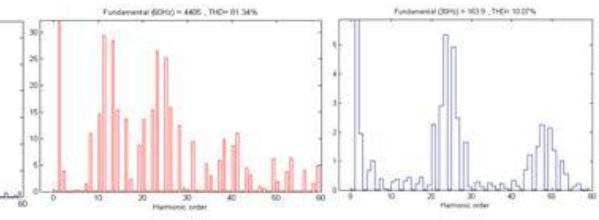
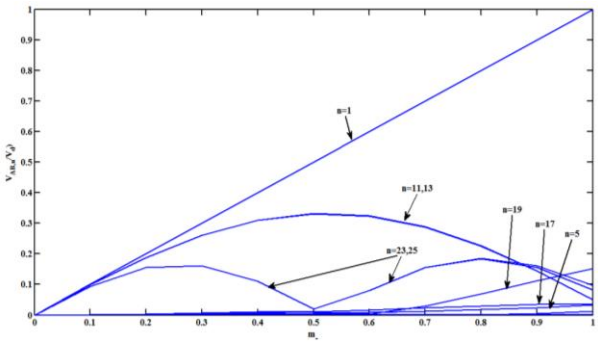


Figure (20) THD% perforamnce for DPWM-MAX (60 Hz, 0.8)

Fig. (13)-(20) exhibit thoroughly the corelation between the variation in the THD% of V_{AB} with incremental modulation indices from zero to 1 for DPWM-MIN. The unsymmetrical nature of the waveforms explain the odd- and even-order harmoincs presence. The absance of the 3rd harmonics is abvious in the plots since it was cancelled following the theroy of the 3rd harmonics injection PWM.



(21) Harmonics content of V_{AB} with 60 Hz and 720 Hz (odd order harmonics)

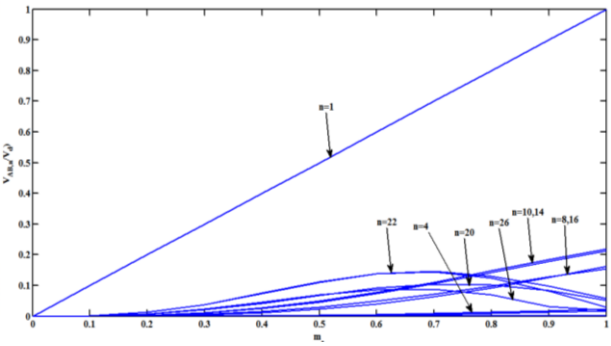


Figure (22) Harmonics content of V_{AB} with 60 Hz and 720 Hz (even order harmonics)

Fig. (21)-(22) illustrate the simulated waveforms of the 3Φ output voltages and current during a dynamic response for a unit step modulation index. The modulation index reference gave risefrom high to low refrenecs (0.8 to 0.5) for the unit step operation in $0.019s$ for different fundemantal frequecies ($60Hz$ and $30Hz$). The output voltage and current waveformsdemonstrate smooth transition during the dynamic response operation.

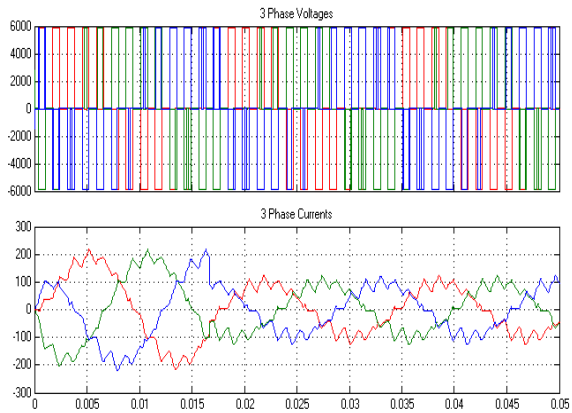


Figure (23) Modulation index unit step from 0.8 to 0.5 voltages and currents dyanmic response with 30 Hz and 570 Hz

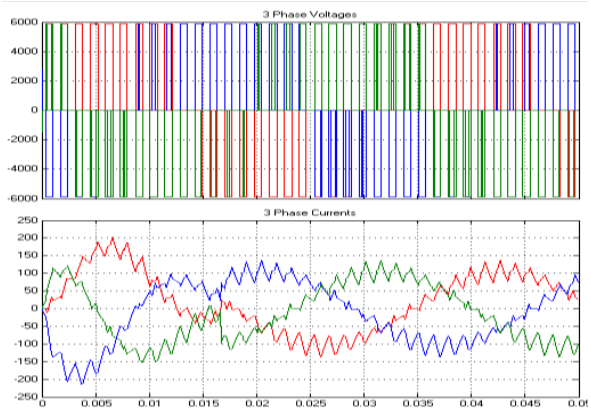


Figure (24) Modulation index unit step from 0.8 to 0.5 voltages and currents dyanmic response with 60 Hz and 570 Hz

Taking the advantage of the DPWM, the switching frequency can be increased to $1920\,Hz$. The simulated dynamic response waveform quality shown in Fig. (24)isthen enhnaced as shwon in Fig. (25).

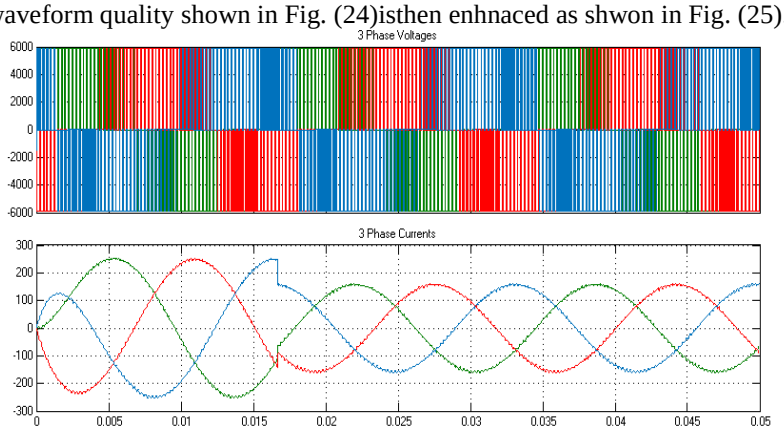


Figure (25) Modulation index unit step from 0.8 to 0.5 voltages and currents dyanmic response with 60 Hz and 1920 Hz

Increasing the switching frequency resulted in an improvement in i_A THD% from around 15% when $f_{sw} = 9\ f_1$ to 1.9% when $f_{sw} = 32\ f_1$. The THD of i_A can be given by

$$i_{A,THD} = \frac{\sqrt{i_{rms}^2 - i_1^2}}{i_1} \quad \textbf{[18]}$$

wherei_{rms} is the total rms current and i_1 is the fundamental rms current.

DPWM-MIN is additionally validated with an active load that is an asynchronous motor with indirect rotor-oriented flux vector control. It is, however, intended solely to show the above-detailed topology with an active load; as such, the modelling and controlling aspects of the overall system is not favoured. Ref [8] is the main reference in which the proposed system has been modified with a DPWM-MIN 3Φ two-level VSC. The simple schematic diagram of the system is depicted in Fig (26).

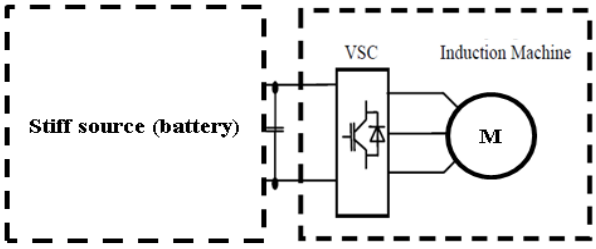


Figure (26) Simple VSD daigram (rectifier side assumed stiff "DC source")

It is the general practice in all vector-controlled algorithms to ensure that the current and flux vectors in the dealt-with machine are orthogonal at one complete fundamental cycle. In the indirect rotor-oriented flux vector control, the objective is to attain the rotor flux vectors (λ_{dqr}) perpendicular to the rotor current vectors (i_{dqr}). This is mainly accomplished by means of adjusting the position of the reference frame (the position of θ) in whichall rotor flux sits upon the d-axis: $\lambda_{qr} \xrightarrow{yields} 0$. The d-axis rotor voltage becomes

$$v_{dr} = 0 = R_r i_{dr} + \frac{d}{dt}[(L_m + L_{lr})i_{dr} + L_m i_{ds}] - \omega_{sl}\lambda_{qr} \quad \textbf{[19]}$$

where the variables can be explained by Fig. (27)

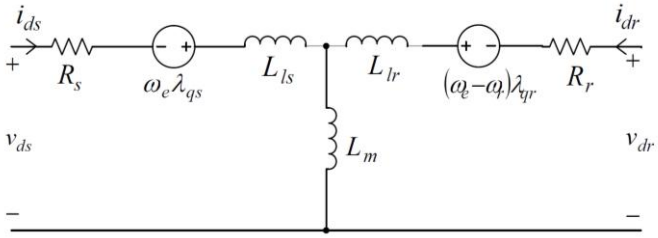


Figure (27) d-axis equivalent circuit of asynchronous motor

Therefore, as $\lambda_{qr} \xrightarrow{yields} 0$ and $\frac{d}{dt} i_{ds} \xrightarrow{yields} 0$, i_{dr} must roll-off to zero. However, their initial values are not zero following the controller activation creating start-up transients, which may accordingly require a feed-forward compensation $G_{ff}(s)$ [9]-[12]. The simulated curves for τ_m, i_{qs} and i_{ds} versus time are depicted in Fig. (28).

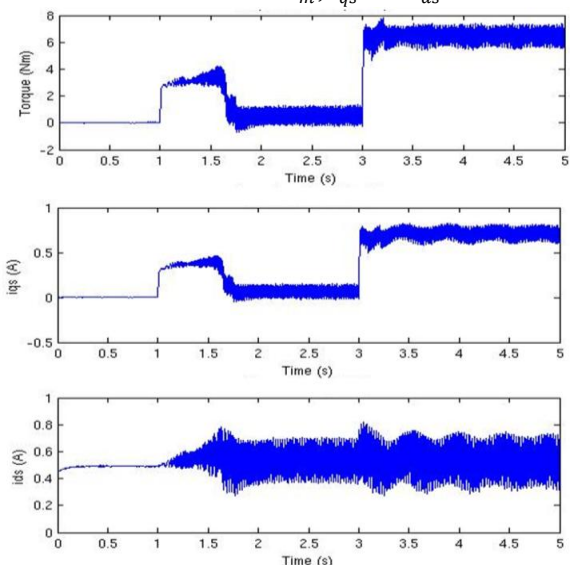


Figure (28) Simulated torque, dq-axes stator currents curves for VSD shown in Fi. (26) (12 kHz)

The curves shown in Fig. (30) illustrate the variable speed drive performance with DPWM-MIN orientation. The step changes of the load "torque" from 0 to 3 Nm at 1 sec, from 3 to 0Nmat 1.5 $sec$and finally from 0 to 6 Nmat 3 sec show the correlation among τ_m, i_{qs} and i_{ds} for the indirect rotor-oriented flux vector control variable speed drive.

The speed waveform is shown in Fig. (29) with a ramp-up time less than 1 sec, which concludes that the disturbance rejection is achieved through the fact that upon the load variation the speed held at its rated value $\approx 400\ rpm$.The inverter THD% performance is depicted in Figs (30).

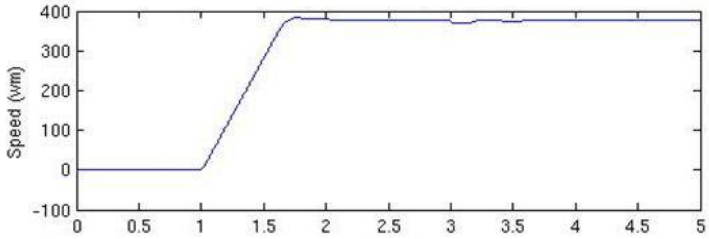


Figure (29) Speed curve showing no effects upon load "torque" varaition shown in Fig. (28)

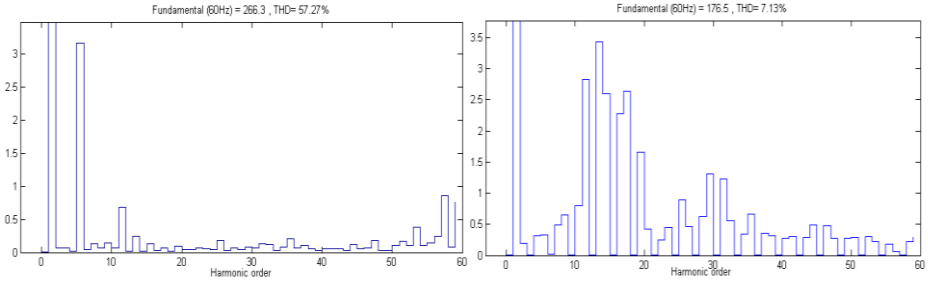


Figure (30) DPWM-MIN THD% performance for V_{AB}andi_A in VSD

Comparing the achieved performance with Ref [8] yields

Table (5) VSC THD% comparsion with VSD appliaction

VSC Topology	2L VSC (DPWM-MIN)	2L VSC (SV-PWM)	3L NPC (SV-PWM)
Switching frequency	$f_{sw} = 12\ kHz$		
Rated device voltage/current	1.2Kv / 50A IGBT		600V / 50A IGBT
THD% $\boldsymbol{V_{AB}}$	57.27	62.65	39.14
THD% $\boldsymbol{i_A}$	7.13	7.98	4.39

Table (5) ascertains how the converter topology along with its modulation strategy impacts the overall system's performance including the efficiency, THD% performance, operating ratings and torque ripples. Although DPWM topology would offer acceptable performance for the undergone induction motor, its torque ripples are criticising as shown in Fig (28). In order to improve the torque ripples of DPWM topology, the switching frequency needs to be increased. Consequently, the carrier bonds taking place at $n.f_{sw}$ shifts to higher frequencies of the THD% V prodviding a recovering damping of the THD% i. The switching frequency is therefore increased to 20 kHz and the simulated torque waveform is shown in Fig (31). The flux waveform is also depicted in Fig. (32) to apperciate that the controller precluds the rotor flux from violating the error tolarenace during dynamics.

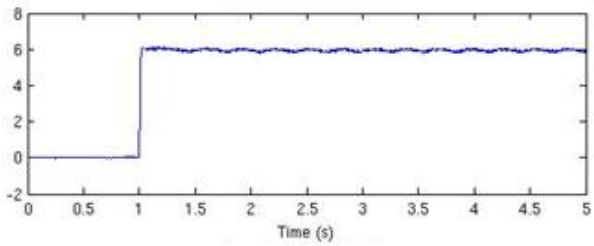


Figure (31) Torque curve with improved harmonics ripple 20 Khz

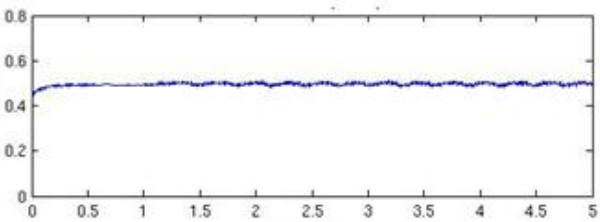


Figure (32) Rotor flux stability with load "torque" variation in Fig. (31)

VIII. CONCLUSION

The feasibility of the 120° DPWM has been investigated thoroughly in this survey with the focus being on the DPWM-MAX and DPWM-MIN schemes. The investigation was implemented with a passive RL load and an active asynchronous motor load, where in either loads it is evident that discontinuous switching patterns led to a suboptimal harmonic performance compared tothe continuous modulation arrangements in terms of the number and magnitude of carrier sidebands that are generated. However, it can be particularly noted from the simulated waveforms that the harmonic sideband cancellations (the cancellation of odd harmonics around the first carrier multiple) that is a feature of the continuous modulation strategies no longer occurs. Nevertheless, DPWM startegy is more applealing in applications that require high switching frequencies with correspondingly low switching loasses. In an overall term, the 3Φ two-level VSC with DPWM would fit in between the 3Φ two-level VSC with SV-PWM and the 3Φ three-level NCP with SV-PWM.

IX. ACKNOWLEDGMENT

Hadi Alyami is a king Abdullah foreign scholarship Program sponsored and gratefully acknowledges the financial support of the Ministry of Education in Saudi Arabia.

REFERENCES

[1] Abdul. R, Saikrishna. K, Apparao. D "Space vector-based three-level discontinuous pulse-width modulation algorithm" IET Power Electronics, April 2013.

[2] A. Yazdani, R. Iravani "Voltage-Sourced Converters in Power Systems: Modeling, Control, and Applications" IEEE/John-Wiley, ISBN: 978-0-470-52156-4, Feb. 2010.

[3] G. Narayanan, V. T. Ranganathan "Two Novel Synchronized Bus-Clamping PWM Strategies Based on Space Vector Approach for High Power Drives" IEEE Transactions on Power Electronics, Vol. 17, No. 1, July 2008.

[4] G. Narayanan, Harish K. Krishnamurthy, Di Zhao, RajapandianAyyanar "Advanced Bus-Clamping PWM Techniques Based on Space Vector Approach" IEEE Transactions on Power Electronics, Vol. 21, No. 4, January 2009.

[5] M. Schweizer, T. Friedli, J.W.Kolar "Comparative Evaluation of Advanced Three-Phase Three-Level Inverter/Converter Topologies Against Two-Level Systems" IEEE Transactions on Industrial Electronics, Vol. 60, No. 12, pp. 5515-5527, January 2014.

[6] Prieto J, Jones M, Barrero F, Levi E, Toral S. "Comparative Analysis of Discontinuous and Continuous PWM Techniques in VSI-Fed Five-Phase Induction Motor" IEEE Transactions on Industrial Electronics. 2011.

[7] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," IEEE Transactions on Industrial Applications, Vol. 41, No. 3, May. 2005.

[8] S.Bernet, K. Jalili and D. Krug "Design and Characteristics of a Rotor Flux Controlled High Speed Induction Motor Drive Applying Two-Level and Three-Level NPC Voltage Source Converters" IEEE Transactions on Industrial Electronics. 2005.

[9] S. Chiniforoosh, J. Jatskevich, A. Yazdani, "Definitions and applications of dynamic average models for analysis of power systems" IEEE Transaction on Power Delivery, Vol. 25, No. 4, Oct. 2010.

[10] VenkataDinavahi, Reza Iravaniet. all "Dynamic Average Modeling of AC-DC Converters for Power Systems Applications" IEEE Transactions on Industrial Electronics, Vol. 50 NO.6, 2009.

[11] Wenxi Yao, Haibing Hu, and Zhengyu Lu "Comparisons of Space-Vector Modulation and Carrier-Based Modulation of Multilevel Inverter" IEEE Transactions on Power Electronics, Vol. 23, No. 1, January 2011.

[12] Yushu. Zhang, G. P Adam, T. C. Lim, B.W. Williams "Voltage Source Converter in High Voltage Applications: Multilevel versus Two-level Converters" AC and DC Power Transmission IET, Published by IEEE, 2011.

[13] Zhou Keliang, Wang Danwei "Relationship Between Space-Vector Modulation and Three-Phase Carrier-Based PWM: A Comprehensive Analysis" IEEE Transactions on Industrial Electronics, Vol. 49, 2002.

APPENDIX

V_{DC} can be calculated using,

$$m_a = \frac{\sqrt{3}\, V_{ref}}{V_{DC}}$$

This can be re-arranged for the fundamental line-to-line (rms) voltage as $m_a = \frac{V_{ref}}{V_{DC}} = \frac{V_{L-L}\sqrt{2}}{V_d} = 1$

$$\therefore V_{DC} = 4160\sqrt{2} = 5883\ V$$

The RL load can now be determined whereby using the per-unit system analysis $V_B = V_\Phi = \frac{V_{L-L}}{\sqrt{3}} = 2402\ V$. The base impedance is hence defined as $Z_B = \frac{V_B}{I_B} = \frac{2402}{138.8} = 17.305\ \Omega$. Thus, for the given power factor,

$$R_{load} = \frac{V_{L-L}}{\sqrt{3} \times I_B} \cos\theta \approx 15.57\ \Omega\ per\ \Phi$$

Inductance load is similarly found as $L_{load} = \frac{V_{L-L}}{\sqrt{3} \times I_B\ \omega_B} Sin\theta$, where $\omega_B = 2\pi f$ and $f = 60\ Hz$. Hence

$$L_{load} = \frac{V_{L-L}}{\sqrt{3} \times I_B\ \omega_B} Sin\theta \approx 20\ mH\ per\ \Phi$$