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3T XOR Gate Using Dual Mode Gate

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ABSTRACT*: In this brief, we introduce novel low-power dual mode logic (DML) family, is designed to operate in 3T XOR gate in the sub threshold region. This proposed logic family can be switched between static and dynamic modes of operation according to system requirements. In static mode, the gates (DML)feature very low-power dissipation with moderate performance, while in dynamic mode they achieve more performance, with increased power dissipation. This is achieved with a simple concept.The simulation results are discussed by using Tanner. The proposed methodology is shown in 3T XOR GATE by using 45nm process.*
INDEX TERM*: Dual mode logic, High performance, 3T XOR Gate*

I. INTRODUCTION

In the advancements of technology and the expansion of mobile applications, power consumption has become a primary focus of attention in VLSI digital design. Recently, digital sub threshold circuit design has become a very promising method in ultralow powerapplications[1].Circuits operating in the sub thresholdregion, utilize a supply voltage (*V*DD*)* that is less than the threshold voltages of the transistors, which allows significant reduction ofboth dynamic and static power. The most common logic design family used for sub threshold today isCMOS. Ultralow voltage operation, which offers low-tomoderate performance with ultralowpower dissipation, was examined for the first time in 1972 and was originally used forlow throughput applications such as wrist watches, biomedical devices, and sensors .Dynamic logic, such as domino logic, has been used since the 1970's for high-performanceapplications. In the past, there have been several attempts to use dynamic logic in sub threshold to improve the speed. In this brief, wepropose a novel logic family, dual mode logic (DML), designed to operate in the sub thresholdregion[2]. DMLachieves an improvement in speed of up to 10× compared to a standard CMOS, whiledissipating 1.5× more power. In the static mode, a 5× reduction of power dissipation isachieved, compared to a basic domino, at the expense of a magnitude decrement inperformance. The earlier designs of XOR gate was based oneither eight transistors or six transistor or four transistor that are usually used in most designs. This paper proposes a new design technique for a 3T XOR gate.

II. DML STRUCTURE AND PRINCIPLE OF OPERATION

The DML logic family may be switched between static and dynamic modes of operation according to system requirements. DML logic circuits areto operate in the sub-threshold region. A dual-mode logic gate, for selectable operation in either of static and dynamic modes containing: a static gate at least one logic input and a logic output. Mode selector configured for outputting a turn-off signal to select static mode operation and for outputing a dynamic clock signal to select dynamic mode operation and a switching element associated with the mode selector static gate containing a first input connected to a constant voltage, a second input for imputing the mode selection signal from the mode selector, and an output connected to a logic output of the static gate. The dual-mode logic gate is configured to: i) disconnect the static gate output from both of the first and second inputs when the mode selector applies the turn-off signal to the second input; and ii) connect the static gate output to both of the first and second inputs when the mode selector applies the dynamic clock signal to the second input. The static gate contain a type-A gate and the switching transistor a p-type transistor, the second diffusion connection being connected to a high constant voltage. The static gate contain a type-B gate and the switching transistor comprises an n-type the second diffusion connection being connected to a low constant voltage. The basic DML gate architecture is composed of a standard CMOS gate and anadditional transistor M1 gate is connected to a global clock signal[4],[5]l. The DML aims to allow operation in twomodes: static mode and dynamic mode. To operate the gate in the dynamic mode,the clk is assigned an asymmetric clock, allowing two distinct phases are: precharge andevaluation. During the precharge phase, the output is charged to high/low,

depending on thetopology of the DML gate. In the evaluation phase, the output is evaluatedaccording to the values at the gate inputs. The DML topologies, marked *Type A* and*Type* B.Type A has an added p-MOS transistor that precharges theoutput "1" during the precharge phase.Type B has an added n-MOS that precharges the output to a logical "0." Dynamic logicgates are often implemented using a footer, which requires an additional transistor. The footer isused to decrease precharge time by eliminating the ripple effect of the data advancing throughthe cascaded nodes and allowing faster precharge. Switching the DML gate to operate in CMOS-like (i.e., static mode) operation: the global Clk should be fixed high for Type A topology and constantly low for Type Btopology.

A. Dual Mode Logic Gate

DML gate architecture includes: A static gate. A switching element connected to the output of static gate and Mode selector connected to the input of the switching element. Mode selector switches between the two functional modes, static and dynamic, by applying the required signal at the input of switching element.

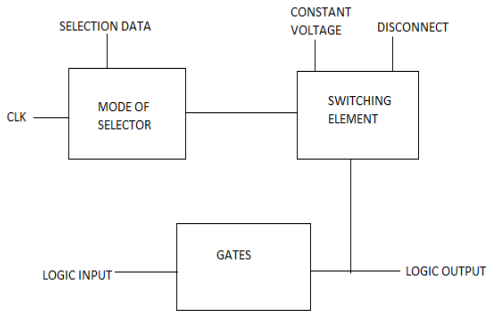

Fig. 1 Circuit Diagram of Dual Mode Logic Elements

When static mode is selected, switching element creates no electrical connection between the static gate output and other portions of the circuit enabling static operation. For example, in a p-type transistor serving as switching element the term "disconnect" may be considered similar p-type CMOS transistor having one diffusion input connected to high when the gate signal is high thereby turning off the p-type CMOS transistor. During dynamic operation, switching element receives a dynamic clock signal provided by mode selector which periodically connects the static gate output to a constant voltage level allowing dynamic operation.

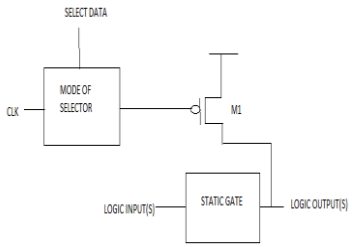

Fig.2 Type A DML Gate.

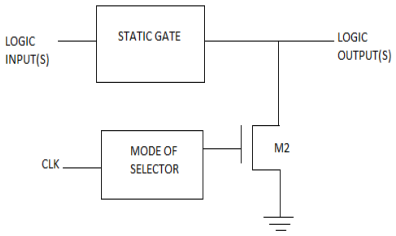

Fig. 3 Type B DML Gate.

When the DML gate is operated in the static (e.g. CMOS) mode, mode selector applies a constant logical value to the M1 gate, thus turning off switching transistor M1. During static operation the gate input should be fixed to a constant high for Type A topology and constant low for Type B topology. As a result,

switching transistor M1 has almost no effecton the topology. Mode selector has one or more data inputs for inputting data used to determine whether static or dynamic mode is selected.

Dynamic logic gates are often implemented using a footer, which requires an additional transistor. The clock signals applied to the M1 and M2 gates of an exemplary Type-A DML logic gate with footer, during the pre-charge and evaluation phases respectively Mode selector inputs a global Clk signal which goes low, turning on the pre-charge switching transistorM1, and charging the output high.The footer M2 is closed by disabling a path to the ground. To allow precharge, the inputs should be low, even though this is not compulsory when using footer.

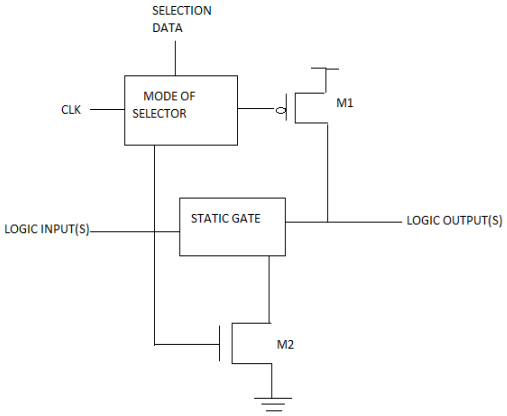

Fig.4 Type A DML gate with an NMOS footer

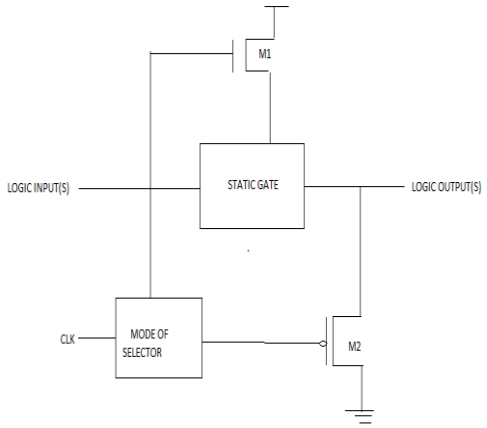

Fig.5 Type B DML gate with a pMOS footer.

Mode selector inputs is high Clk signal by turning off the upper pMOS transistor and opening a path to the ground through the footer. During the evaluation phase, the logic output is evaluated based on the input logic signal. Dynamic mode operation for a Type-B DML gate with footer is performed in a similar manner.

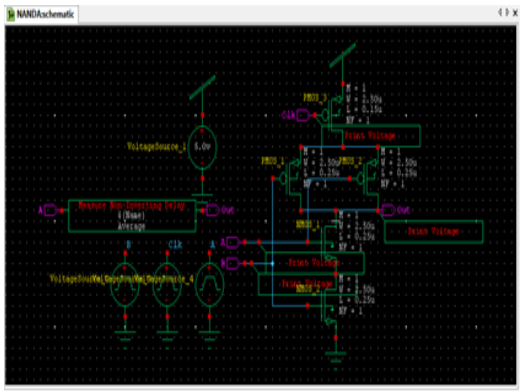

Fig. 6 Type A DML gate with a header

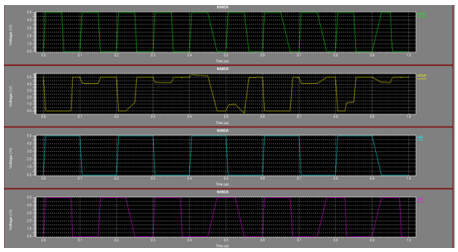

Fig .7 Corresponding waveform

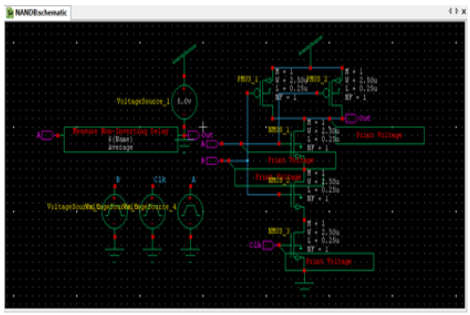

Fig.8 Type A DML gate with a header

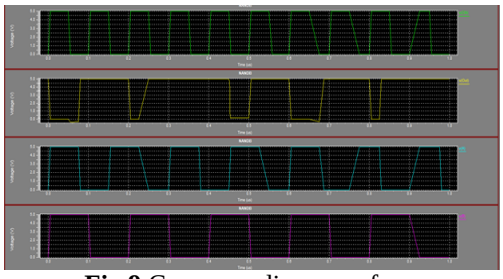

Fig 9 Corresponding waveform

III. PROPOSED WORK

The significant of 3T XOR gate is mainly to minimize the area and power savings. It is based on CMOS static inverter and pass transistor logic.

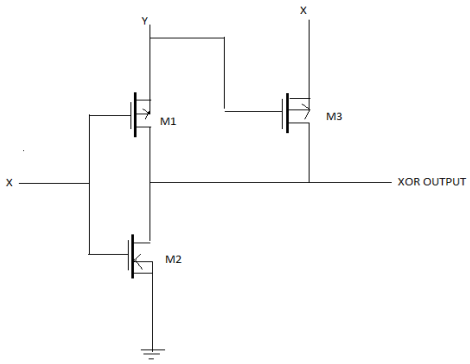

Fig.10 Circuit diagram of 3T XOR Gate

The proposed XOR logic gate using three transistors. The design is based on modified CMOS inverter and PMOS pass transistor logic. When the input Y is at one, the inverter on the left functions as a normal CMOS inverter. Therefore the output is the complement of input X. When the input Y is at zero, the CMOS inverter output is at high impedance. However, the PMOS pass transistor M3 is turned ON and the output gets the same logic value as input X. The operation of the whole circuit could be given as a 2 input XOR gate as given in Table.

INPUT A	INPUT B	OUTPUT=X'Y+XY'
0	0	X/0
0	1	X'/1
1	0	X/1
1	1	X'/0

Existing system produced of high power dissipation and delay. In the proposed method power dissipation and delay is reduced by adding 3T XOR gate in dual mode CMOS NAND gate. It is mainly used in low power consumption application.The proposed methodology is shown in a 45nm CMOS process. In general , 3T XOR gate the average power consumption is 6.14 $e^{-0.08}$ watts. In this type A 3T XOR gate the PMOS is connected to the header.The power consumption 7.95 $e^{-0.08}$ watts.

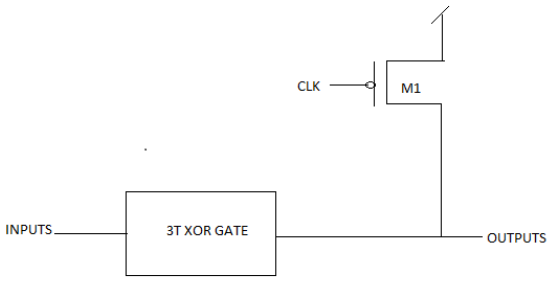

Fig. 11 Type A 3T XOR with header.

In this type A 3T XOR gate while the NMOS is connected to the footer. The power consumption 2.69 $e^{-0.08}$watts. When compared to the type A the average power consumption is less in type B.

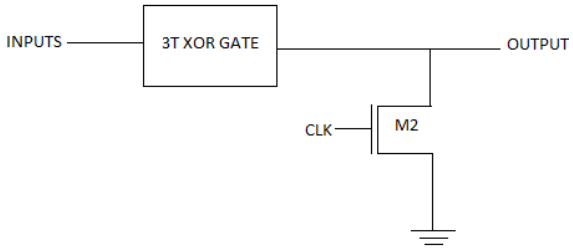

Fig.12 Type 3T XOR with footer.

DML 3T XOR gate can be switched between static and dynamic mode of operation according to the system requirments.

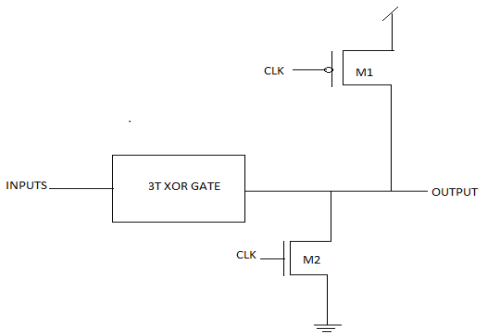

Fig .13 3T XOR with header and footer.

In this DML 3T XOR gate the PMOS is connected to the header and the NMOS is connected to the footer. The power consumption 5.703 $e^{-0.04}$ watts.

IV. CONCLUSION

The 3T XOR gate based DML logic networks was presented.CMOS NAND gate has the high power consumption but in the proposed 3T XOR gate using dual mode gate has reduction in the power consumption and also has high speed.45nm design process is implemented.

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