IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
Vol. 06, Issue 11 (Nov 2016), ||V1|| PP 62-71

Novel applications of an isolated active power filter using a transformer

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Abstract**:** This paper proposes a decreased voltage transformer coupled shunt hybrid active power filter. It is designed with two inverters with a split dc link voltage. The dc voltage of the HFI is decreased by the transformer's turn ratio. The LFI provides a limited reactive power handling capability due to the high reactance in the shunt path, however it provides excellent harmonic compensation at reduced price switches are used in the HFI while IGBTs are used for the LFI. PWM based controller and hysteresis controller for operating the LFI and HFI respectively are used. The performance of the proposed topology and controller are designed in MATLAB/SIMULINK. The benefits of the topology is confirmed by validating it in an experimental setup.

Index Terms—Active Power filter (APF), harmonics, transformer, passive filter, low frequency inverter (LFI), high frequency inverter (HFI)

I. INTRODUCTION

The Shunt Active Power Filters are generally used for removing the harmonics from current and suppress the Reactive Power. Researchers from the past 20 years have been trying to work upon these areas [1-33]. There are three basic aspects of operating the shunt active power filter: Namely reference generation technique, reference tracking and topology design respectively. The reference current can be computed in the time domain and frequency domain. Now a days soft-computing based reference generation technique has gained its importance due to the availability of digital memory and processors at low price. The ANN based reference generation technique also has come to light in this area, Bhattacharya *et. al* have presented a paper on adaline based harmonic compensation for reference generation [11]. APF also requires to track the reference current to compensate the harmonics. Matas *et. al* proposed sliding mode based tracking method to improve transient stability of the system [8]. Researchers are trying to build effective topologies of the shunt active power filters for their specific applications in the industries. S. Bhattacharya *et. al* proposed the design of the shunt active filter in using two inverters and transformers to compensate the 5^{th} and 7^{th} harmonics[10]. Srianthumrong *et. al* proposed a medium voltage transformer less topology for compensating the reactive power and harmonics [9]. Bhattacharya *et. al* proposed a dual parallel topology with reduced switches to compensate the current harmonics [4]. This paper proposes a new topology with a single transformer wish split dc link .The primary of the transformer along with the capacitor are tuned to 6^{th} harmonics to eliminate the 5^{th} and 7^{th} from the load current. The secondary is tuned to 12^{th} harmonics eliminate the11^{th}and13^{th} harmonics from load current.The Paper is written in six sections. Section I introduces the paper. Section II reports the implementation of APF and transformer design. Calculations of the two band pass filters connected on both the sides of the transformer are also discussed in the same section. Controller design is reported in section III. Simulation and experimental results are shown in section IV and V. Section VI concludes the work.

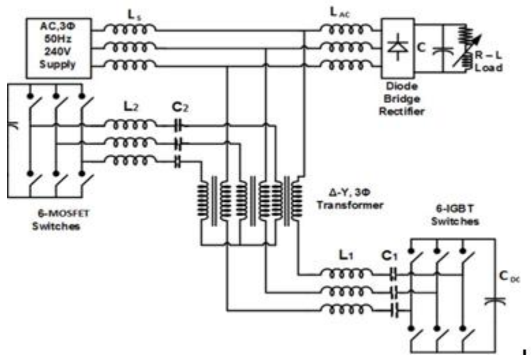


Fig.1 A proposed transformer based shunt active filter topology

II. Active filter implementation and transformer design

The proposed hybrid APF is implemented by two three phase VSI (Voltage Source Inverter). One VSI is used for dedicated compensation of 11th & 13th higher order harmonics. The inverter is operated at higher switching frequency thus it is termed as High Frequency Inverter (HFI). As shown in Fig.1 another VSI is used to compensate 5th and 7th harmonics and this inverter is operated at lower frequency thus it is termed as Low Frequency Inverter (LFI).The reactive power demand is compensated by the same VSI .The Primary side of the transformer is connected through an LC filter to the LF-VSI. The filter is tuned tune near 6th harmonics as reported in [4].The secondary side of the transformer is connected through a passive filter tuned to near 12th harmonics with a high q-factor. The L-C combinations and HFI mitigates all the harmonics above 11th.

The inverter eliminating lower harmonics has a switching frequency of 5 kHz and it is SPWM based. While HFI uses hysteresis controller for its simplicity in implementation and the average frequency is kept at 20kHz.

The transformer reduces the dc link by its turn ratio. It facilitates the use of cheap high frequency lower voltage rating switches. It also reduces voltage rating of capacitor by the turn's ratio. Moreover size and rating transformer is extremely low compare to total KVA rating of the system, since it is designed to compensate higher order lower strength harmonics. LC filter in secondary also ensure that current does not flow into secondary winding for lower order harmonics. However the reactive power handling capability of proposed topology is limited and it is VAR handling capability may calculated from (1). The LC filter inserted into the shunt path offer higher impedance for flow at power frequency. The reactive power handling capacity of proposed topology is calculated as shown in [4]. The reactive power capability mostly depends on the voltage ratings and value of C_1. The effect of C_2 is very low as the referred value of C_2 in primary is negligible because it is divided by the transformer's turn ratio's square.

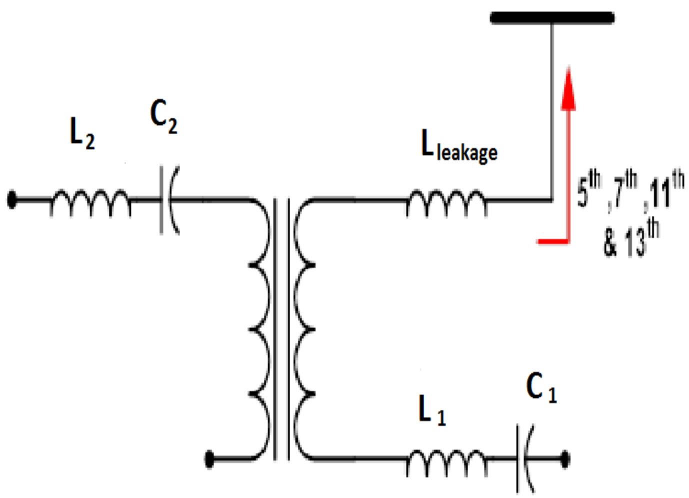
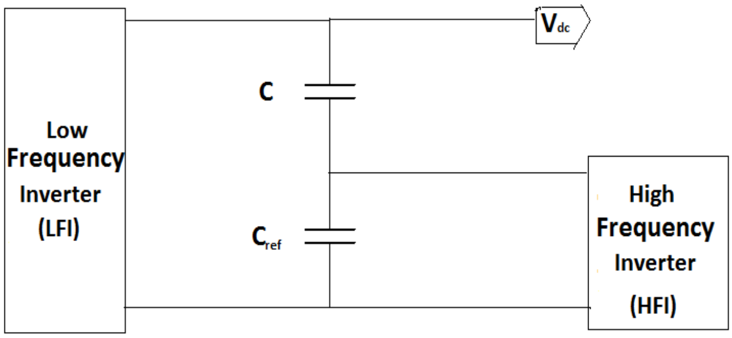


Fig.2(a) Tuning both the LC filter for eliminating 5th,7th & 11th ,13th harmonics respectively from the load current

$$Q_C = 3\omega C_1 V_{C1}^2 \qquad (1)$$

Even though reactive power handling capacity of proposed topology is limited but it provides the designer enough flexibility to choose a the APF with proper KVAR compensating capability for given rating capacitor and its and voltage rating. E.g. higher voltage rating of capacitor will increase KVAR rating of APF but it will also increase total cost of the system. Moreover higher the value of capacitor will increase the stability of the system however it will reduce voltage across capacitor. A small signal analysis based stability study reported in [4] and from that analysis value of capacitor and its voltage rating is selected for given reactive power ratings.

Researchers have observed that simulation gives excellent results for a Q-factor of about 25 to 35 for primary side and 30 to 40 for secondary side The dc link capacitor is maintained by LFI. DC link capacitor is spilted for HFI and LFI are shown in Fig.2 (b). For this proposed topology the dc link capacitor is kept n times higher than the C_1 to bring down the dc link voltage to 1/n times of the supply voltage.



. Fig.2(b) equivalent circuit of dc link

III. CONTROLLER

The LFI and HFI both operate in the feedback mode, the sine and cosine rotational transformation are generated in the standard way with two voltage transducers sensing the two voltage vectors and thereby generating the third vector. Parks transformation is then applied to find the sine and cosine of the components. The LFI's switching pattern is generated by using a sine PWM technique with a switching frequency of 5 kHz. While the HFI is operated using a hysteresis control with a mean frequency of about 20 kHz . The use hysteresis control helps in reducing the complexity of the controller. One of the disadvantage of hysteresis controller is that its switching frequency is not constant. The constant band hysteresis controller ensure that drifting of switching frequency is content with in 1% of mean switching frequency. The load current is converted in abc-dq frame with park transformations. The cut off frequency of LPF (low pass filter) is kept such way that the subtraction generates higher order harmonics (i.e. 11^{th} & 13^{th}) in d-q domain. This $d^{\sim}$ and $q^{\sim}$ is used as the reference to operate the switching of HFI. To generate reference for LFI 6^{th} harmonic component of sine and cosine function are used for the parks transformation. It is implemented in simulation by SIMULINK using abc to dq transformation block while the hysteresis control is achieved by the relay block and the PWM is realized by the standard simulation modeling techniques.

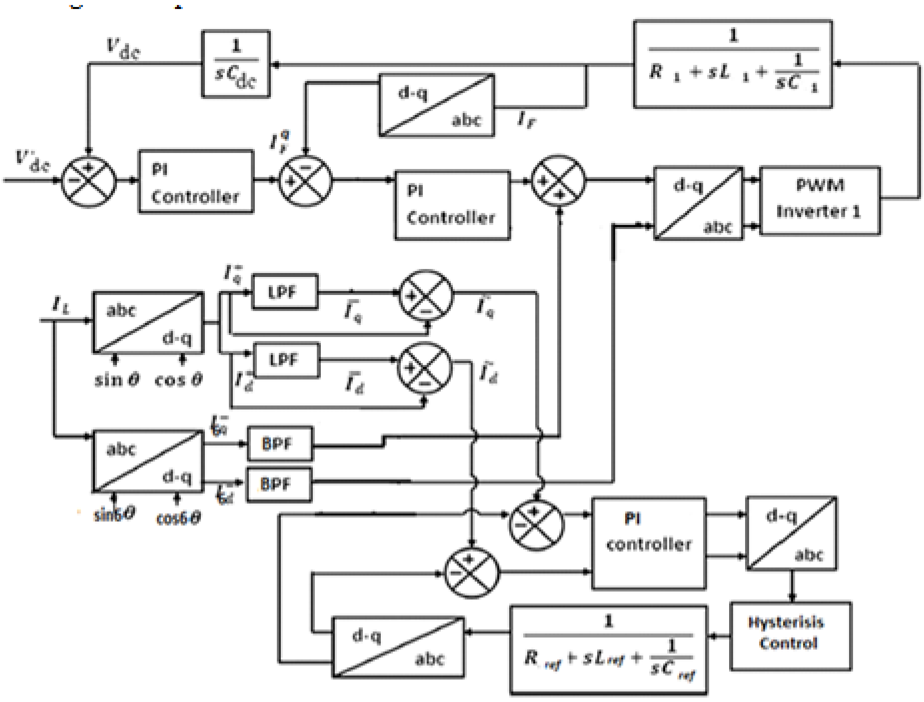


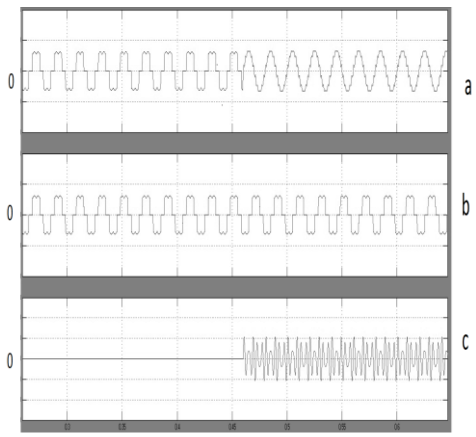
Fig.3 Block Diagram of the proposed Controller

IV. SIMULATION RESULTS

Simulation of the system is configured on SIMULINK . The Powersim block is used to construct the voltage source inverters ,transformer and diode bridge rectifier. The switching frequency of the low and high frequency inverters is set at 5 kHz and 20 kHz(mean) respectively. The LFI is made with IGBT based switches while the HFI has reduced DC link voltage thereby lowering the need of maximum voltage handling capacity. MOSFET based switches are used for buildup of the HFI . A highly inductive R-L load feed through the diode bridge rectifier is considered as nonlinear load. for reference generation. This load current in d-q axis is feed to band pass filter to extract reference for low frequency harmonics.

Inverter dead time is kept 2 μs for avoiding the shorting of the two lines.

Fig.4 shows steady state operation of APF. The source current, load current, compensating current of low and high frequency is shown in top to bottom order. The harmonic strength of corresponding source current(compensated) and load current is shown in Fig.8 .The THD of compensated source current is 4% This THD satisfies the requirement the IEEE 519 standards.



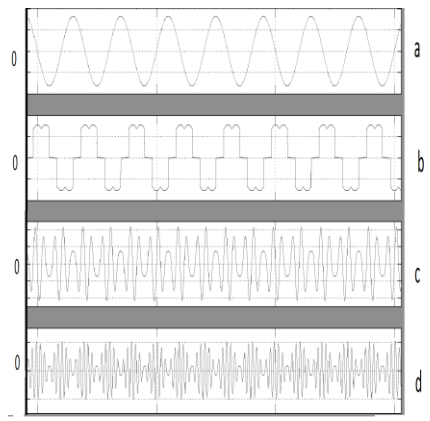


Fig.5 Starting of LFI
a) Source current (Sclae:20A/div)
b) Load current (Sclae:20A/div)
c) Output of only LFI(Sclae:10A/div)
Time div 50msec/div

Fig.5 Series2 shows individual harmonic strength
For load current for fig. 5

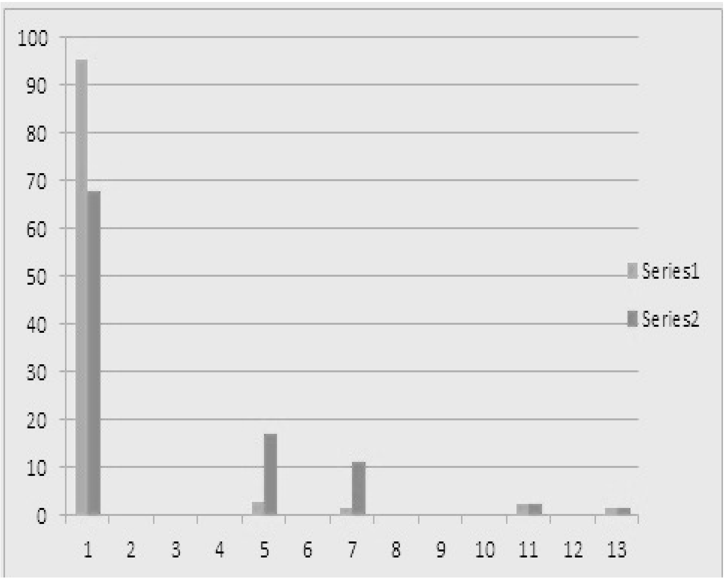


Fig.6 operating with only LFI (THD is 8%) series1 shows individual harmonic strength
For compensated source current for

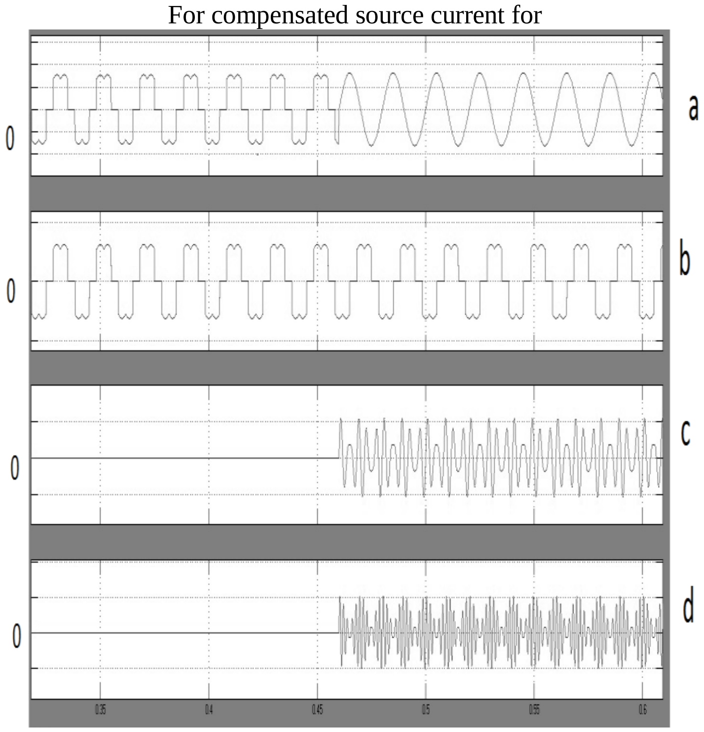


Fig.7 starting of both the inverters
a)source current (Sclae:20A/div)
b)Load current (Sclae:20A/div)
c)LFI current (Sclae:10A/div)
d)HFI current (Sclae:5A/div)
Time div Sclae: 50msec/div

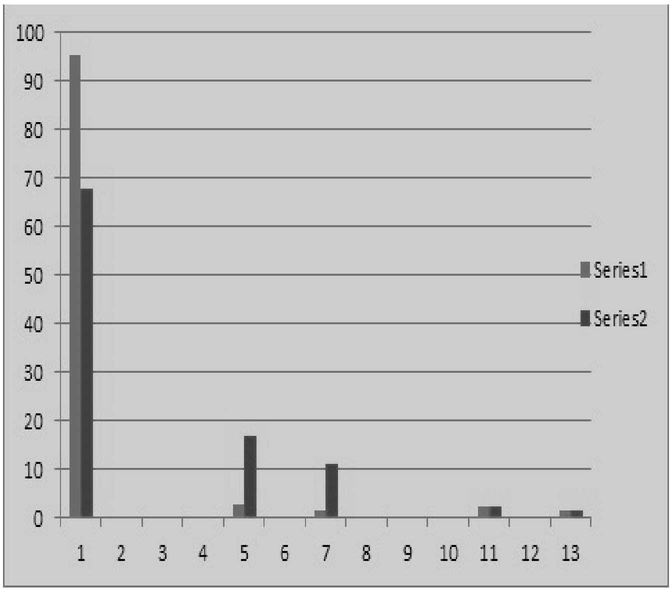


Fig.8 operating with both HFI & LFI (THD is 4%) series1 shows individual harmonic strength For compensated source current Series2 shows individual harmonic strength For load current of Fig.4

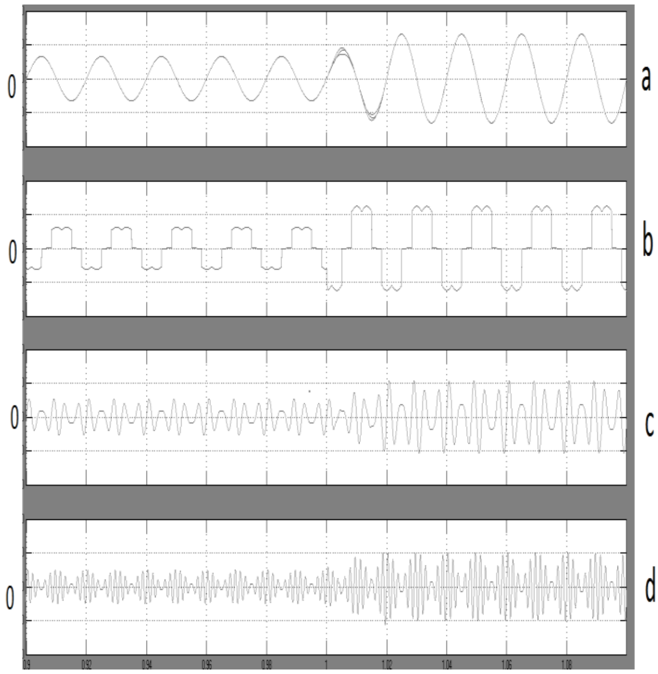


Fig.9 Step Change in load
a)source current (Sclae:20A/div)
b)load current (Sclae:20A/div)
c)LFI current (Sclae:10A/div)
d)HFI current (Sclae:5A/div)
Time div Scale: 50msec/div

As it can be observed clearly from Fig.5 and Fig.7 that both the inverters have a “glitch free” start, which is highly recommended for the smooth operation of the active power filter. Fig.5 shows starting of APF with LFI only. The source current, load current and compensating current of LFI are shown in top to bottom order. Fig.7 shows starting of both the inverter simultaneously. The source current, load current ,compensating current of LFI and HFI are shown in top to bottom order.

To manifest the working of the LFI , The APF is operated with only the LFI connected , as the higher harmonics are not compensated due to the absence of HFI thereby increasing the THD to be 8% as shown in Fig.8 The source current is compensated immediately after the starting of the inverter within two cycles and the load profile is left unaltered. The APF functions appropriately with a changing load and stabilizes its compensating action within one cycle. As shown in Fig.9 with a step change in load at 0.1 second after the start of simulation the APF works without any problem. In our course of investigations a highly inductive R-L load feeding through a diode bridge rectifier is considered as non linear load.

V. EXPERIMENTAL RESULTS

The proposed topology is also tested experimentally. The experimental prototype was made using MOSFET and IGBT's. The experiment was conducted at a supply of 240 volts , 50 Hz frequency with a load of 3kVA. The whole system is built in SIMULINK dsPACE-1104 environment. The experimental results observed are well matched with the simulation results. Researchers are carrying out extensive hardware implementation and further experimental results will be submitted at the time of final submission. Presently two hardware results have been provided to manifest performance of proposed system. Fig.10 shows the source voltage, source currents of phase A,B,C respectively of the APF. Fig.11 demonstrates the dynamic performance of the APF. Load change is occurred at a 32msec. The compensated source current, load current, compensating current of the HFI and LFI are shown in top to bottom order.

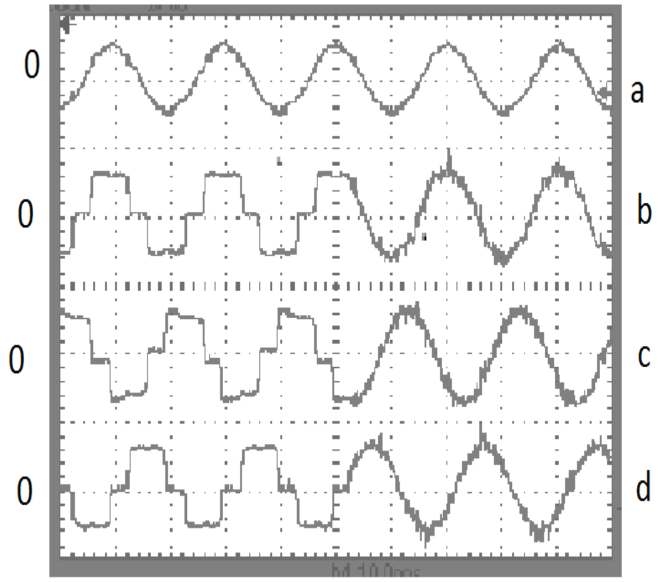


Fig.10 Source current before and after compensation
a) source voltage of phase A.(Scale:100V/div)
(b) source current of phase A.(Scale:10A/div)
c) source current of phase B. (Scale:10A/div)
d) source current of phase C (Scale:10A/div)
Time div 10msec/div

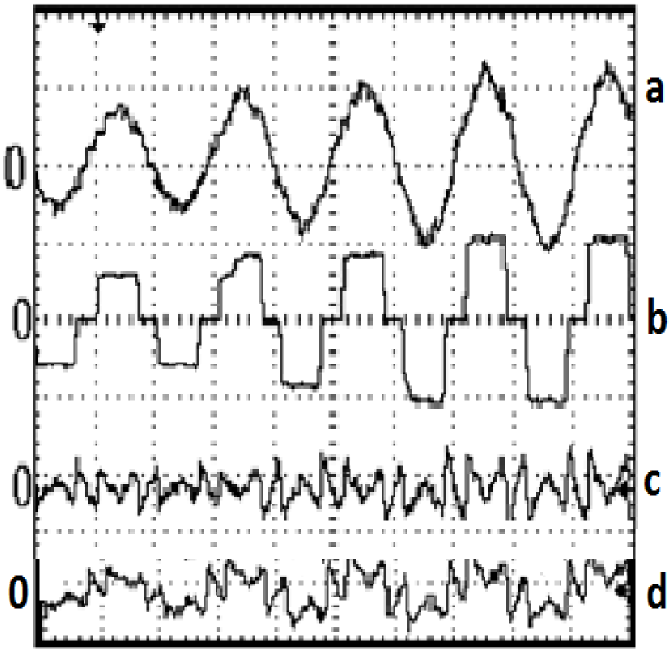


Fig.11 step change operation of shunt active power filter.
a) source current. (Scale:10A/div)
b) load current. (Scale:10A/div)
c) compensating HFI current(Scale:10A/div).
d) compensating LFI current. (Scale:10A/div)
Time div 10msec/div

TABLE I SYSTEM PARAMETERS

Load Rating	3kW
Line Voltage	250V
Line Frequency	50Hz
Power system Inductance	0.2mH
A.C load inductor	3mH
D.C. capacitance across rectifier	2000 µF
Filter Inductance L_1	5.96mH
Filter Inductance L_2	1.49mH
Filter capacitor C_1& C_2	47 µF
Quality Factor LFI Filter	25-35
Quality Factor HFI Filter	30-40
LFI DC link voltage	100V
HFI D.C link Voltage	25V
LFI D.C link capacitor	1mF
HFI D.C. link capacitor	4.7mF

VI. CONCLUSION

The paper has proposed a reduced voltage transformer based topology that gives enhanced performance in reduced cost. The HFI connected through the transformer in shunt path has a reduced DC link voltage with the aid of the transformer. Since the transformer compensates the higher order harmonics, so its kVA rating is very low thereby minimizing the manufacturing cost. The LFI that is connected to the primary of the transformer is responsible for compensating the reactive power as well as the 5^{th} & 7^{th} harmonics even though it has a limited capacity for reactive power but still provides an excellent low cost solution for mitigating the lower order harmonics.

The proposed topology has been extensively simulated on SIMULINK . Researchers have also implemented the topology on an experimental set up using dsPACE-1104 and the results of simulation and hardware implementation match well with each other thereby confirming the usefulness of the proposed topology.

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