IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
Vol. 07, Issue 02 (Feb. 2017), ||V1|| PP 01-07

High frequency unity power factor resonant converter with adjustable brightness for electronic ballast lamp applications

M.Vijayasanthi [#1], Dr.M.sushama [*2]
[#] *EEE, CMR College of Engineering & Technology, Secunderabad, India*
[1] *reenareeva@gmail.com*
[*] *EEE,JNTUH Hyderabad, India*
[2] m73sushama@yahoo.com

Abstract:- In this paper we propose a high frequency unity power factor correction resonant converter for electronic ballast lamps. The change in the switching frequency of the converter changes the output voltage amplitude of the converter also changing the harmonic distortion in the output voltage and current. To maintain the input current shape the converter employs small energy tanks reducing the THD of the input current. The efficiency, THD of the converter are analyzed in MATLAB Simulink software with respect to change in switching frequency and presented in this paper**.**

Key words: Total Harmonic Distortion (THD) Matrix Laboratory (MATLAB)

I. INTRODUCTION

With advancements in electrical technology the demand of loads are increasing day by day. Traditional loads or equipment in domestic and commercial usage are less efficient and consume more power from the source and also inject harmonics in the supply. In many domestic and commercial loads lighting is the major part of power consumption. Replacement of electromagnetic ballast lamps with electronic ballasts are increasing for efficient light performance operation and harmonic elimination [1]. To get high frequency output voltages the input AC voltage needs to be converted to DC with DBR (Diode Bridge Rectifier) with an attachment of high rating capacitor for reduction of ripples in the DC output voltage for high frequency inverter operation. This utilization of converters for high frequency applications drains large current from the source with poor input power factor and harmonic distortions in input voltage and current. To avoid these issues of power quality [2], maintaining the power factor and reduction of harmonic generation is a major concern for these converting operations. For the improvement of input power factor many filtering methods have been employed in which a simple passive element (inductor) is the basic filtering option with also harmonic reduction for these converters. Addition of few inductors and capacitors at the input source before the rectifier merely reduces the harmonics and shapes the input line current to sinusoidal. For achieving unity power factor more than 0.9 the capacity of these filter elements [3,4] must be increased to a larger value in turn increasing the size of the elements which is impractical after an extent. Rather than increasing the capacities of these elements, sophisticated circuit topologies can be introduced for unity power factor and harmonic elimination capabilities of the converter. With increase in complexity of control topology [5] the cost of the equipment for the circuit fabrication also increases, resulting in increment of economy making it a disadvantage to the converter. It is very important to keep the cost of the converter in a specified range to compete with products in the market. In this paper we introduce a PFC circuit topology for electronic ballast lamps application with series resonant converter in very low economical range. The proposed converter topology has reduced THD [6] and input line current shaping capabilities achieving unity power factor without any additional passive elements.

II. PROPOSED CIRCUIT TOPOLOGY

The proposed resonant converter for electronic ballast lamp can be seen in fig. 1 with two controllable MOSFETs as power switches [7]. The MOSFET is connected to an anti parallel diode which gives the ability to conduct in positive and negative directions. The load considered here is an equivalent circuit of lamp comprising of parallel resistive and inductive elements. For starting of the lamp a capacitor C_L is connected in parallel.

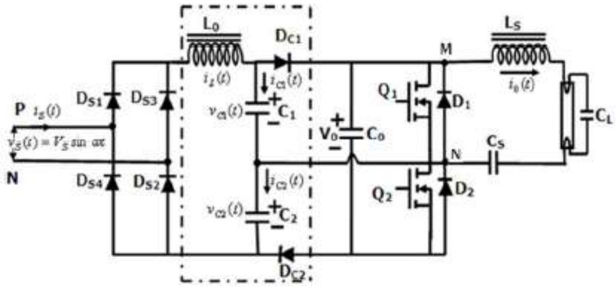

Fig. 1: Proposed resonant converter with PFC

Both MOSFETs (Q1 and Q2) switch ON and switch OFF alternatively with a variable frequency of 50kHz to 500kHz. The resonant frequency of the proposed topology has be maintained below the switching frequency for inductive load operation. For a smooth DC link voltage [8] a bulk capacitor C_0 is connected before the resonant circuit. During the operation of the inverter the bulk capacitor draws a small peak current from the source reducing the power factor and increase in harmonic distortion of the source. To avoid this issue of power quality a PFC (Power Factor Correction) circuit [9,10] is introduced before the bulk capacitor which can be observed in fig. 1 enclosed in dotted lining. The PFC circuit comprises of an inductor with two series capacitors C1 and C2, with also two freewheeling energy transfer diodes D_{C1} and D_{C2}. The two storage devices C1 and C2 charge and discharge with a high frequency providing some of the power output to the load. As the charge and discharge of these power tanks takes place at a high frequency, the capacities of these devices is very low. The two energy transfer diodes D_{C1} and D_{C2} transfer the energy from inductor Lo to the large storage device C_0. The arrangement of these passive elements in the PFC circuit drains the current in phase with the input voltage with high frequency oscillating sinusoidal structure [11]. These oscillations in the input current can be removed with an input filter connected after the source making the current signal more sinusoidal.
The input voltage can be expressed as

$$V_{ac}(t) = Vm \, Sinwt \qquad (1)$$

Here V_m = voltage amplitude, w = frequency given as 2*pi*f with respect to time ‘t’
The sinusoidal input voltage is fed to DBR (Diode Bridge Rectifier) converting the AC input voltage to pulsating DC. The pulsating DC voltage is fed to PFC circuit which drains current from the source represented as

$$I_{ac}(t) = I_m \, Sinwt \qquad (2)$$

Here I_m = current amplitude, w = frequency given as 2*pi*f with respect to time ‘t’
The below two tables have the switching states of each switch for particular interval of time.

TABLE I
For interval at every π/8 radians

Device/ interval	I	II	III	IV	V
D_r	ON	OFF	OFF	ON	ON
D_{C1}	OFF	OFF	ON	ON	ON
D_{C2}	ON	OFF	OFF	OFF	OFF
Q_1	OFF	OFF	OFF	OFF	ON
D_1	OFF	OFF	OFF	OFF	OFF
Q_2	ON	ON	OFF	OFF	OFF
D_2	OFF	OFF	OFF	OFF	OFF

For interval at every π/2 radians

Device/ interval	I	II	III	IV
D_r	ON	ON	ON	ON
D_{C1}	ON	ON	ON	ON
D_{C2}	ON	OFF	ON	ON
Q_1	OFF	OFF	OFF	OFF
D_1	OFF	OFF	OFF	ON
Q_2	ON	OFF	OFF	OFF
D_2	OFF	OFF	OFF	OFF

When the MOSFET Q2 switches ON the capacitor C1 charges by the source line current through the booster inductor Lo. The charging line current during this switching state is given as

$$i_L = V_{ac} – (Vac\text{-}Vc1)\ Cosw_rt + I_L\ \sqrt{}(L_0/C1)\ sinw_rt \qquad (3)$$

Vc1 and I_L are the initial conditions of capacitor C1 and booster inductor L, w_r is the resonant frequency given as $w_r = 1/\sqrt{}(L_0/C1)$

The voltage across the capacitor is given as

$$V_{C1} = Vr – (V_{C1})\ cosw_rt + I_{Lo}\ \sqrt{}(L_0/C1)\ sinw_rt \qquad (4)$$

During the conversion of input voltage to DC by DBR at low voltages, the peak value of the capacitor voltage Vc1 will be less than the DC voltage output Vo of the PFC converter. In this operating state the input and the inductor current will be discontinuous [12]. During high voltages of the DBR the capacitor voltage Vc1 is reached to Vo, with the input current and inductor current continuous. The inductor current during this state is given as

$$i_L\ (t) = (Vr - Vo)t + I_{Lo2} \qquad (5)$$

After the freewheeling operation of the diode Dc1 the current comes to zero and the second mode starts with switching OFF of MOSFET Q2 and MOSFET Q1 switches ON. Now the second cycle begins with the charging of capacitor C2 and the operation continuous as discussed above with the switching ON of MOSFET Q2. Here the diode Dc2 is in freewheeling state and inductor Lo discharges through into the load. With these operation of switches alternatively a high frequency AC wave is generated and fed to the lamp.

III. SIMULINK MODELING AND DESIGN CONSIDERATIONS

The given proposed topology in fig.1 is designed in MATLAB Simulink software with below the parametric values in table II.

TABLE II

Vin	230Vrms 50Hz
Vdc link	320V
C1=C2	4nF
Lo	3.5mH
Fs	50kHz-500kHz
Co	1000uF
Cs	47nF
R lamp	410
L lamp	730uF
CL	3.6nF

The below figure is the Simulink modeling of the proposed circuit with the given parameters [14].

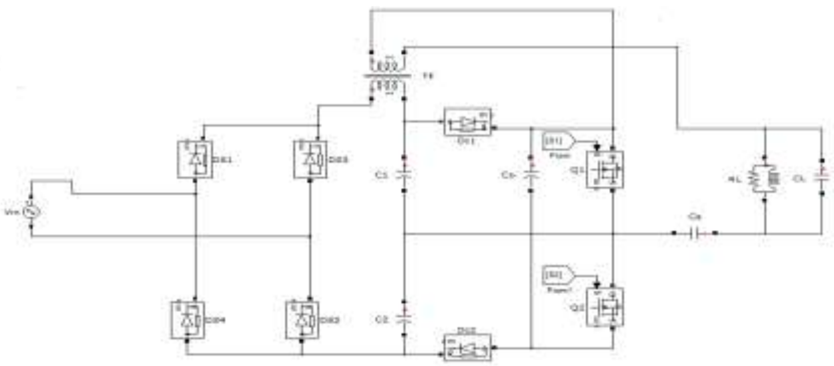

Fig. 2: Simulink modeling of proposed resonant circuit

The above topology is operated with different switching frequencies from 50kHz to 500kHz [13] and the characteristics of every element is observed with respect to time. Parameters like THD, power factor (cosθ) of input and output voltage and currents are observed also calculating the efficiency of the converter with change in switching frequency of the MOSFETs. The duty ratio of both the switches Q1 and Q2 are maintained at 50% operating alternatively. The below are the graphs of the elements at 500kHz operating frequency.

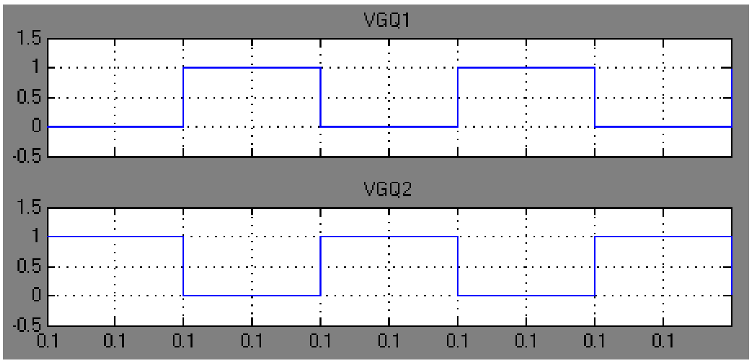

Fig. 3: MOSFET gate signals at 500kHz frequency

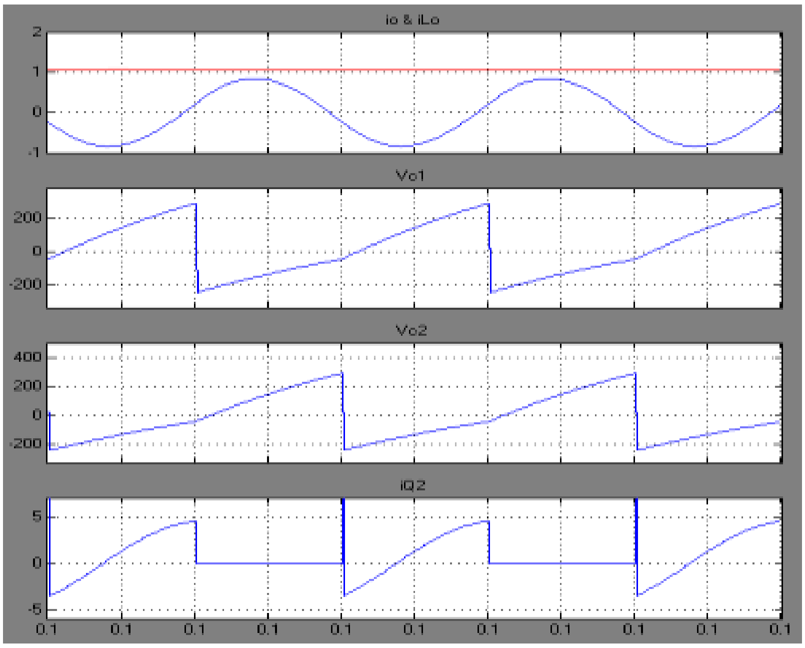

Fig. 4: Waveforms of axis 1: i_o- output current and i_{Lo}- inductor current; axis 2: V_{c1}- voltage of capacitor C_1; V_{c2}- voltage of capacitor C_2; axis 3: i_{Q2}- current through MOSFET Q_2.

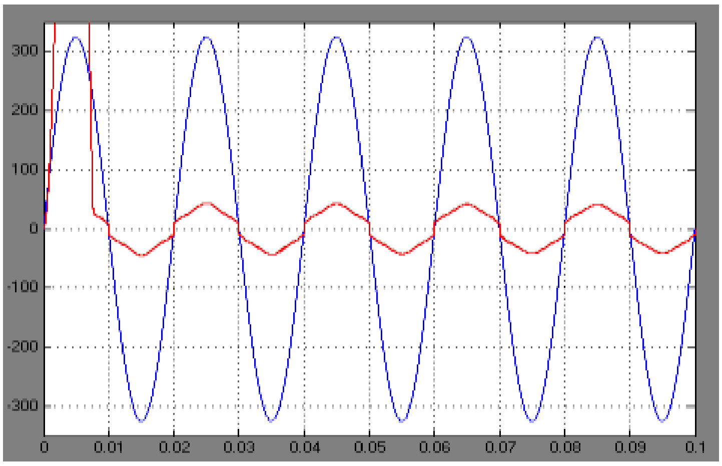

Fig. 5: Input voltage and input current

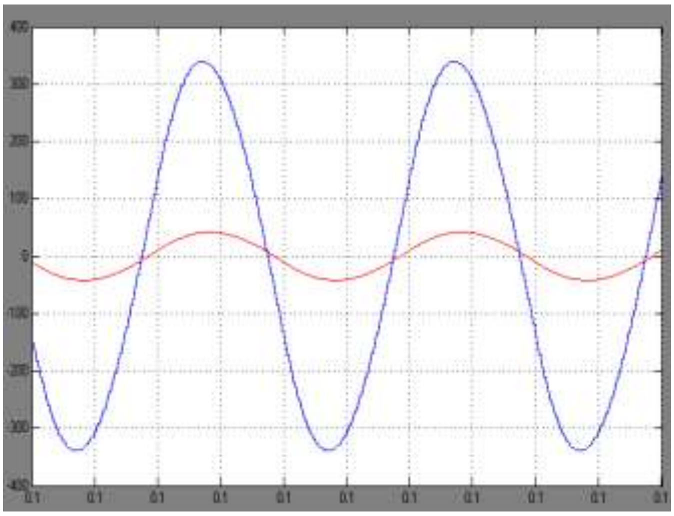

Fig. 6: Lamp voltage and lamp current

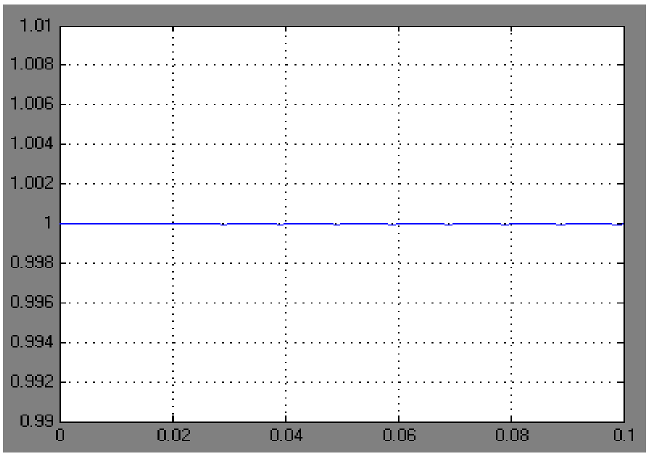

Fig. 7: Input power factor

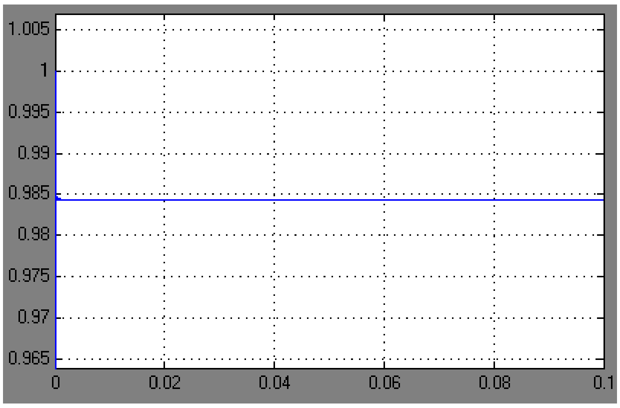

Fig. 8: Output lamp power factor

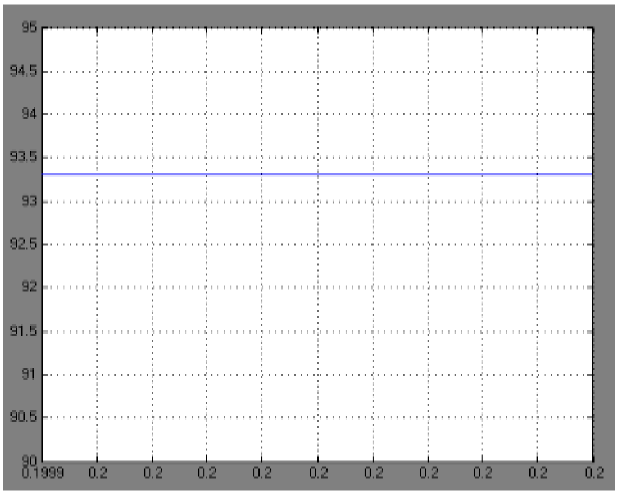

Fig. 9: Efficiency of the converter

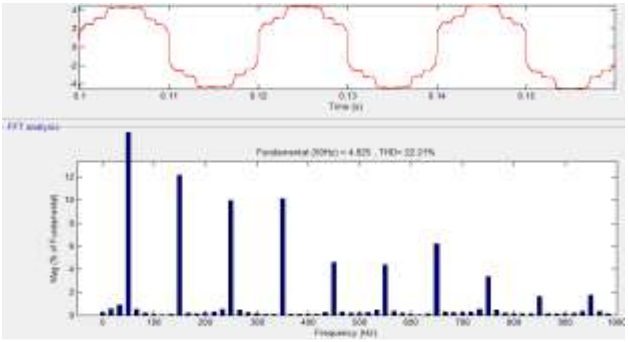

Fig. 10: FFT analysis of Input current

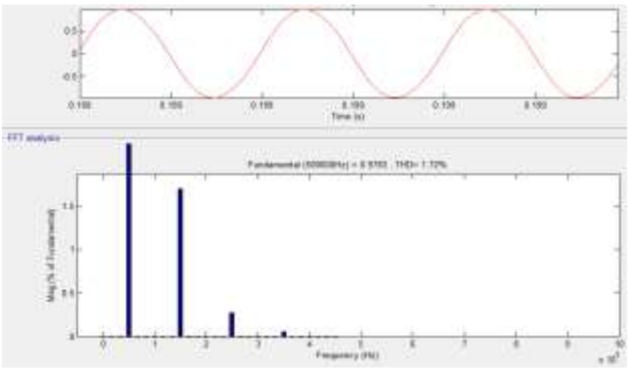

Fig. 11: FFT analysis of lamp current

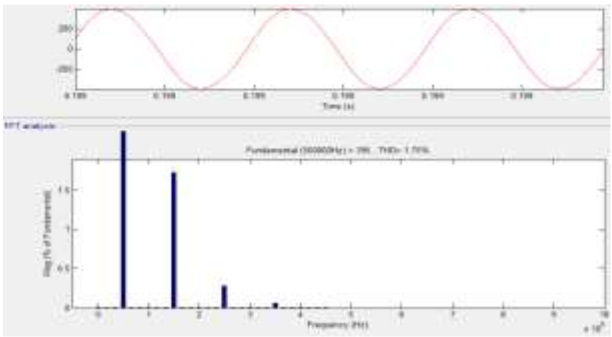

Fig. 12: FFT analysis of lamp voltage

TABLE III

Switching frequency (fs) kHz	THD Iin %	THD Vo %	THD Io %	Input Cosθ	Ouput Cosθ	Efficiency %
50	43	57	30	0.9	0.48	78
150	16	47	41	0.9	0.86	81.3
300	14.	2.6	2.5	0.9	0.95	85.6
400	15.3	1.2	1.1	0.9	0.97	92.2
500	22	1.7	1.7	0.9	0.98	93.3

IV. CONCLUSION

With the above results and analysis of the resonant converter with variable frequency from 50kHz to 500kHz it can be observed that at 400kHz the system is more optimal than below and above 400kHz. All the parameters with FFT analysis, power factor and efficiency calculation are given in TABLE III in comparison with other frequencies.

REFERENCES

[1]. Chen Zhao, Xinke Wu, Peipei Meng, and Zhaoming Qian"Optimum design consideration and implementation of a novel synchronous rectified soft switched phase shift full bridge converter for low output voltage high output current applications" IEEE Transactions On Power Electronics, Vol. 24, No. 2, February 2009 pp: 388-398.

[2]. Reas Ecklebe, and Reas Lindemann, and Sebastian Schulz "Bidirectional switch commutation for a matrix converter supplying a series resonant load" and, IEEE Transactions on Power Electronics, vol. 24, no. 5, may 2009 pp:1173-1183.

[3]. Laszlo Huber, Kevin Hsu, Milan M. Jovanovic, Dennis J. Solley, Gennady Gurov, and Robert M. Porter , "1.8-MHz, 48-V Resonant VRM: Analysis,Design, and Performance Evaluation" IEEE Transactions On Power Electronics, Vol. 21, No. 1, January 2006 pp: 79-89.

[4] M.C.Cosby and R.M.Nelms, "A resonant inverter for electronic ballast applications," IEEE Transaction on Industrial Electronics, vol. 41, no. 4, pp. 418–425, 2011.

[5] Yilei Gu, Zhengyu Lu, Lijun Hang, Zhaoming Qian, and Guisong Huang "Three level LLC series resonant DC/DC converter" IEEE Transactions on Power Electronics, Vol. 20, No. 4, July 2005 pp:781-790

[6] James E. Piper. "Operations and Maintenance Manual for Energy Management". Published M.E. Sharpe, ISBN 0765600501, 9780765600509, 2009.

[7] Godyak, V., & Shaffer, J. "Endura: A new high output electrodeless fluorescent light source". Institute for Low-Temperature Plasma Physics Greifswald Proc 8th Int. Symp. On Light Sources, pp. 14 - 23 Fev. 1998.

[8] Endura, Osram. "The high performance electrodeless fluorescent lamp -Quicktronic intelligent". Digital Catalog, p.102, Nov. 2005.

[9] Chang-Shien Lin; "Low power 60 kHz electrodeless fluorescent lamp for indoor use" IPEC, 2010 Conference Proceedings, vol., pp.682-686, 27-29 Oct. 2010.

[10] IEC 61000-3-2. "Limits for harmonic current emissions – Part 3-4: Limits". International Standards, International Electrotechnical Commission, Ed. 3, 2005.

[11] Jen-Cheng Hsieh; Lin, J.; "Novel single-stage self-oscillating dimmable electronic ballast with high power factor correction" Industrial Electronics, IEEE Transactions on , vol.58, no.1, pp.250-262, Jan. 2011.

[12] Wu, T.-F.; Chen, Y.-K. "A systematic and unified approach to modeling PWM DC/DC converters based on the graft scheme". Industrial Electronics, Control, and Instrumentation. IEEE IECON 22nd International Conference on, vol. 2, pp. 1041-1046, August, 1996.

[13] Xiaojun XU ; Huang, A.Q. "A novel closed loop interleaving strategy of multiphase critical mode boost PFC converters". Applied Power Electronics Conference and Exposition, APEC 2008. Twenty-Third Annual IEEE, Feb., 2008.

[14] Bisogno, F.E.; Seidel, A.R.; Holsbach, R.; Do Prado, R.N.; "Resonant filter applications in electronic ballast". Industry Applications Conference, 2002. 37th IAS vol. 1, pp. 348-354, 2002.

[15] Pok Wai Tam, Stephen T. S. Lee, S. Y. Ron Hui, Henry S. H. Chung.; "Practical evaluation of dimming control methods for electronic ballasts". IEEE Transactions on Power Electronics vol. 21, n. 6, pp. 1769-1775, Nov. 2006.