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A 1.2 V_{pp}, 5.53 µw; 3-Bit Flash Analog to Digital Converter Using Diode Free Adiabatic Logic Threshold Inverter Quantizer

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Abstract: An exclusive Diode Free Adiabatic Logic (DFAL) based Threshold Inverter Quantizer (TIQ) comparator is Suggested in this paper for implementation of a 3-bit flash type analog to digital converter. The suggested work is simulated with TSMC-65nm technology on Cadence® EDA tool. For appropriate implement of DFAL-TIQ, it is requisite to have a suitable reference voltage for each of the comparator and it is done by accurately sizing the transistors of the comparators. The average power dissipated by the suggested flash type ADC when simulated at 100 Hz, $1.2V_{pp}$ and for 1fF capacitive load is 5.53 µw, which is 66.03 % lesser than that of the power dissipated by Flash ADC containing conventional CMOS-TIQ Comparator.

Keywords:DFAL, CMOS, TIQ, ADC.

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I. INTRODUCTION

Crucial helpfulness of an Analog to Digital converter is to transfigure analog information to its compatible digital form. ADCs are frequently incorporated in portable, digitized and devices like digital cameras, mobile-phones, and some of the contemporary biomedical devices like glucometer and ECG monitoring devices etc. The basic steps of signal conversion include quantization and code conversion of the analog input signal applied. ADC architectures are universally characterized as Flash type, Pipelined, Sigma-Delta, Dual Slope, and Successive-Approximation ADC. Out of these categorizations, a Flash ADC is adopted for high speed applications, on the other hand it has high power dissipation issue; which is a vital nervousness to the developers [1-2].

The high speed and mobile devices operated on battery utilizes ADC as an integral part of system, instead of a separate module for data conversion, such arrangement requires least power to be dissipated during working period. There are some commonly used approaches to condense the dissipation of power like, reducing supply voltage and the switching activity of the CMOS circuit; but this is insufficient to meet existing requirements for reduction in power dissipation. Owing to this intention most of the designers have concentrated on adiabatic circuit development to achieve the desired objective.

In the suggested work, it is estimated to design a Flash type ADC by means of Diode Free Adiabatic Logic (DFAL) based Threshold Inverter Quantizer (TIQ) comparator as a substitute for CMOS-TIQ for deduction in power dissipation. The schematic of DFAL is similar to the static CMOS logic; still the circuit operates in adiabatic means; which gives the deduction in power dissipation during circuit operation [3-5].

II. DFAL INVERTER

The salient feature of DFAL topology as presented in Fig 1 is that, it is diode free; there is a slightest probability of presence of any diode in its charging or discharging path. In presented inverter, split-level sinusoidal clock V_P and V_{PC} is used as power supply, and kept 180^0 out of phase. The voltage level of V_P exceeds than that of V_{PC} by a factor of $V_P/2$, this will significantly reduce the voltage difference between the electrodes and subsequently power dissipation is condensed. This split clock charges/discharges the load capacitance quite sluggishly than the other adiabatic power clocks, since the effectiveness of adiabatic logic circuits is concentrated on how leisurely the C_L is charged or discharged?

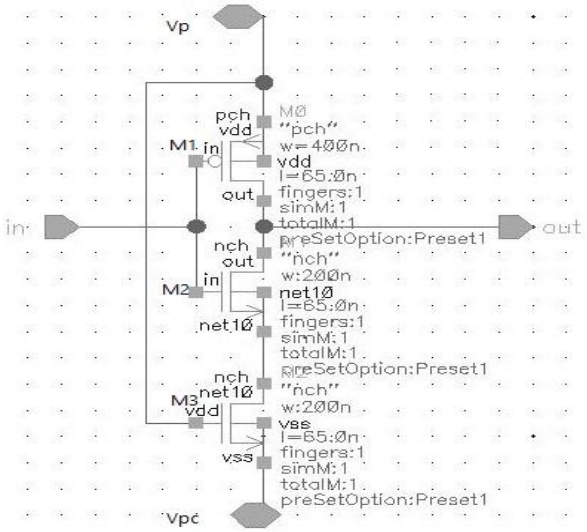

Fig 1. DFAL Inverter Schematic

The circuit arrangement of DFAL inverter is comparable with the CMOS-Inverter; on the other hand, circuit operates in adiabatic means. The transistor M_3 is used as pull-down network next to transistor M_2, which is utilized as diode for the discharge path. Power clock (V_P) pedals the turning ON and OFF of this transistor M_3 [6].

The main root of power dissipation in the adiabatic circuits is the discharging path in the MOS-diodes because, the threshold voltage drop is recognized as non-adiabatic loss; in case of DFAL inverter ON resistance is the reason for the power dissipation recognized as adiabatic loss of MOS transistor M_3 channel of. The power dissipated by this is lower than that of the power dissipated by the threshold voltage drop through diodes. In addition to that, M_3 is also used to recover the charges from the output node; henceforth the adiabatic losses can be recovered. Nevertheless, the losses cannot be completely recovered and power dissipation cannot be completely removed, because of the nonreversible characteristics of DFAL-Inverter. Henceforth by with MOS transistor M_3 the power dissipation is enormously reduced as compared to the CMOS or any other diode based adiabatic inverter. The relationship used in the power clock is mathematically expressed as [6].

$$V_p = \frac{V_{dd}}{4}\sin(\omega t + \theta) + \frac{3}{4}V\,dd \quad (1)$$

$$V_{pc} = \frac{V_{dd}}{4}\sin(\omega t + \theta) + \frac{1}{4}V\,dd \quad (2)$$

The energy dissipated by the DFAL inverter is given as

$$E_{DFAL} = E_{CHARGE} + E_{DISCHARGE} \quad (3)$$

$$= 0.5\,C_L V_{tp}^2 + 0.5\,C_L\,(V_{PC\ P\text{-}P} - V_{tn})\,V_{tn} \quad (4)$$

III. FLASH ADC ARCHITECTURE

All-encompassing architectural view of Flash ADC is as depicted in Fig 2 which principally involves two sections, first the comparator segment and second is the Code Converter segment; if Sample and Hold (S/H) is let off. This style is simple and most suitable for System on Chip (SoC) applications.

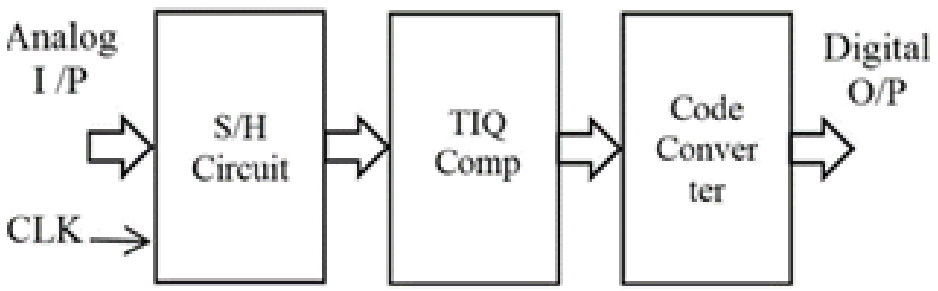

Fig 2. Architecture for Flash ADC

For the work anticipated in this paper; the comparator section comprises of DFAL-TIQ for reduction in amount of power dissipation in comparison with conventional CMOS-TIQ comparator. Output of comparator section is accessible as thermometric code format and is vital to convert it in binary code, to satisfy this requirement a Code Converter Section is employed, at the output digital code is available after conversion [5-7].

DFAL-TIQ COMPARATOR

Most significant segment in the Flash type ADC circuit is the comparator. Various architectures are recommended for accomplishment of flash type ADC comparators like; differential-amplifier latch, auto-zeroed sequentially sampled type, dynamic type, Threshold Inverter Quantizer (TIQ) and Quantum-Voltage (QV). Faster conversion rate is achieved by the TIQ based comparator design. Orthodox CMOS-TIQ comparator is concerned with switching power dissipation; an approach for reducing this in such comparator is proposed by using adiabatic logic, here the Diode Free Adiabatic Logic is used as its elementary factor for effective decrease of the power dissipation. The anticipated comparator for 3-bit Flash type ADC is portrayed in Fig 3 [5-8].

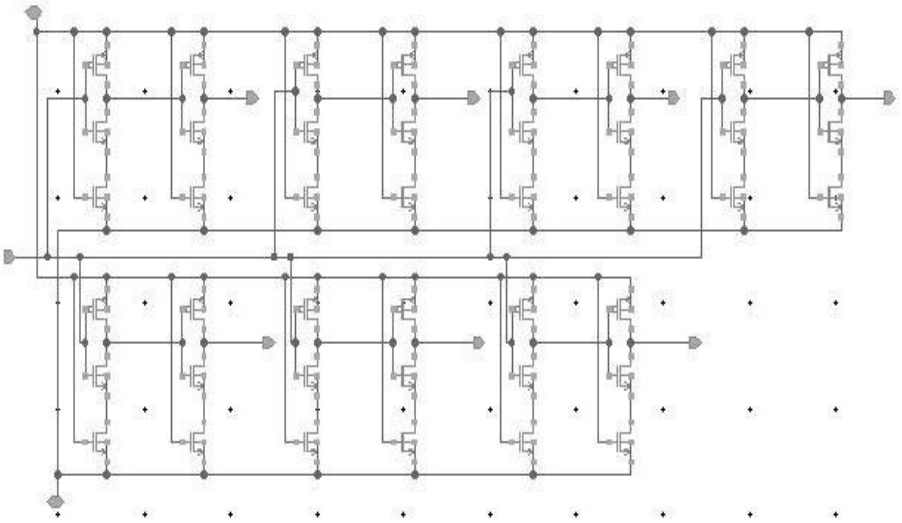

Fig 3 DFAL-TIQ Comparator

In the DFAL-TIQ comparator each of the inverter is comprising of two identical stages; first stage is conditioned to provide the expected threshold voltage level and the second stage is acting as a gain booster stage, which is there to sustain the identical DC threshold level that of the first stage and the other function is to preserve the linearity of DFAL-TIQ comparator.

The anticipated comparator stage for 3-bit flash type ADC, involves seven stages of DFAL-inverter ($2^{\text{no of bit}} - 1 = 2^3 - 1 = 7$) with variable threshold voltage in each inverter. The deviation of the threshold voltage level for DFAL-inverter will guarantee the faithful binary output at each stage, which is accessible in the form of thermometric code. The anticipated DFAL-TIQ is simulated using Cadence-Virtuoso-IC616 with TSMC 65nm technology, the results for the transient sweep analysis and DC sweep analysis are as showed in Fig 4 and Fig 5.

The deviation of the threshold voltages for each stage of DFAL-inverter can be easily witnessed in the Fig 4 and Fig 5. For the transient analysis; the analog input signal having frequency of 100 Hz and 1.2 V_{pp} is applied and for DC sweep analysis the input voltage is diverse in linear steps from 0 V to 1.2 V.

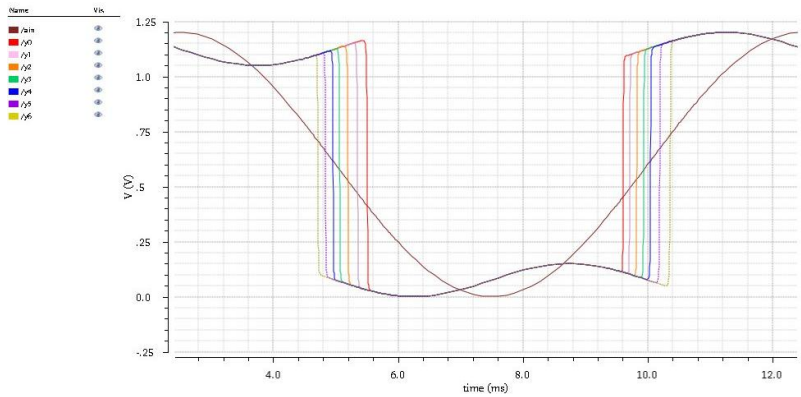

Fig 4. DFAL-TIQ Transient sweep analysis

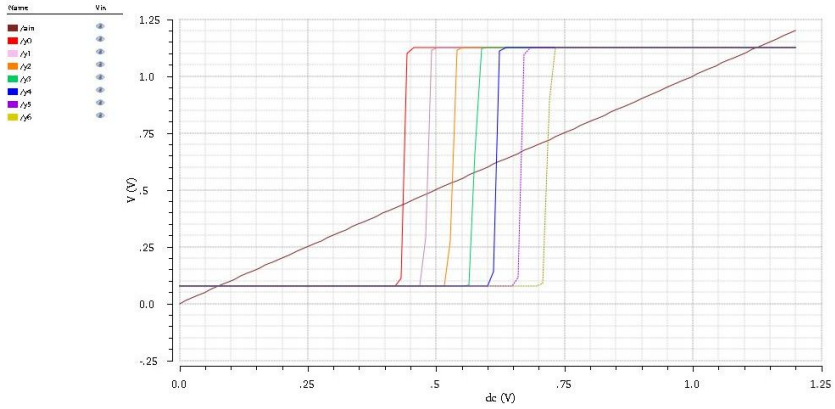

Fig 5. DFAL-TIQ DC sweep analysis.

THE CODE CONVERTER

The output of the DFAL-TIQ comparator is the thermometric code format, to convert this into its equivalent binary code, the Thermometric-to-Binary Code Converter (TM2B) is employed. The unpretentious method to implement Thermometric to Binary code converter is with a binary encoded ROM [9]. Conversely, the converter can also be realized by Wallace tree method as well [11]. In advanced stages of development, Fat-Tree converter was also utilized for the realization of code converter [12].

Method suggested in this work, utilizes a converter realized using 2:1 multiplexer as elementary module, as it has plentiful advantages, such as low circuit complexity and low power dissipation [13]. Schematic level circuit for a 7 to 3 line converter is reported in Fig 6.

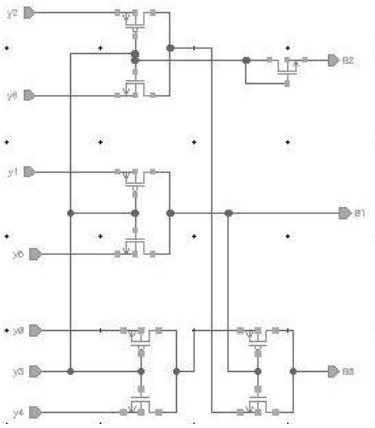

Fig 6. Mux based Thermometric to Binary Code converter

The circuit arrangement of the TM2B converter is done in such a way that it should satisfy all the eight conditions of TABLE I, each row in the TABLE indicates a binding input thermometric-code (the output of comparator stage) and its corresponding 3-bit binary output which will be considered as the output of the Flash ADC.

TABLE I Truth Table for Thermometric to Binary Code Converter

Sr.	Thermometric Code							Binary Code		
No.	Y6	Y5	Y4	Y3	Y2	Y1	Y0	B2	B1	B0
1	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	1	0	0	1
3	0	0	0	0	0	1	1	0	1	0
4	0	0	0	0	1	1	1	0	1	1
5	0	0	0	1	1	1	1	1	0	0
6	0	0	1	1	1	1	1	1	0	1
7	0	1	1	1	1	1	1	1	1	0
8	1	1	1	1	1	1	1	1	1	1

THE FLASH ADC SCHEMATIC

Schematic diagram for proposed Flash ADC is reported in Fig 7, which is a two-stage architecture. First stage contains of the DFAL-TIQ comparator along with the gain booster stage. In the second stage, the code converter is implemented in cascade with the comparator stage to furnish a whole ADC.

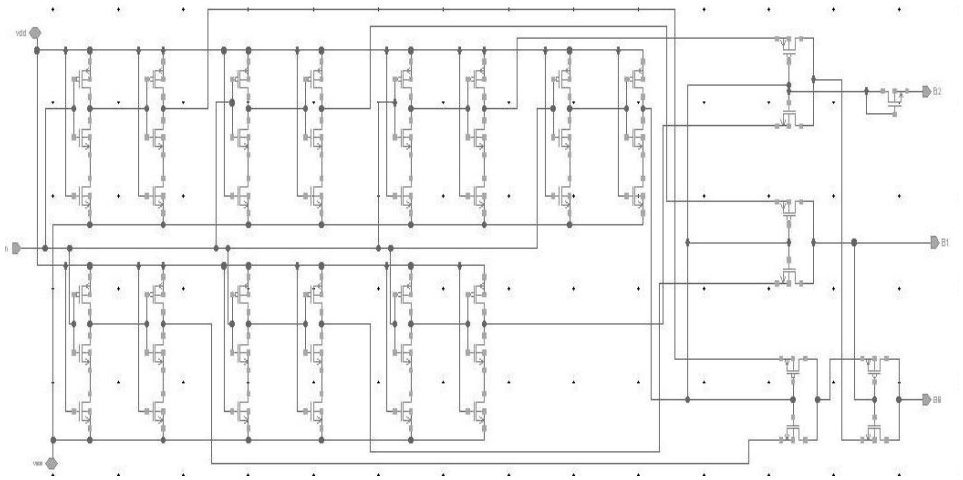

Fig 7. Schematic of DFAL-TIQ comparator based Flash ADC.

IV. SIMULATION RESULTS

The anticipated flash ADC is simulated using Cadence-Virtuoso-IC616 on TSMC 65nm technology, the observed results for the DC sweep analysis and transient sweep analysis are as extracted in Fig 8 and Fig 9 respectively. From these two responses plots, it is illusory that with the variation of the input in linear steps, and binary output bits b2, b1 and b0 are perceived; which in sequence appears as 111, 110, 101, 100, 011, 010, 001, and 000 after a specific time interval. This time interval is decided by the systematic variation of the widths and lengths of the MOS transistors used in the design.

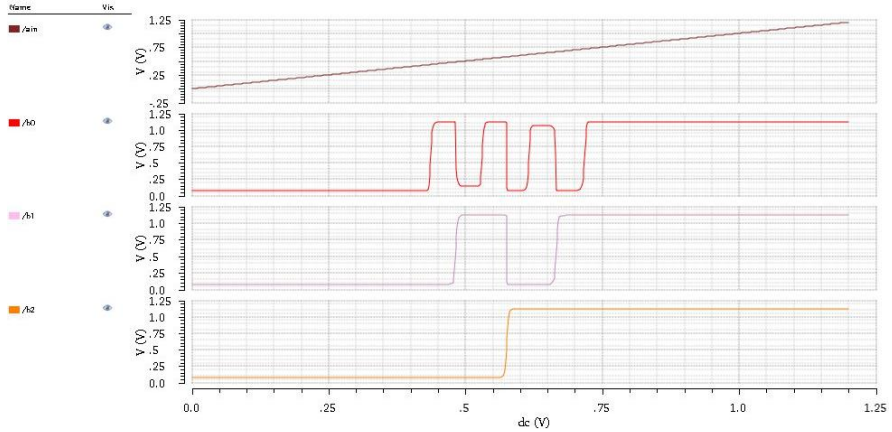

Fig 8. DC sweep response of Flash ADC

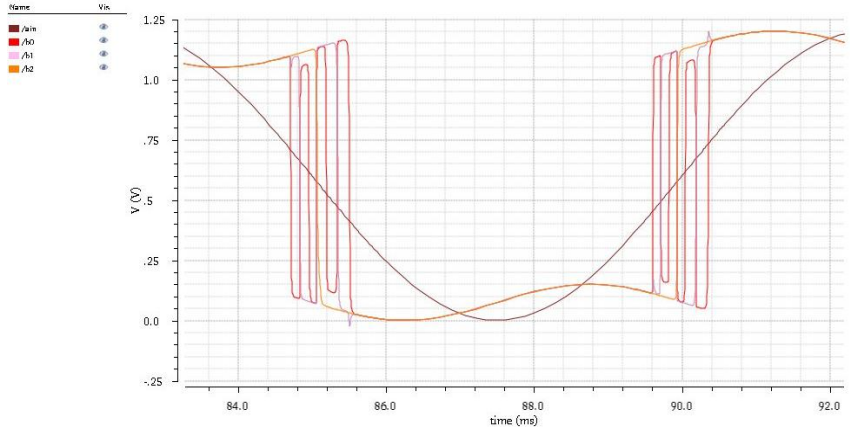

Fig 9. Transient response of Flash ADC

Transient analysis of proposed circuit is carried out at various input frequency signals in order to acquire a relative analysis of power dissipation at 1.2 V at different frequencies is as presented in Fig 10. Static and dynamic parameters for the proposed design were observed; and DNL/INL plots for ADC with proposed DFAL-TIQ comparator are displayed in Fig 11 and the conforming values are : DNL = + 0.56 LSB /-0.61 LSB and INL = +0.40 LSB / -0.43 LSB, respectively.

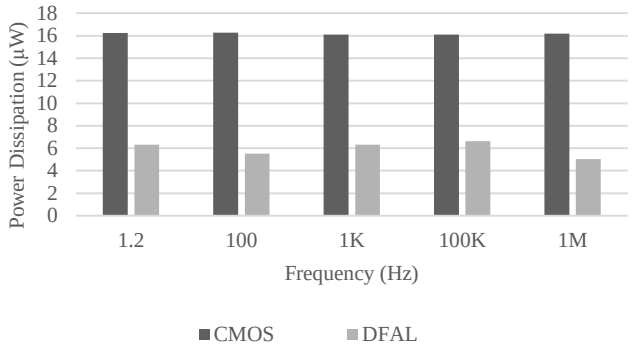

Fig 10. Power dissipation comparison as a function of frequency

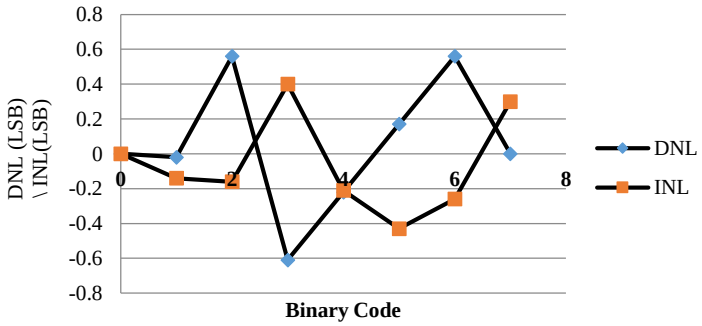

Fig 11. DNL / INL response plot for proposed ADC

To measure the dynamic parameters of the proposed ADC, Fast Fourier Transform (FFT) test is a used and observed results are as THD =-25.25dB, SNR=19.45 dB, SNDR=18.39 dB, ENOB=2.76 bits SFDR = 23.4 dB.

V. CONCLUSION

Diode free adiabatic logic (DFAL) TIQ is a novel adiabatic logic family TIQ for Flash type ADC. The simulation results and relative performance assessment publicized that power dissipation in the DFAL logic family are considerably minimized in comparison with the CMOS family; thus, the suggested DFAL family leave behind the traditional CMOS-TIQ ADC and consumes almost 63 % less energy, and the static parameters observed as: DNL = + 0.56 LSB /-0.61 LSB and INL = +0.40 LSB / -0.43 LSB, respectively.

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