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Design and Simulation of Modified Alum Based On Glut

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Abstract: In today's world where use of semiconductor technology is so wide area occupied by the circuit and delay are main points of concern. Interconnections are known to be main reason of the problem. With the use of multi valued logic (MVL). MVL is preferable our conventional binary logic as it gives optimum speed and better data handling capacity. In this paper we propose an ALU which is based on Quaternary logic look up table. Designed ALU is compatible with Standard CMOS technology. The Schematics are designed in S spice and simulation is done in T spice of the Tanner software.

Keywords: Multi valued logic (MVL), Arithmetic logic unit (ALU), Quaternary logic look up table, Tanner.

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I. INTRODUCTION

ALU is important part of any processor. In this paper we propose a modified ALU which is based on Quaternary lookup table. MVL systems lead to saving in the number of interconnections. Due to the availability of the additional logic levels, the wires convey more information. It ultimately reduces the number of devices and leads to saving of area. Because of the use of quaternary lookup table instead of binary lookup table the power consumption and delay are reduced in this design. The transistor count is also reduced thereby reducing the area required. This design is compatible with standard CMOS. ALU is designed by mapping binary LUT into quaternary LUT with integrated circuits. Proposed ALU is implemented in Multiple-Valued voltage Mode Logic. The operands are converted to binary using a QtoB converter operations are performed in binary and results are converted to quaternary by using BtoQ decoder. This paper is organized as follows. In section II modules used to design the ALU are discussed in section III operator modules are with their simulation. In Section IV results and conclusion are given.

MODULES USED:

A. Down literal circuit (DLC):

The down literal circuit (DLC) divides a multiple valued signal into a binary signal at an arbitrary threshold value. DLC consists variable threshold voltage values by way of controlling only two bias voltages. Therefore, DLC is very useful circuit element in quaternary logic or any multiple value logic system.

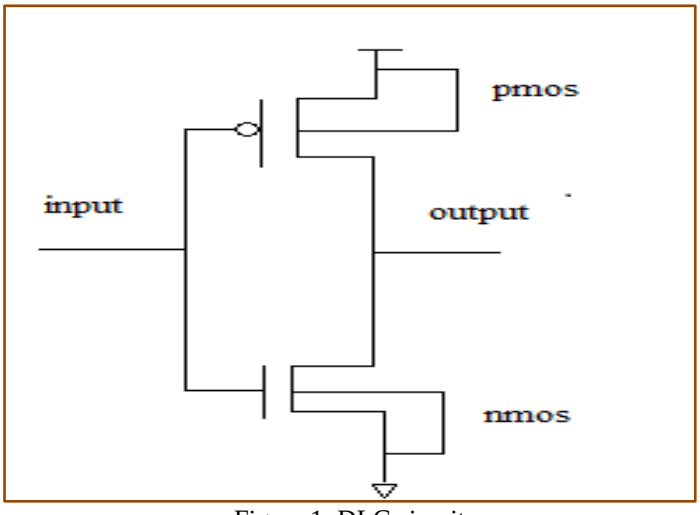


Figure 1: DLC circuit

A. Quaternary lookup table:

A quaternary logic lookup table with clock boosting technology proposed in paper [9] is used in the design of this ALU. Look-up tables (LUT) are digital blocks which can store data depending on function implemented. Multiplexer is basic element of look-up table. Number of input processed in LUT and radix of number system are responsible for type of multiplexer used. When an n-bit LUT is designed with select lines of multiplexer as input lines the capacity of LUT is given by

$C=n \times b^k$ (1)

Where |C|: capacity n: outputs, k: inputs and b: logic values for a function.

The total functions implemented in an LUT with k input are given by

$F = b^{|C|}$ (2)

Where $C= n \times b^k$ from equation (1) and b: logic values for a function.

From equation (1) & (2) it is clear that using a quaternary LUT in place of a binary LUT is beneficial.

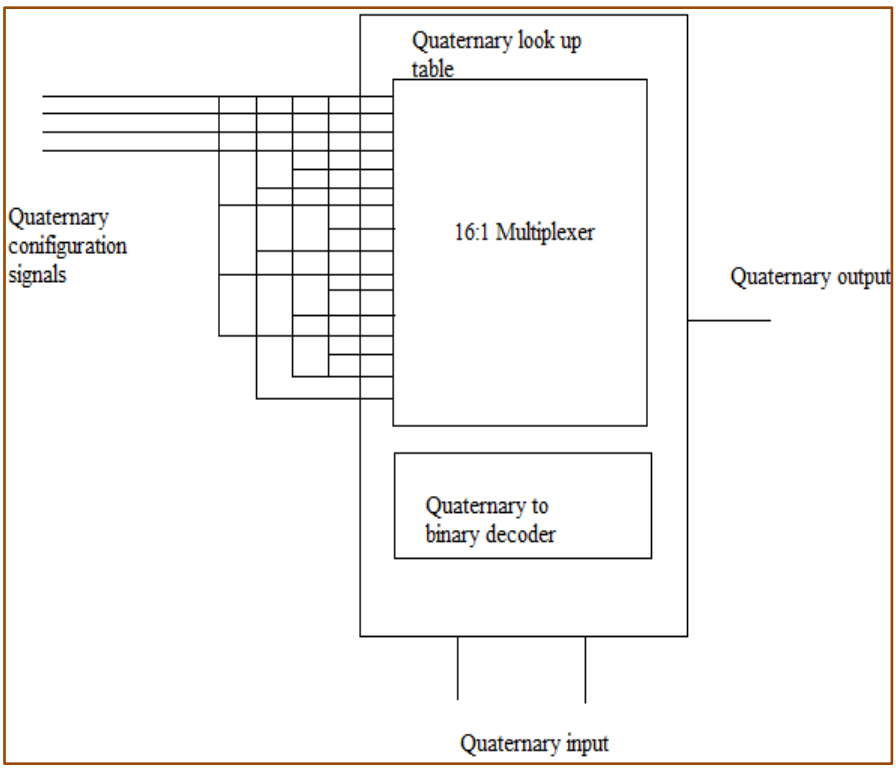


Figure 2: Quaternary Look up table

The main reason of selecting of a multiplexer as main block in LUT is that it can also be used as adder, subtractor or any arithmetic operation in the ALU along with the LUT.

B. Quaternary to binary (Q to B) decoder

As we know a 16:1 multiplexer will have 16 inputs lines one output and four select line in a binary system but because of the use of quaternary to binary decoder the select lines are reduced to two. . It fetches quaternary input and converts it into binary to perform regular operations of the designed system. 16 control signals are generated which are applied to clock input of each switch. The switches connect input to the output. For generation of required control signals the quaternary configuration variables are converted into binary so as to use binary logic gates.

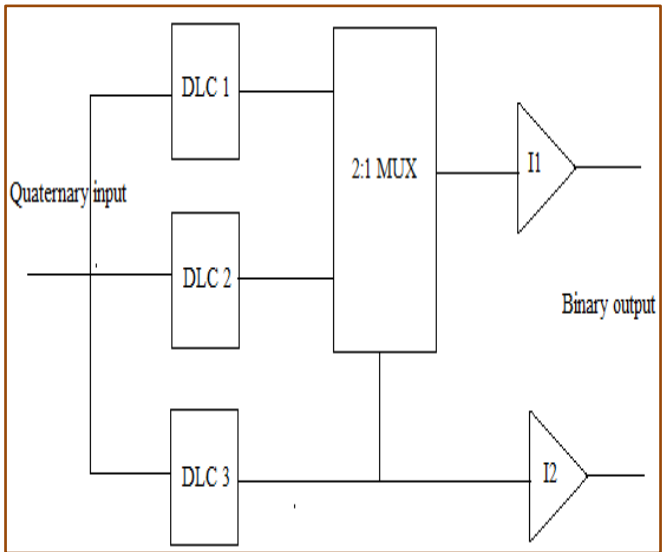
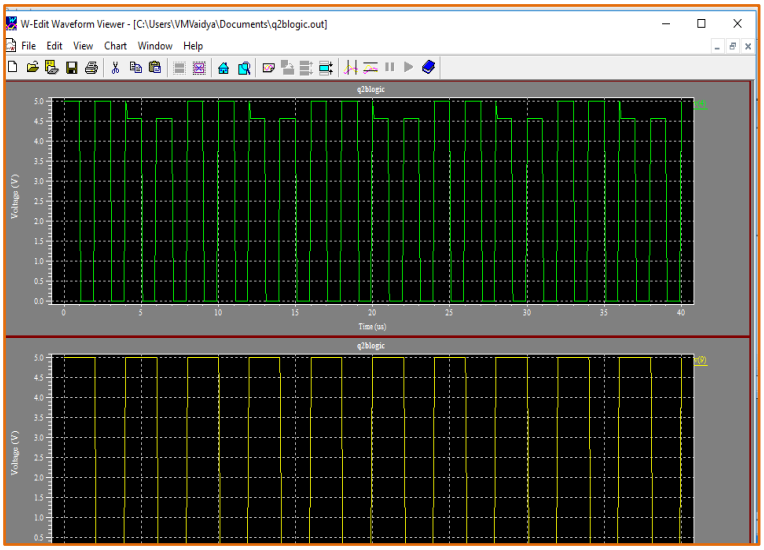


Figure 3: Block diagram of quaternary to binary converter



Simulation 1: Quaternary to binary converter

C. Binary to quaternary converter

It is used at the output side. All the internal operations are done in binary hence at the output side a binary to quaternary decoder is required.

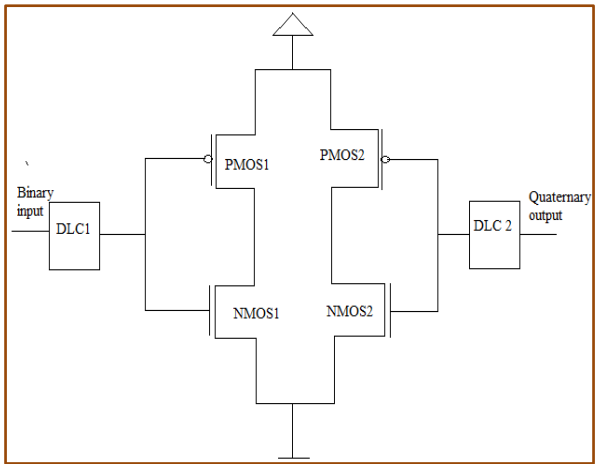
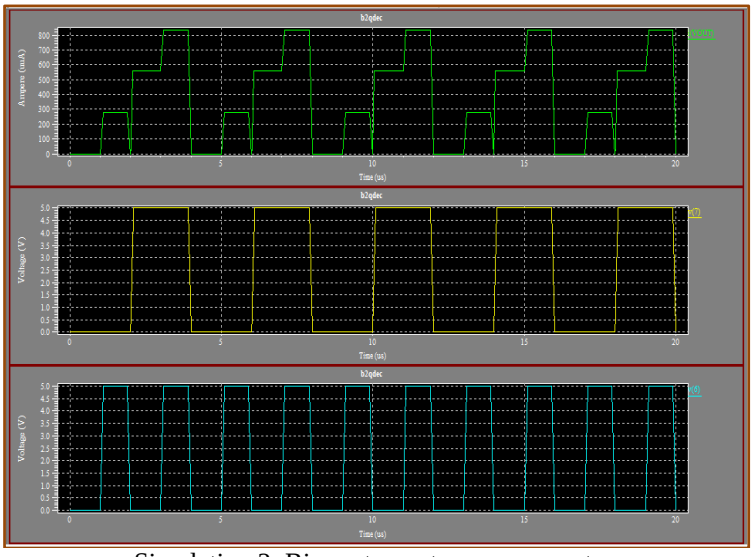


Figure 4: Block diagram of binary to quaternary converter



Simulation 2: Binary to quaternary converter

II. MODULES DESIGNED

A. Full Adder

Addition table for quaternary addition is given bellow:

+	0	1	2	3
0	0	1	2	3
1	1	2	3	10
2	2	3	10	11
3	3	10	11	12

Table 1: Addition with quaternary operands

When these operands are converted in binary by QtoB converter they are represented as binary no system as 00, 01, 10, and 11. The addition table can be represented as

+	00	01	10	11
00	0	1	2	3
01	1	2	3	0
10	2	3	0	1
11	3	0	1	2

Table 2: Addition with binary operands

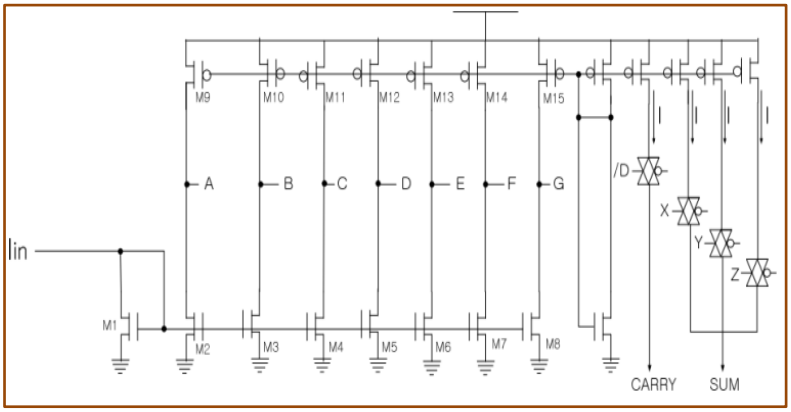
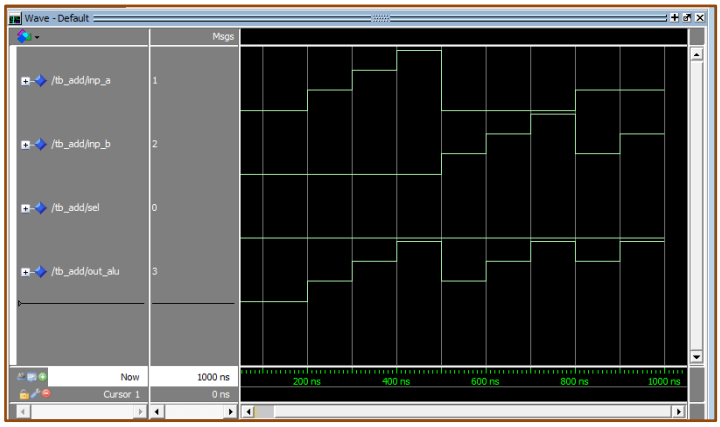


Figure 5: Schematic of full adder



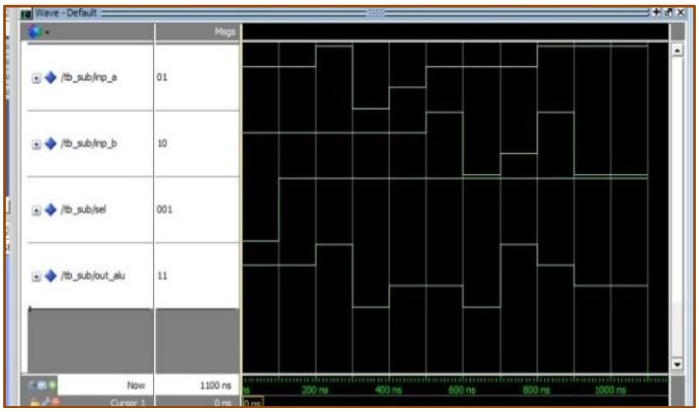
Simulation 3: Full Adder

B. Subtraction unit

Table for quaternary subtraction is given below:

-	0	1	2	3
0	0	3	2	1
1	1	0	3	2
2	2	1	0	3
3	3	2	1	0

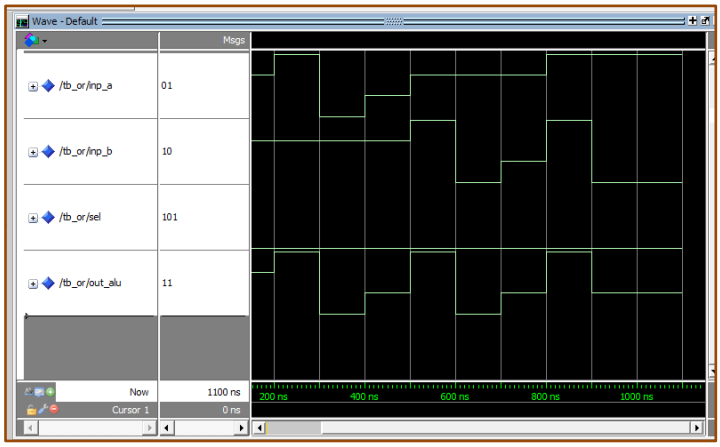
Table 3: Subtraction



Simulation 4: subtraction unit

C. AND & OR units

Simulation 5: AND operation



Simulation 6: OR operation

III. RESULTS

The simulation results of Q to B and B to Q converters are shown in simulation 1 & 2 respectively. Simulation 3 & 4 show simulation results of arithmetic operators addition and subtraction. Simulation 5 & 6 show results of logical AND & logical OR respectively. Power voltage and transistor count of each circuit is given in following table.

Module	Power	Voltage	Transistor Count
Full Adder	8.25µW	3V	94
Subtraction unit	1.08µW	3V	22
AND	2.1 µW	3V	18
OR	0.4 µW	3V	18

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