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A Survey and Comparative Study of Normal Gate and Reversible Gate Implementation of Digital Multiplier based on Ancient Indian Mathematics

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Abstract: Ancient Indian Vedic Mathematics (AIVM) is collection of sutras (formula), decoded and rediscovered by Jagatguru Swami Sri Bharti Krisna Tirathji Maharaj. These sutra are applicable to each field of mathematics and also valid for any number system. Practice of Vedic mathematics is known as mental mathematics because one can easily compute large calculation without any paper pencil. This property of VM attracts system designer, engineers and researchers to implement these sutra into computer hardware. Multiplication is one of the most important operations in various fields. This survey will explore various design technique and compare them.

Keywords: Vedic Mathematics, Digital Multipliers, Reversible Gate, FPGA

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I. Introduction

Vedas are ancient collection of hymns written in India. Tough mathematical problem can be easily solved with the help of Vedic Sutras (Mathematical aphorisms) contains in the parisista (the Appendix-portion) of the **Atharvaveda** in few simple steps. The Sutras apply to and cover each and every branch of mathematics [1], even **in Binary numbers also.** These sutras are rediscovered by Jagatguru Swami Sri Bharti Krisna Tirathji Maharaj early twentieth century. As we know that multiplication is one of most important task performed by computer systems which involve in image processing, DSP, FFT, cryptographic applications, embedded systems etc. Booth multiplication and array multiplication algorithms are most common algorithms which is implemented in most Processors and coprocessors [2]. Booth and array multipliers are not very efficient in terms of power and execution time (speed) and implementation area requirement when we compare it with Vedic mathematics based multipliers are efficient in terms of execution time (speed), power and area[3]. In this paper, we reviewed various papers that Implement multiplier with normal gate and reversible gate.

II. Fundamentals: Vedic Mathematical Architecture and Reversible Gate

Vedic multiplication: Urdhva-Triyakyabhyam i.e. vertically and crosswise, sutra was most commonly used by majority of researchers. Other then UT there 15 more mathematical sutra are available in Ancient Indian Vedic Mathematic (AIVM), so there are total 16 sutras.

Let's Assume A1A0 and B1B0 are two digit binary numbers and M3M2M1M0 is result of their multiplication,

```
   A1A0
   B1B0
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M3M2M1M0
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so as per Vedic mathematics formula M(3 -0) can be calculated in following manner

M(0) = A0.B0 // AND operation between A0, B0; Please observe that it is vertical multiplication(Urdhva)
M(1) = A1B0 XOR A0B1// It is cross multiplication (Triyakyabhyam)
M(2) = (A1B0 AND A0B1) XOR A1B1// it is cross and vertical opration

M(3) = A1B1 AND (A1B0 AND A0B1)

We know that the half adder produces a sum and a carry value which are both binary digits.
S = A xor B
C = A and B
If we closely observe Vadic method then we can conlude following :-
M(0) is Simple multiplication of vertical digits (A0.B0)
M(1) is sum of two cross multiplication products i.e. (A1B0), (A0B1)
M(2) is sum of carry generated in calculation of M(1) and vertical product A1B1
M (3) is nothing but carry generated in calculation of M(2), if any

So from above discussion it is clear that 2x2 multiplier can be implemented in many ways.

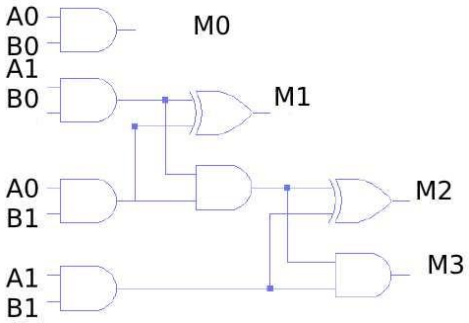

Figure 1 2x2 Vedic Multiplier

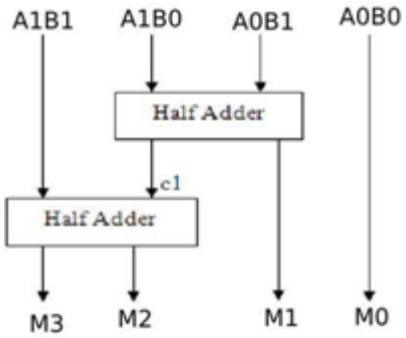

Figure 2 2x2 Conventional Vedic Multiplier

Figure 1 and Figure 2 represent 2x2 vedic multiplier which is implemented by many researchers, this 2x2 multiplier will become base architecture for higher order multiplier, one can easily implement 4x4 multiplier with four 2x2 multiplier and with adders, this design can be extended to 8x8, 16x16, 32x32, 64x64 and so on.

Reversible Gate: In irreversible hardware realization minimum KTln2 joules of energy will be dissipates with loss of one bit of information, here K= Boltzmann's constant and T = absolute temperature[5].In 1973, to avoid such power dissipation , Bennet suggested and showed that circuit must be implemented by using reversible logic gate[6].

Reversible Logic Gate

A Circuit/Gate will be called reversible if it can generate unique outputs from inputs and vice versa there is one to one mapping of input and output. Number of output and number of input in reversible circuit is equal, NOT gate is also an example of reversible gate. For N input reversible gate must have N output [7-10]. Input vector must be derived from its output vector [4].

Constant Inputs is input which is maintained at logic '1' or ,0, for implementing logical function[11]. **Garbage Output** is output added to given function to make in reversible [4].

If any function **have I = Number of Input**, **O = Number of Output**, and **I** is not equal to **O**. So to make this function as reversible we have to add some Constant Input and garbage output in a such way that after in Number of Input should be equal to number of output.
IF
Constant Inputs = C
Garbage Outputs = G
I + **C = O + G [**4]
Feynman Gate FG [12-13**]**
If A, B are inputs and P, Q are outputs then output function of Fenyman Gate is
P = A
Q = A XOR B
Output function of fenyman gate is directly implemented in VHDL/Verilog. It is also known as CNOT gate.
There are some other reversible gate which is implemented in VHDL are Fredkin gate, Taffoli gate, Peres gate, TR gate, DPG gate, DKG gate[7].

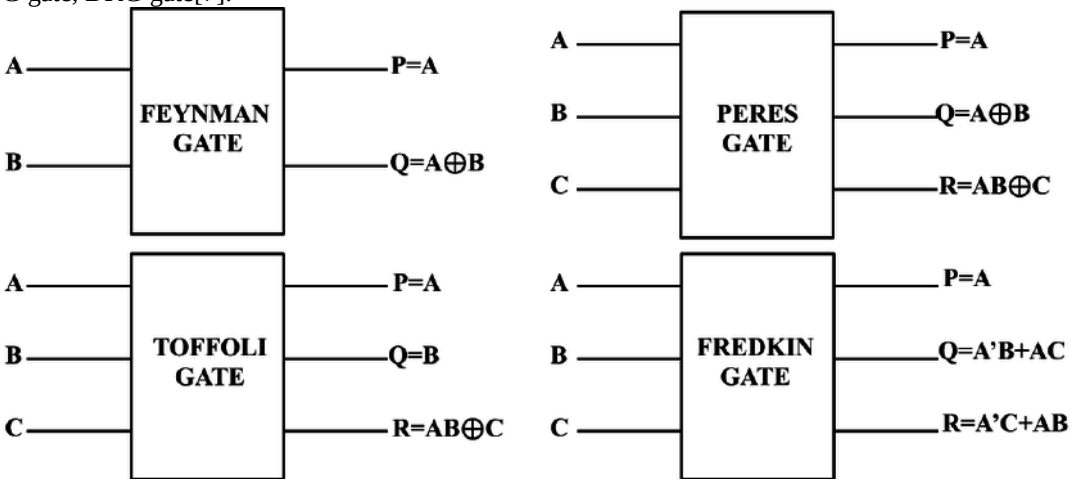

Figure 3 [14] Basic Reversible Gate

III. Trends and Development of AIVM based Multipliers

Normal Gate Implementation:- In [15], Tiwari et al study and implement two sutra **(UT and Nikhilam**) , they implement it for 2,3,4,8 bits and compare it with conventional multiplier. They compare not only in terms of delay but also in number of multiplication and addition required. They use CLA adder, it will make the addition process and carry generation faster. They implement it on XILINX:SPARTAN:S30VQ100:-4 and found that multiplier based on VM is faster than array and booth.
Sharma et al [16], in this paper they studty **Urdhva**-Triyakyabhyam sutra of AIVM and develop 2 bit multiplier for multiplication of quadratic equation whole design is simulated in cadence virtuoso on 180nm process. This paper is basically implementation of AICM in CMOS logic design. They reported that power consumption of their design is 6.44mV and claim that it is very low; however this paper is silent on delay.
In [17] Anjana et al, they study **Urdhva-Triyakyabhyam** sutra of AIVM and propose Floating-point Multipliers, They implement 24x24 multiplier for FPM using two different adders (RCA and CLA) and compare it with other design in which uses array multiplier. They also use partial reconfiguration feature, which was introduce by Xilinx in late 1990,s. Their result shows that AIVM based multiplier with CLA give better result in terms of delay, however in terms of On-chip Total Power (W) AIVM based multiplier and array multiplier both are on the same boat.
Jaina et al [18] study the **Urdhva-Triyakyabhyam** sutra of AIVM and implement 4x4, 8x8 and 16x16 multiplier. As we know that AIVM based multiplier needs adders, in this paper author use carry save adder. They also implement 8 bit, 16 bit and 32 bit MAC. MAC is circuit which adds the result of multiplication with special register (accumulator). They compare their AIVM based multiplier with modified Booth Wallace Multiplier.
In [19] Authors study the **Yavadunam'** sutra of AIVM and implement Squaring circuit for 8 bit to 64 bit operations and compare it in terms of delay with Booth multiplication with two other implementation of Squaring circuit. **Barik et al consider the deficit case of Yavadunam sutra of Vedic mathematics where the number is**

less than the base They found that their implementation based on AIVM give better result. They implement their design by using Xilinx ISE 10.1 software on 4vlx15sf363-12 device.
In [20] Akhalesh et al study the **Urdhva Triyakyabhyam** sutra of AIVM and design DSP operation (liner convolution, circular convolution and correlation) in MATLAB, they compare it with inbuilt MATLAB function and found that AIVM based operation gives better result.
Sethi et al [21] implement **Yavadunam** sutra of AIVM for implementing squaring circuit for 4 bit, 8 bit, 16, bit, 32 bit and 64 bit; compare it with modified Booth's algorithm and squaring circuit using Vedic multipliers reported by Kasliwal et al. (2011). They found that their implementation give much better result. They implement their design in Vertex4vlx15sf363-12 device.
In [22] Kasliwal et al implement **Urdhva-Triyakyabhyam** sutra of AIVM for designing of digital multiplier, they design and simulate 4 bit, 8 bit and 16 bit multiplier and compare it with Booth's multiplier. Design was implemented in Xilinx Virtex 4vlx15sf363-12 device.

Reversible Gate Implementation:- In [4] Sakode et al, design 4 bit and 8 bit multiplier, they design 4x4 bit multiplier with help of full adder and Peres gate and use this design for making 8x8 bit multiplier, for it they use **Urdhva-Triyakyabhyam** sutra of AIVM, they also use 8 bit reversible adder. Whole design was implemented in SPARTAN 3 XC3S50 device.
In [23] Gowthami et al develop 2x2 bit multiplier based on **urdhva-Triyakyabhyam** sutra of AIVM, after that they implement 4x4 multiplier in which 2x2 multiplier is base multiplier. For adder circuit they use HNG gate for implementing reversible Ripple Carry Adder and Peres gate as half adder. They also implement 8x8 and 16x16 multiplier. This paper report Constant input, Garbage Output and Quantum cost but silent over delay issue. For simulation they use Xilinx 14.3 ISE.
Giridhari et al [24] , they study **Urdhva-Triyakyabhyam** sutra of AIVM and implement 8x8 multiplier, in which 4x4 multiplier is used as base component and use reversible ripple carry adder. The compare normal and Vedic multiplication in term of number of addition and multiplication. This paper explains steps of methodology (reversible Adder circuit with no input carry in detail. Vertex XC4VLX15 device is used for implementation. However this paper does not provide any numerical value for Garbage Out, Quantum Cost etc.
Shivarathnamma et al [25], Implement 4x4 bit multiplier based on **Urdhva-Triykyabhyam** sutra of AIVM, for implementing 4x4, they design 2x2 reversible multiplier which consist of Taffile Gate, BME gate and three Peres gate thus total five reversible gate were used. HNG gate were used for developing reversible Ripple carry adder unit.
In[26] Himangi et al, implement 8x8 digital multiplier based on **Nikhilam** sutra of AIVM, their 4x4 multiplier consist HNG gate and PG gate. They did not specify that the adder circuit is reversible or not.
In [27] Srikanth G et al, Design The 32x32 bit vedic multiplier based on **Urdhva-Triyakyabhyam** sutra of AVIM their design includes reversible logic gates like Feynman gate, Peres gate, HNG gates and four 16x16 bit vedic multipliers.

IV. Discussion

Table 1 is summary of reviewed paper, in which digital multiplier design based on AIVM is implemented by normal gates. From table 1 it is clear that **Urdhva-Triyakbhyam** sutra was most preferable sutra of AIVM for all purpose multiplication. However Yavadunam and Nikhilam sutra is better choice for special purpose circuit such as squiring circuit.

In both sutras Adder plays major role in determining the speed of circuit, so one can find tread off between area and speed by selection of appropriate adder circuit.

Table 2 is finding of survey of digital multiplier implemented using reversible gate. In this implementation **Urdhva-Triyakbhyam** sutra was again preferable choice of scholars. Main motivation behind reversible logic gate implementation is that, it will reduce the power dissipation and also provide immunity against DPA.

Table 1 : Findings of Survey (Normal Gate Implementation)

scholar	Delay in (ns)	Remark	References
Tiwari et al	27 ns (Wrost Case) **@ 37 MH OP Frequency**	8 bit Multiplier, CLA Adder is used ; XILINX: SPARTAN: S30VQ100: -4 is used Compared with Array and Booth; DELAY 43, 124, 12 of Array Booth and VM respectively; UT and Nikhilam Sutra of AIVM	[15]
Sharma et al	NA	2 bit Multiplier;COMOS Logic Design;6.44mV Power Consumption; UT Sutra of AIVM	[16]
Anjana et al	VM(CLA) 31.832, VM (RCA) 33.246 Array Multiplier 56.481	24x24 Multiplier; Use Partial Reconfiguration feature of Xilinx; UT sutra of AIVM	[17]
Jaina et al	36.09	16x16 Multiplier; Carry Save Adder is used; SPARTAN3 XC3S50 -4;UT Sutra of AIVM	[18]
Barik et al	10.95 (8 bit) 11.176 (16 bit) 17.322 (32 bit) 21.76 (64 bit)	Vertex-4 FPGA device 4vlx15sf363-12;deficit case of Yavadunam sutra; Yavadunam sutra of AIVM	[19]
Akhalesh et al	NA	MATLAB; UT Sutra of AIVM	[20]
Sethi et al	4.993 (4 bit) 8.948 (8 bit) 18.564 (16 bit) 37.345 (32 bit) 75.236(64 bit)	Vertex4vlx15sf363-12 device; Yavadunam sutra of AIVM	[21]
Kasliwal et al	4.993 (4 bit) 14.256 (8 bit) 33.391 (16 bit)	Xilinx Virtex 4vlx15sf363-12, UT Sutra of AIVM	[22]

Table 2:- Findings of Survey (Reversible Gate Implementation)

Scholar	Delay in (ns)	Gout and QC	Remark	References
Sakode et al	13.65 (4X4) 29.23 (8X8)	20, 80 (4 bit)	Peres gate; SPARTAN 3 XC3S50 device; UT sutra of AIVM	[4]
Gowthami et al	NA NA	198, 628 (8 bit) 866, 2740 (16 bit)	HNG gate for RCA; Peres Gate as Half Adder;UT Sutra of AIVM	[23]
Giridhari et al	NA	NA	reversible ripple carry adder; Virtex XC4VLX15; UT Sutra of AIVM	[24]
Shivarathnamma et al	NA	60,166 (4 bit)	BME,TG and Peres gate for 2x2 multiplier;HNG gate for RCA;UT Sutra of AIVM	[25]
Hemangi et al	8.73	NA	Nikhilam sutra of AIVM	[26]
Srikanth G et al	99.827 (32 bit)	NA	UT sutra of AIVM	[27]

V. Conclusion

This paper will help to researchers in understanding of various development stages of implementation of digital Vedic multipliers based on AIVM. Hope this paper will help in high speed, low area and low power design of digital multiplier. There is still a lots of work remain which will improve the performance of digital multipliers.

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