IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
Vol. 09, Issue 1 (January. 2019), ||V (I) || PP 15-19

Performance Evaluation of High Speed Multipliers

[1]Rmesh Babu Badite [2]P D S S S Siva Durga[3]sunitha Kallu*ri*
[1]Assistant Professor, Sri Mittapalli College of Engineering, Guntur, AP, India
[2]Assistant Professor, Sri Mittapalli College of Engineering, Guntur, AP, India
[3]Assistant Professor, Sri Mittapalli College of Engineering, Guntur, AP, India
Corresponding Author: Rmesh Babu Badite

Abstract- Day to day life technology was gradually increased portable devises were played significant role in the digital market. Most of digital circuits required less area, speed and power consumption .In multipliers required clock signals because the multipliers are complex circuits, to overcome this drawback the proposed structure satisfying the performance of circuit. In this paper two different multipliers are designed those are modified Wallace multiplier and array multiplier with the combination of truncated multiplier. The comparison is carried out by using EDA tool i.e.to developed this paper in Xilinx ISE 12.3 design suit for synthesis and simulation.

KEY WORDS: Truncated multiplier, Array multiplier, Modified Wallace multiplier, Multiplexer.

Date of Submission: 18-12-2018 Date of acceptance: 03-01-2019

I. INTRODUCTION

The problem with multipliers is, they are very costly and poor in overall performance. The performance speed of multiplier influences a computational problem. Assume that we consider two unsigned binary numbers as X and Y with respective bit lengths of M and N. it is very useful to represent X and Y in binary notation for performing multiplication operation for them.

$$X = \Sigma\, Xi\ 2^i \quad i = 0 \text{ to } M$$
$$Y = \Sigma\, Yj\ 2^j \quad j = 0 \text{ to } N$$

$$\begin{aligned} Z = X \times Y &= \Sigma\, Z_k 2^k \quad k = 0 \text{ to } M + N - 1 \\ &= (\Sigma\, Xi\ 2^i \ i = 0 \text{ to } M)\,(\Sigma\, Yj\ 2^j \ j = 0 \text{ to } N) \\ &= \Sigma\,(\Sigma\, X^i\, Y^j\, 2^{i+j})\ i = 0 \text{ to } M\text{-}1,\ j = 0 \text{ to } N\text{-}1 \end{aligned}$$

In multiplication operation was done in two numbers one was multiplicand and another was multiplier .If multiplicand had M bit and MULTIPLIER had N number of bit ,then the output of multiplier had M*N number of bits. This multiplication having two steps one is the first step was generating partial products, which are produced by and the multiplier and multiplicand are operated on and operation. All the corresponding bits ,and shifted to the left to the every corresponding partial product until all bits were done in the multiplier and multiplicand .And the second step was adding the each column of the partial products. which is a copy of multiplier or a 'zero' because the values are a1 or 0 in the binary number system.

By implementing a new method, comparable to the manual computing method, multiplication maybe a bit faster using the technique. The example of multiplication shown in below in this all the partial product were generated same instant of time and it took less time to generate.

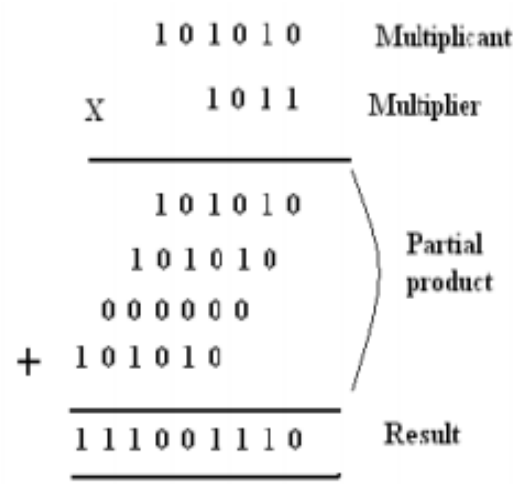


Fig: 1 example of manual multiplication

II. MULTIPLIER ARCHITECTURES:

Array multiplier was the one of the multiplier for multiplying the two binary numbers, those are multiplier and multiplicand. The below figure represent array multiplier architecture it multiplies two binary numbers ,if each number contains m and n bits of size then output will be the m*n number of bits. In this multiplier having two stages one for calculating the partial products another one was the sum of partial products. And using the number of adder to done the addition are n-1*m. The efficient layout of the partial products adding structure is same as a rectangle.

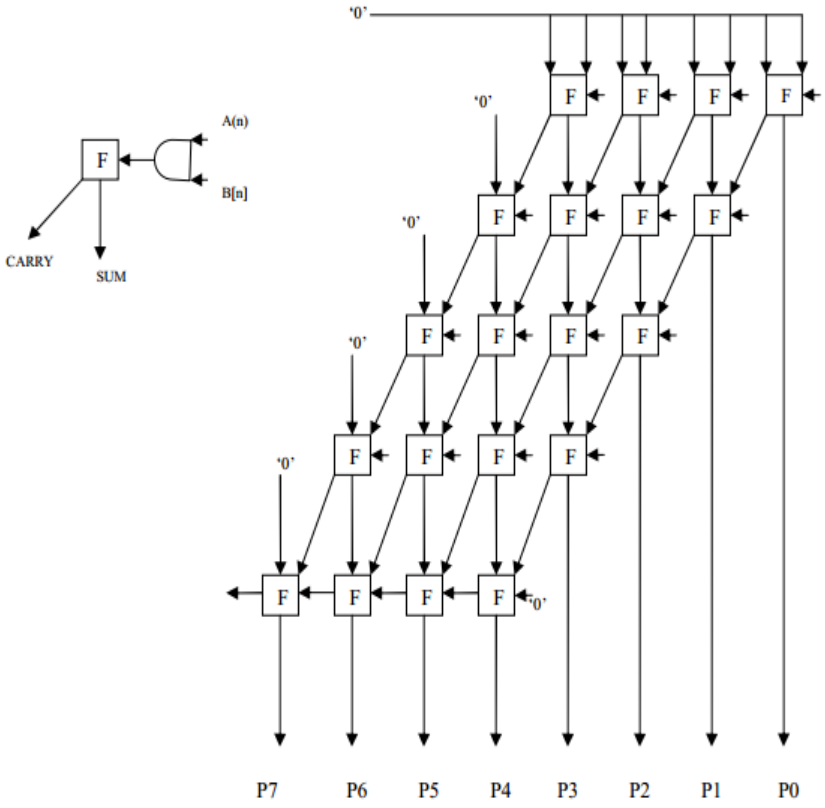


Fig: 2 Array Multiplier Architecture

The truncated multiplier technique is shown in the fig 3, by reducing the usage it consumed less area because of partial products of least significant bits were removed from least significant columns. In this multiplier least significant bits were always zero, T was the degree of the truncated multiplier. This multiplier also having a few steps one is to find the partial products and second one was the eliminating the significant bits and rounding finally.

The process of deleting was the first step the degree of truncating is generally 50% of the size of the product .The process of truncating is defined as the process of deleting the large number of partial products. All the least significant bits were replaced by zeros in this multiplier. In this multiplier all the significant bits were formed a matrix and most of the least significant bits is equal to zero and remaining most significant were added.

In any multiplication if the multiplier and multiplicand can having n,and m number bits simultaneously then the output will be in the number bits in m*n. Coming to the truncated multiplier gave the best results to traditional multiplier .And it occupied lesser area. The truncated multiplier consumed less power compared to the conventional multiplier and the speed of execution was high. The truncated multipliers were used in fir filters , digital signaling process and etc. It used less memory.

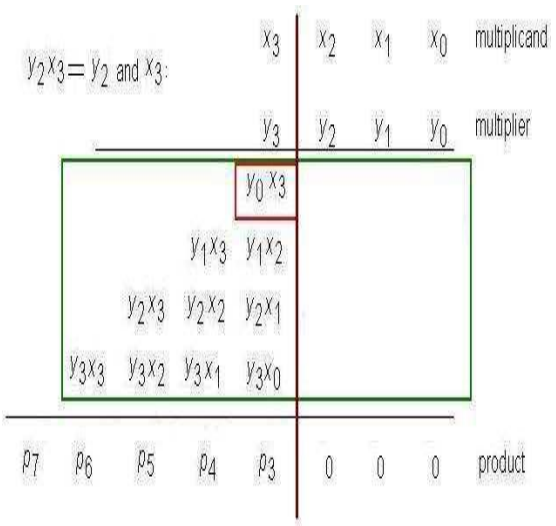


Fig: 3 4x4 bit Binary Multiplication with truncation

The Wallace multiplier is shown in figure 4. The multiplier design uses efficient hardware for multiplying two binary values. Wallace multiplier uses mare half adders and full adders when compared to the conventional multiplier. Hence it is necessary to modify the design implemented. The modified multiplier greatly reduces the hardware requirements and reduces the complexity. The Wallace multiplier design firstly generates the partial product and arranges them in the shift rows. Then it took three rows together and reduces them to two rows, the reduction simultaneously performs for every three rows. Thus produced two rows are splits with the remaining rows and form three again.

$$r_{i+1} = 2[r_i/3] + r_i \bmod 3$$

$$\text{If } r_i \bmod 3 = 0, \text{ then } r_{i+1} = 2r_i/3$$

The overall design gets two final rows. These two rows are then given to a ripple carry adder to perform addition between them. Thus produced final result will be the product of the two binary numbers.

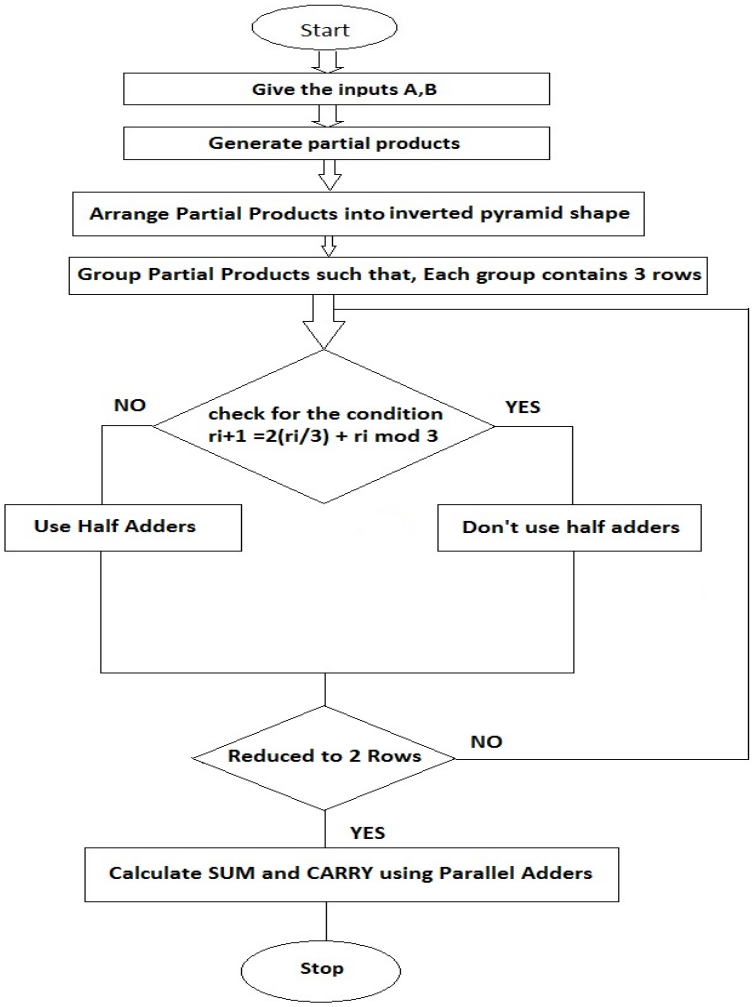
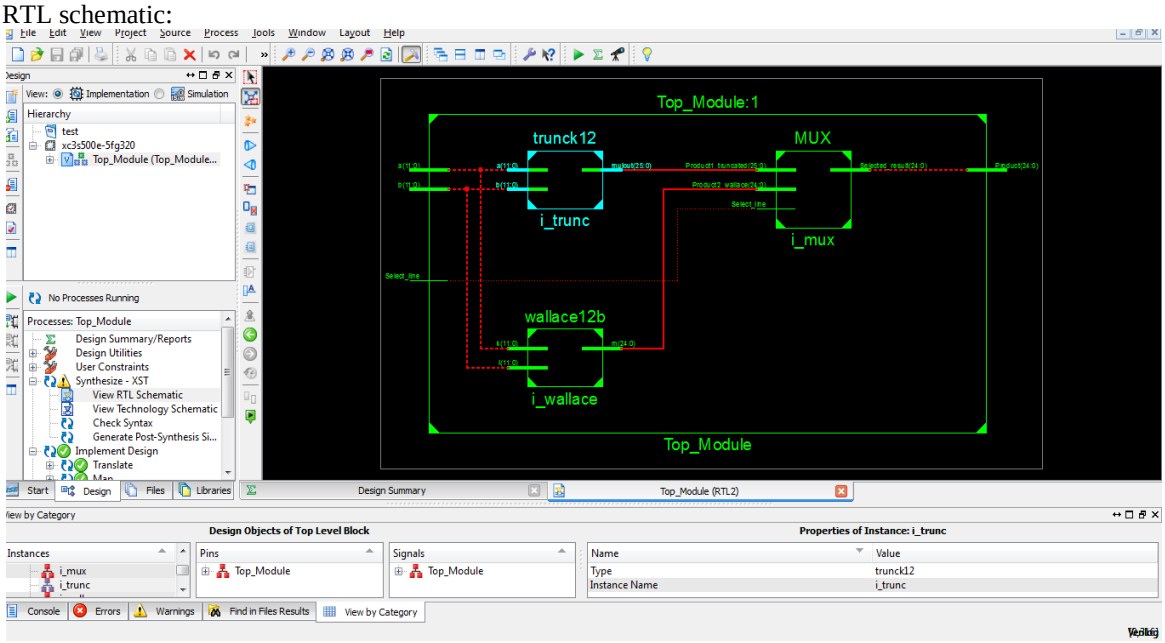


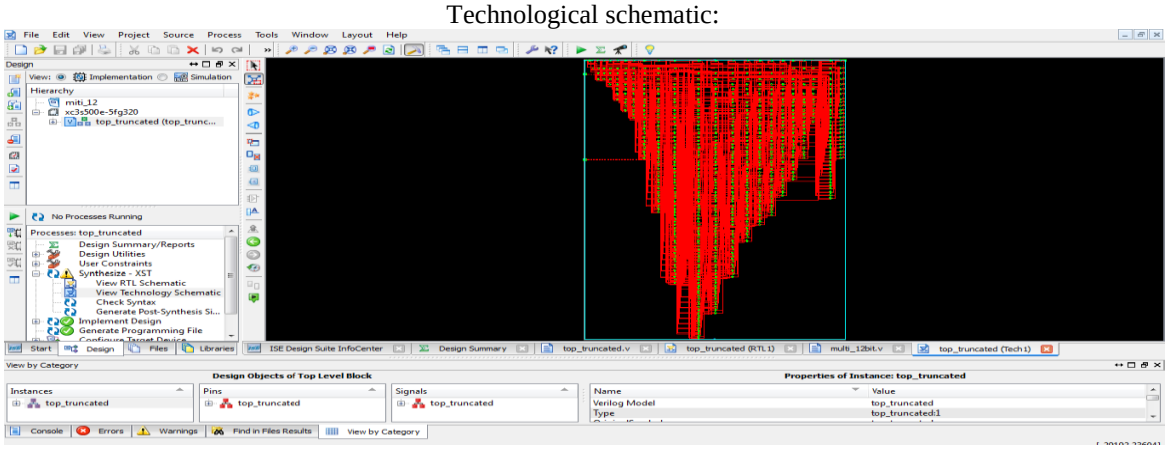
Fig 4: modified Wallace flow chart

III. RESULTS

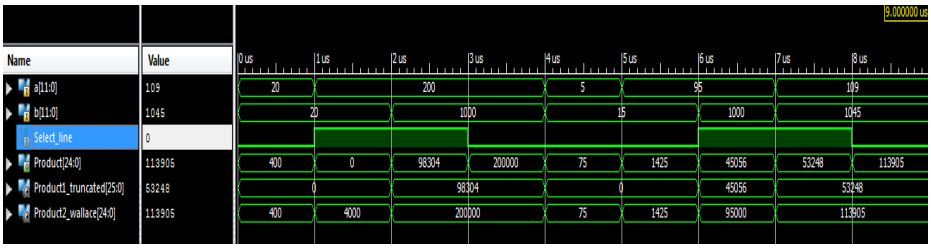
RTL schematic:



Technological schematic:



SIMULATED WAVEFORM:



Comparison Table

Multiplier	No .of LUT's	Delay	Memory
Truncated with modified Wallace	618	30.679ns	245 MB
Truncated with array	648	41.102ns	271 MB

IV. CONCLUSION

Here, in this paper two different multipliers were designed which are array multiplier and modified Wallace multiplier with the combination of truncated multiplier. In proposed design which is nothing but truncated with modified Wallace the area (in terms of LUT's) is less which are 618 when compare to the existing truncated with array multiplier which are 648. The proposed system gave best results in delay and usage of memory compared to the existed design .This multipliers output are derived depending on mux selection line, which depends on the user. In future, based upon the requirements there may be a chance to change the multipliers.

REFERENCES

[1]. Shen-Fu Hsiao, Jun-Hong Zhang Jian, and Ming-Chih Chen," Low-Cost FIR Filter Designs Based on Faithfully Rounded Truncated Multiple Constant Multiplication/Accumulation" ieee transactions on circuits and systems—ii: express briefs, vol. 60, no. 5, may 2013.

[2]. M. M. Peiro, E. I. Boemo, and L. Wanhammar, "Design of high-speed multiplierless filters using a nonrecursive signed common subexpression algorithm," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process, vol. 49, no. 3, pp. 196–203, Mar. 2002.

[3]. C.-H. Chang, J. Chen, and A. P. Vinod, "Information theoretic approach to complexity reduction of FIR filter design," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 8, pp. 2310–2321, Sep. 2008.

[4]. F. Xu, C. H. Chang, and C. C. Jong, "Contention resolution—A new approach to versatile sub expressions sharing in multiple constant multiplications, "IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 2, pp. 559–571, Mar. 2008.

[5]. F. Xu, C. H. Chang, and C. C. Jong, "Contention resolution algorithms for common sub expression elimination in digital filter design," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 52, no. 10, pp. 695–700, Oct. 2005.

Rmesh Babu Badite. "Performance Evaluation of High Speed Multipliers." IOSR Journal of Engineering (IOSRJEN), vol. 09, no. 01, 2019, pp. 15-19.