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Study of Temperature variation on Dopingless SOI

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Abstract: -In this paper, we study the impact of temperature on various performance parameters of n-type dopingless Silicon on Insulator transistor (DL-SOI). On-off current ratio (Ion/Ioff) decreases with increase in temperature. Simulation study shows that subthreshold swing (SS), drain induced barrier lowering (DIBL) and trans-conductance are degraded with increasing temperature. A comparative study is also performed between junctionless SOI transistor (JL-SOI) and DL-SOI with respect to temperature. Performance parameters such as SS, DIBL, Ion/Ioff are degraded in both the devices with increases temperature, but DL-SOI shows better performance in terms of performance parameter than JL-SOI with increasing temperature. DL-SOI also shows lower self-heating in comparison to JL-SOI device with drain voltage.

Keywords: -Dopingless, Drain Induced Barrier Lowering, Junctionless, Silicon On Insulator, Subthreshold Slope, Self-Heating.

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I. INTRODUCTION

Scaling of gate length puts severe challenges such as leakage current, short channel effects (SCEs), formation of p-n junction with steep doping profile junction and high thermal budget [1]. JL transistor overcomes the issues associated with scaling of conventional MOS device below 20 nm node. In JL transistor, source-channel-drain regions are uniformly doped with doping concentration of 10^{19} cm^{-3} [2].Uniform doping profile does not allow any junction formation at source-channel-drain regions [3]. JL transistor gives full CMOS functionally and reduction in short channel effects (SCEs).However high doping creates the problem of higher sensitivity of V_{th} and I_{off} due to random doping fluctuation (RDF) [4]. Poor off state switching is another issue associatedJL transistor [3], [5].

, DL transistor is a new proposed novel device which addresses the problems associated with JL device [6]. DL transistor contains uniformly doped source, channel and drain regions with intrinsic doping profile (10^{15} cm^{-3}). In DLtransistor, n-type source /drain regions are fabricated by charge plasma concept.Rajasekharan et al introduced the charge plasma conceptfor fabrication of p-n diode [7].

In recent paper, Chee-Woo Lee has reported electric parameters of JL device [8]. They reported the comparison study of JL device and Inversion mode device. V. Shrivastava reported the effects of temperature variation on performance of DL transistor [9]. Inthis paper, we have reported the comparative study of self-heating of DL-SOI and JL-SOI with respect to device parameters variation through 2D TCAD simulations [10].

II. DEVICE STRUCTURE AND SIMULATIONS

Figs 1(a)-(b) show the device structure of DL-SOI transistor and JL-SOI transistor. The simulation parameters for DL- SOI transistor are same as JL-SOI transistor except intrinsic silicon body with carrier concentration of $N_d = 10^{15}$ cm^{-3}. Threshold voltage is kept constant for both devices. In DL-SOI transistor source and drain regions are induced by using charge plasma concept [1]. In order to induce electron concentration at source and drain regions, the following two conditions must be satisfied:

1. Workfunction of source and drain electrode (φ_m) should be less than "$\chi_{Si} + (E_g/2q)$";where χ_{Si} is the electron affinity of Silicon, E_g is the band-gap of silicon, q is the charge of electron [1].
2. Silicon film thickness should be less than the Debye length $L_D = \sqrt{((\varepsilon V_{th})/qN)}$, where V_{th} is threshold voltage, ε is the dielectric constant of silicon [1].

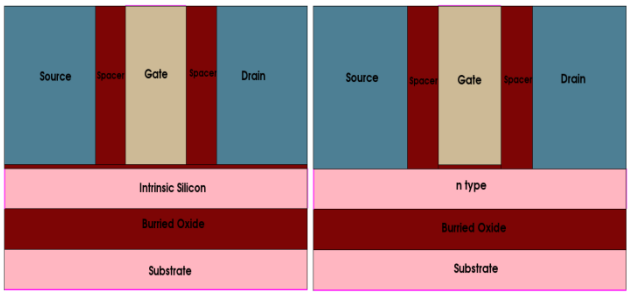
In DL-SOI device, metal with workfunction of 3.9 eV is used as source and drain electrode to induce n^+ regions [1]. The other parameters of both devices are given in the table below.

Lombardi mobility model along with Shockley- Read-Hall (SRH) and Auger recombination model is used for simulations. For temperature analysis Fermi-Dirac model is used. Impact ionization for highly doped channel is not included for simulation at constant temperature. Self-Heating analysis is carried out using

hydrodynamic model. Lombardi's mobility model shows the effect of mobility degradation due to surface acoustic phonon and surface roughness scattering. SRH model introduced the effect of defects on recombination of electrons, holes and trapped carriers [10].

TABLE I: DEVICE PARAMETERS FOR SIMULATION

Parameters	JL-SOI	DL-SOI
Silicon thickness	10 nm	10 nm
Effective oxide thickness (EOT)	1 nm	1 nm
Gate workfunction	4.7 eV	5.5 eV
S/D Extension	10 nm	10 nm
Gate length	20 nm	20 nm
Buried Oxide thickness (t_{box})	10 nm	10 nm



(a) (b)

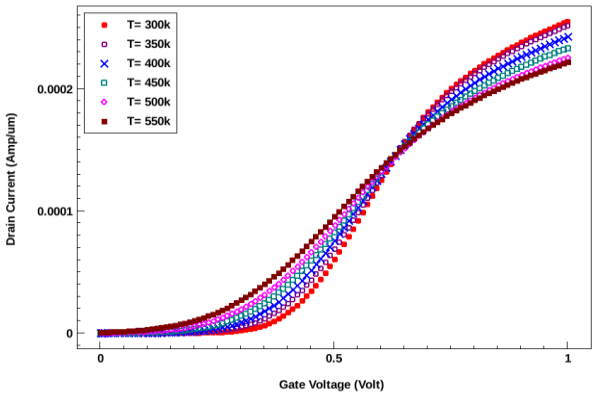
Fig.1 (a) DL SOI Structure (b) JL SOI Structure

III. EFFECT OF TEMPERATURE VARIATION

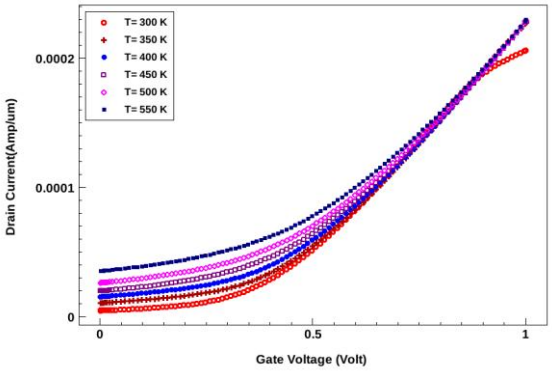
Mobility of charge carrier is controlled by two types of scattering (a) Lattice scattering and (b) Impurity scattering. In lightly doped devices mobility is controlled by lattice scattering. Thermal vibration increases with increase in temperature which increases the probability of scattering of charge carriers. In lattice scattering mobility varies as $T^{-3/2}$. In highly doped devices carrier mobility is controlled by impurity scattering. At low temperature interaction forces between charge carriers and impurity atoms are dominating due to low mobility of charge carriers. Higher interaction forces leads to higher scattering of charge carriers. At high temperature interaction forces are less dominating. Therefore scattering is reduced and mobility increases with increase in temperature. In impurity scattering Mobility varies as $T^{3/2}$.

Fig. 2 (a)-(b) show the effects of temperature variation on I_{on} of both the devices. In DL-SOI, V_{th} reduces with increase in temperature which leads to increase in I_{on}. At the same time phonon scattering dominates in DL-SOI which reduces the mobility of charge carriers.Therefore, I_{on} reduces in DL-SOI with increase in temperature due to mobility degradation. At gate voltage ~0.6 volt effects of V_{th} reduction and mobility degradation compensate each other and this gate voltage is called ZTC (zero temperature coefficients).

In DL devices mobility is mainly defined as surface mobility and interfaces at top and sidewall of the device. Interface mobility deceases rapidly with increase in gate voltage due to interface scattering. In JL devices channel lies within the bulkof device and mobility degradation is smaller with increase in gate voltage in comparison to DL devices. In JL-SOI,I_{on} increases with increase in temperature till 400 K. Above 400 K,I_{on}almost saturates because both type of scattering compensate each other. Therefore, there is no ZTC point.
Figs 4(a)- (b) show the variation of on current with respect to temperature in both of the devices.



(a)



(b)

Fig.2 Transfer characteristics of (a) DL-SOI (b) JL-SOI with respect to lattice temperature

Threshold voltage of MOS transistor is given by the

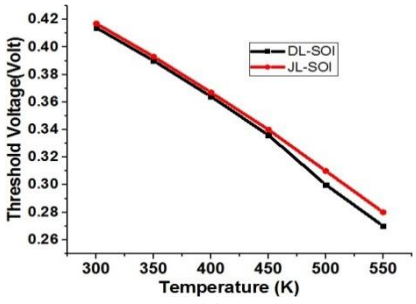
$$V_t = V_{FB} + 2\emptyset_F + \Upsilon\sqrt{2\emptyset_F} \qquad (1)$$

Where $\emptyset_F$ is the flat band voltage, Υ is the body bias coefficient and $\emptyset_F$ is the Fermi energy level. Fermi energy decreases with increasing temperature that leads to decrease the threshold voltage of both the devices. Fig 5(a) shows the variation of threshold voltage of both of the devices.

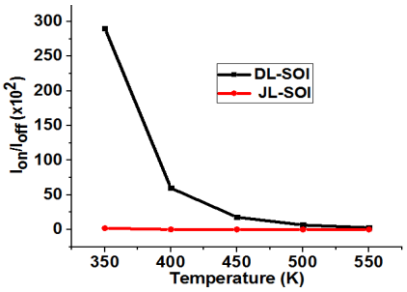
Fig 5(b) shows the variation of On current to Off current ratio. Subthreshold leakage current increases exponentially with temperature. Subthreshold current equation is with zero gate voltage can be explained by Shockley diode model

$$I_{sub} = I_o(e^{\frac{V_{DS}}{\emptyset_T}} - 1) \qquad (2)$$

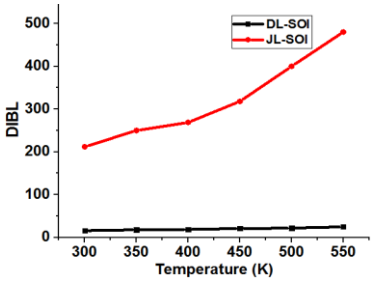
Where I_0 is the reverse saturation current and $\emptyset_T = kT/q$. Reverse saturation current I_0 doubles with 7^o increase in the temperature. DIBL increases with temperature, but DL-SOI shows lower DIBL than JL-SOI as shown in fig 3 (c).



(a)



(b)



(c)

Fig.3 Variation of (a) V_{th}(b) I_{on}/I_{off} (c) DIBL with respect to lattice temperature

IV. SELF HEATING

EFFECT OF BODY BIAS VARIATION

In n-type DL-SOI and JL-SOI transistor mobility degrades with negative body bias voltage. Mobility degradation reduces the kinetic energy of charge carriers and controls the heat generation due to collision of charge carriers. Fig 4 shows the variation of lattice temperature due to self-heating with negative body bias voltage.

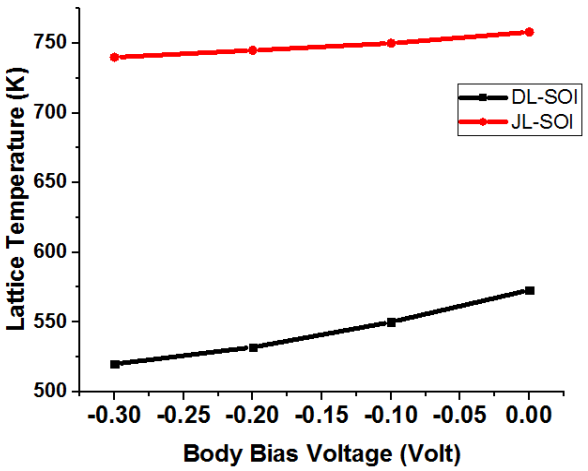


Fig 4 Variation of lattice temperature in DL-SOI and JL-SOI with respect to body bias voltage

EFFECT OF GATE LENGTH

Both of the transistors show mobility degradation with increase in gate length [2]. Mobility degradation reduces the kinetic energy of the charge carriers. Therefore, less heat is generated due to collision of low energetic charge carriers. Fig 5 shows the variation of lattice temperature in DL-SOI and JL-SOI with respect to gate length variation.

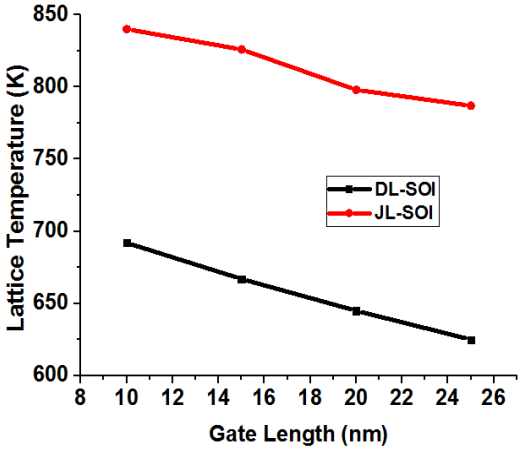


Fig 5 Variation of lattice temperature in DL-SOI and JL-SOI with respect to gate length

OXIDE THICKNESS VARIATION

Reduction in oxide thickness increases the vertical electric field components. Furthermore, increase in vertical electric field leads to decrease in lateral electric field according to Poisson equation [11]. Poisson equation states that rate of increase of electric field in one dimension decreases the electric field in another direction. Degradation of lateral electric field reduces the scattering of charge carrier. Therefore, self-heating reduces with decreasing oxide thickness.

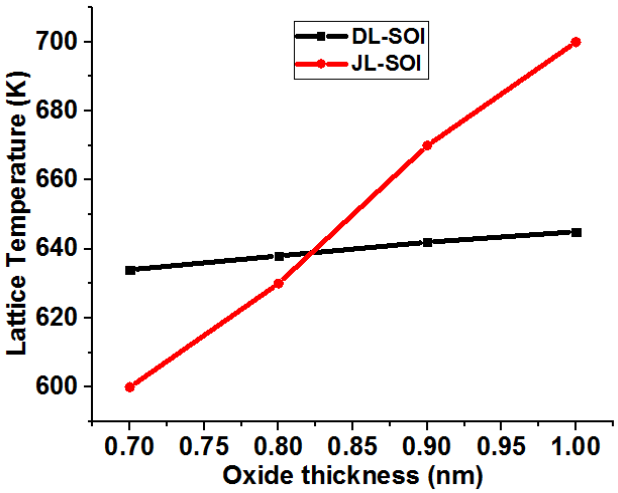


Fig 6 Variation of lattice temperature in DL-SOI and JL-SOI with respect to oxide thickness

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