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Studies on the Application of R-SFCL in the VSC-HVDC Transmission System

Puneet S. Gupta[1], Shankar S. Vanamane [2], U Gudaru [3]

[1]*(Department of Electrical Engineering, Walchand College of Engineering, Sangli, Maharashtra, India)*

[2]*(Department of Electrical Engineering, Walchand College of Engineering, Sangli, Maharashtra, India)*

[3]*(Department of Electrical Engineering, Walchand College of Engineering, Sangli, Maharashtra, India)*

Abstract: *Relating with the existing high-voltage direct- current based on line commutated converter , the voltage source converter-based HVDC (VSC-HVDC) system has several merits, but the DC short-circuit faults because of the large discharge current of the DC-link capacitor makes VSCs are more prone to fault. This paper aims to summarize a superconducting fault current limiter (SFCL), which can efficiently suppress the amplitude of short circuit current of the VSC-HVDC system. The SFCL utilizes resistance to limit the quickly rising current. Firstly, the study of working principle and operating characteristics of the SFCL. Secondly, the rules of parameters co-ordination are analysed in order to obtain the best current limiting effect of the SFCL .Lastly, a simulation model is established, and verification of the current-limiting effect of both the limiters and the parameters coordination.*

Keywords: Resistance superconducting fault current limiter, Parameter design, VSC-HVDC system.

I. Introduction

By the developments of the distributed generations, energy storage equipment and dc loads, the Voltage Source Converter based direct current distribution system is very popular. It has formidable benefit such as the low power loss, independent power control, high reliability, low investment, and so on, by Compared with the traditional alternating current distribution system and the line commutated converter (LCC) based direct current system. There is a lots of development in power electronic technology and fully controlled power electronic devices. The pulse width modulation technique and high-voltage-direct-current system based on (VSC-HVDC) has been studied and in very much application now a days. For bulk power transmission VSC-HVDC is a very much reliable and cost-effective solution. Due to the advancement in the VSC-HVDC system have shown better alternate than traditional conventional thyristor-based HVDC systems [1] In VSC-HVDC there is no protection against DC line fault as compared with thyristor based HVDC system [2]. When the dc side fault occur the fault current will increases to ten times within few milliseconds because discharging of dc side capacitor and ac fault current will be feed into the system through the freewheeling diodes act as a rectifier bridge so converter will be damaged during the fault [3].In DC current there no natural zero as compared to sine wave so by forcing the large dc current to zero causes very high energy stress on dc circuit breaker components. There is no acceptable solution has been found to interrupt HVDC short-circuit currents although number of ideas for HVDC breaker schemes have been published and patented. This is the major challenge to VSC-HVDC transmission technology [4]. A fault current limiter can limit the large fault current during the response time of DC circuit breaker in a VSC-HVDC transmission system. The current interruption stress on DC circuit breakers can be mitigated by installing a fault current limiter.

Many scientist are studying and implementing the super conducting fault current limiter (SFCLs) in HVDC system and they recommended SFCL for its low power dissipation and fast response during the normal operation. Reference [5] proposed flux-coupling-type SFCL for an HVDC system which can limit dc fault current's amplitude and maintain a small rate of the dc current change, which is helpful to prohibit the commutation voltage reduction, so in this way by the application of SFCLs we can decrease the chance of HVDC commutation failure. Reference [6] proposed the inductive type the saturated iron core type superconductive fault current limiter (SI-SFCL) is studied along with its working principle and electrical

properties and its verification of current suppressing action is studied in VSC-HVDC system. In this paper, the proposed SFCL is studied and applied to reduce the effect of DC short circuit on a VSC-HVDC transmission system. This SFCL use the resistances to suppress the rapidly rising current. The resistive SFCL is very fast in operation and it has instantaneous operation and return back to original state after the operation. In Section II the introduction of resistive SFCL, its parameter co-ordination and integration of SFCL with a VSC-

HVDC system is studied. In Section III MATLAB model is built with integration of resistive SFCL in VSC-HVDC. In Section IV the DC fault study in a VSC-HVDC system and study of results is being done.

Reference [7] proposed the comparison between inductive and resistive SFCL performances. The results demonstrate that both SFCL reduces the current, suppress the voltage fluctuations and reduces the power. After studying restraining capability to voltage fluctuations, current limiting ratio and all over performances it is concluded that resistive SFCL is better than inductive SFCL. Preliminary study of optimization of SFCL is studied on the basis of current suppression, cost of equipments and stability of voltage. Reference [8] proposed the study of short circuit and ground fault in VSC-HVDC system .Author suggest that critical time limit of a switch gear system will be decided by the most serious short circuit fault by doing simulation .In this paper the fault location method has been proposed for ground faults under various circumstances such as operating situations, resistances, distances and it is verified by the simulations. Reference [9] proposed the application of different SFCL in a VSC-HVDC system as per transient nature of DC fault. The technical aspect and parameter designing of resistive SFCL is also discussed. In this paper the resistive SFCL is suggested for VSC-HVDC system because of its sensitivity towards DC fault proper quenching resistance capability and during the fault process the voltage variation decays in over damping nature due to pre-dominance of resistance in SFCL.

II. Theoretical Analysis

A. Principle of the Resistive SFCL

The schematic configuration of the resistive SFCL is shown in Fig. 1 This device is mainly consist of normal switch from where current is flowing during normal state but as the fault occur the current is diverted through high resistance path. The suppression of current is due to the resistance only. As per the fault current the resistiv e SFCL built up the resistance to limit fault current in with a very fast response time. This device will be integrated with a VSC-HVDC system.

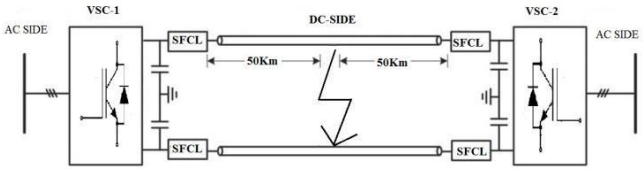

Fig.1. Diagrammatic configuration of the resistive SFCL

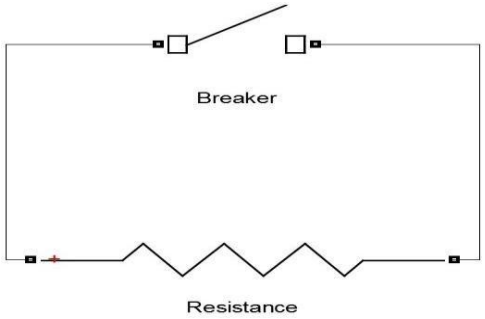

Fig 2: Diagrammatic Schematic of the VSC-based HVDC system and the integration with SFCLs.

Fig. 2 shows the diagram of a VSC- based HVDC transmission system integrated with the SFCL, the circuit impedance is represented by Zs, It also depicts a typical VSC-based dc system, in which the SFCLs are integrated at the terminals of the dc lines. During a dc fault, the SFCLs should limit not only the dc-side fault current but also the over current at the ac side and in the converter station. For simplification of the analytical process SFCL's characteristics the equivalent circuits, which are based on the operation status of the SFCL under normal condition and faulted condition are explained are given in Fig. 3.

(1)

Under the normal condition the current is flowing from without any obstruction of resistance, , so there will be zero resistance (superconducting state) drop during the steady state operation but as the fault occurs the whole current switch to high resistance path within millisecond, this initiates the load current to the high impedance path. The incipient of fault current is limited in less than one cycle.

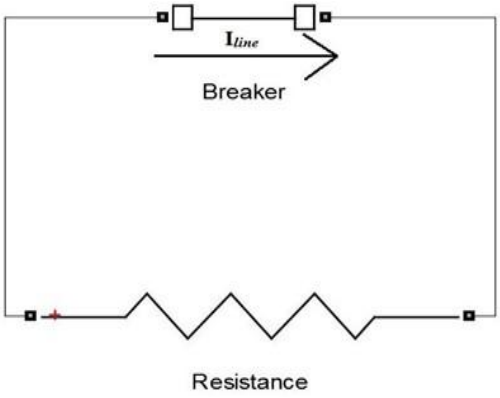

Fig 3a: Operation status of the VSC-HVDC transmission system

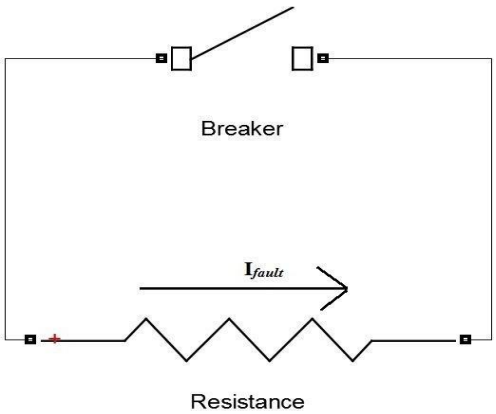

Fig 3b: During the fault operation process

The rapid increase in resistance produces the suppression of current , according to fault current the resistance is developed.

B. Resistive SFCL parameter design

This part explains the current-suppressing effects with respect to different values of *R1*. Thus, in order to decide the optimal current suppressing effect of the resistive SFCL, it is very meaning full to select the perfect values o *R1* in practical application.

According to the fault transient characteristics analysis of a VSC-HVDC system [8], the fault process can be divided into three stages, which are capacitor discharge stage, diode free-wheel stage and grid-side current feeding stage. The transient characteristic of the DC-side voltage Vdc and the corresponding characteristic roots can be expressed as

(2)

(3)

In this L, R, and are values of the equivalent inductance, resistance and of the DC fault circuit, respectively, *C* is the value of the DC capacitor.

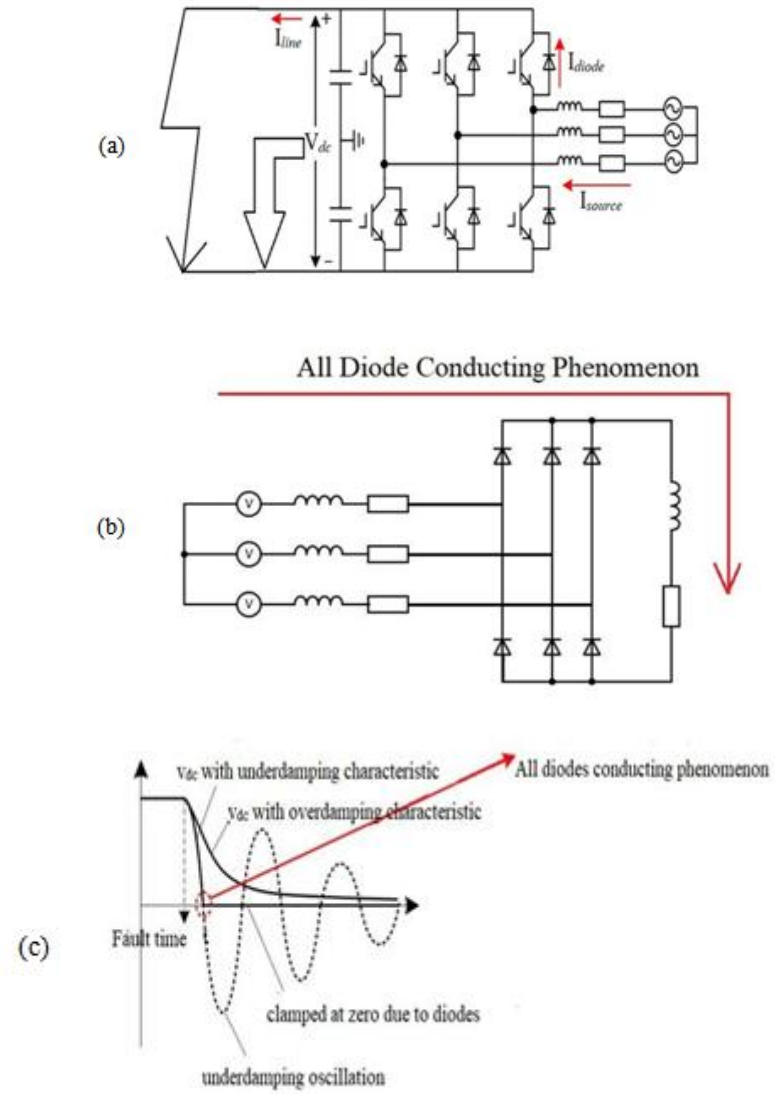

Fig 4(a,b,c): Equivalent circuit of the dc pole-to-pole fault and the transient characteristics of the dcvoltage.

Fig. 4 shows the equivalent circuit diagram of a dc pole-to-pole fault which is the most severe fault among all types of dc faults. In the primary stage of the fault, the large capacitor at the port of the converter discharges to the fault location, providing a high current for the dc-side lines.

Noticeably, the characteristic roots are a couple of conjugated imaginary numbers when under this condition, the variation of Vdc is the under damping oscillation process as shown in Fig. 4. Once Vdc oscillates to zero, all the freewheeling diodes in the converter will conduct simultaneously because the dc fault circuit inductance drives the fault current to flow through them, which is called as the all-diodes conducting phenomenon [8] . At that instant, the diode gets shocked due to the high surge current from the dc fault circuit inductance.

For the ac system, it can be considered that a three-phase fault occurs because all the diodes are conducted and no longer show in one directional characteristic [8]. On the contrary, the characteristic roots are a couple of real numbers if Under this condition, the variation of Vdc is an over damping decay process and the value of Vdc will not decrease to zero, as shown in Fig. 4. Hence, the all-diodes-conducting phenomenon does not happen, namely, the over current does not occur in the converter and the ac side.

Generally, the resistance of the dc fault circuit is so small that the underdamping oscillation condition is easily satisfied [8]. And due to this overcurrent is set up in whole power system.

If the reactive SFCL is applied in the VSC-based dc system, the dc-side fault current should be limited efficiently because the reactive SFCL shows a high inductance (*Ls*) after the dc fault. But, it is unable to avoid the negative impact on the ac side and the converter because the underdamping oscillation condition

still satisfied. so, the reactive SFCL can only limit the dc-side fault current, but not eliminate the serious effect on the ac side and the converter. It is clear that the dc-side fault current after a dc fault can be limited by a resistive SFCL which is applied in the VSC-based dc system. So, the damping characteristic of the dc fault circuit can be changed from the underdamping condition is still satisfied. so, the reactive SFCL can only limit the dc-side fault current, but not eliminate the serious effect on the ac side and the converter. It is clear that the dc-side fault current after a dc fault can be limited by a resistive SFCL which is applied in the VSC-based dc system. So, the damping characteristic of the dc fault circuit can be changed from the underdamping condition to the overdamping condition easily with the increase of the resistive SFCL resistance (*Rs*). Under the condition of the overdamping decay process, the value of Vdc will not decrease to zero anymore. Thus the all-diodes-conducting phenomenon is avoided and the currents at the ac side and in the converter are also limited drastically. In sum, the resistive SFCL is more suitable for the VSC-based dc system compared with the reactive SFCL because it is capable to suppress the whole-system overcorrect when a dc fault occurs.

C. Necessity of the Resistive SFCL

As per the above descriptive analysis, the resistive SFCL suppress the over current during a dc fault from two ways. Firstly, it suppress the dc-side fault current by generating a resistance into the fault circuit and Second one, due to the resistance the damping characteristic changes from under damping to over damping, so that the dc voltage does not go to zero and there will be no shocking effect to the ac side devices and converter diodes . As per the transient characteristics of the dc fault [8], it is determine that the dc-side fault current increases and the dc voltage Vdc reduces very quickly when the dc fault occur. so, some conditions must be followed when the resistive SFCL is designed to be applied into the VSC-HVDC system. First one, the dc- side over current just occurs at the initial stage of the fault so the resistive SFCL must be sensitive enough to the dc side fault. Second one, to limit the dc current at secure level the value of quenching resistance should be large enough. To maintain over damping nature the quenching resistance value will be large enough. At last, In order to satisfy the fast restoration of the VSC-based dc system the recovery time of the SFCL must short. Another view, such as economy, maintenance and footmark, should also be taken care, which an area for further research remain in consideration.

III. Simulation Analysis

In order to analyse the resistive SFCL's performance in a VSC-HVDC transmission system, a simulation model which is corresponding to Fig.2 is built in MATLAB/SIMULINK. Main simulation parameters are indicated in Table I.

A. Primary parameter selection of the Resistive SFCL

The values of current-suppressing resistance may have a short range when the SFCL is applied in a high-voltage system with a certain short-circuit capacity. As for the specific VSC-HVDC system (± 160 kV), the maximum fault current reaches 25 kA without any limiter. Herein, the value range of the current-limiting resistance is about 13~6 Ω with the expected current-suppressing ratio of nearly 34%. Due to the expected current- suppressing ratio of 34%, the primary parameter selection is in Table II. However, the Resistive SFCL with design parameters of different value of resistor are also shown.

Table: Simulation Parameter of VSC-HVDC Transmission System

Parameters	Value
DC voltage	160 kV
Rated capacity	160 MVA
DC capacitor	0.03 F
AC reactor	0.01 H
Resistance of the dc line	0.0139 Ω/km
Inductance of the dc line	0.159 mH/km
Length of the dc line	100 km

Table: Parameter of Resistive SFCL in Different Cases

tor value (ohm)	Fault current(Ampere)
13 ohm	4975
8 ohm	7200
6 ohm	8400

B. *Matlab Simulink model of VSC-HVDC system*

Fig. 5 shows the simulink model of a VSC-HVDC transmission system integrated with the SFCLs and in Fig. 6 shows the simulink model of a SFCL , in this model there are two current measurement devices ,one current device is in series with transmission line going towards controlled voltage source and another current measurement device connected with RMS converter after that SFCL characteristic table is there in which for different value of current different resistor is present , as fault occur the current will be increases and voltage will decreases so as per the fault current the particular value of resistance from SFCL characteristic table is selected and current is decreased to a particular limit and voltage is maintained to a particular value. Controlled voltage source is used to maintain voltage sag.

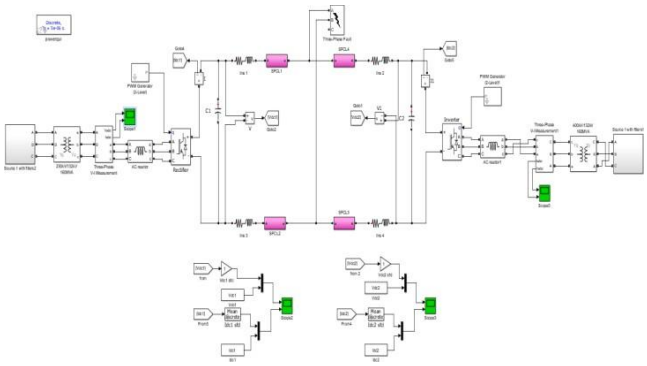

Fig 5: VSC-HVDC system integrated with SFCl designed in Simulink

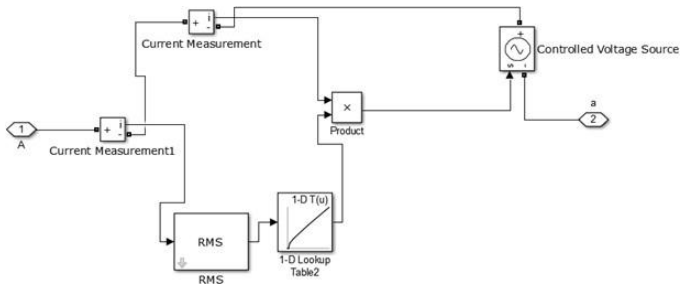

Fig 6: Resistive SFCL developed in Simulink

C. *Current-suppressing Capability Verification of the SFCL*

Simulation conditions are described as a pole-to-pole fault occurs at t=.4sec. The fault position is 50 km fromtheVSC1.

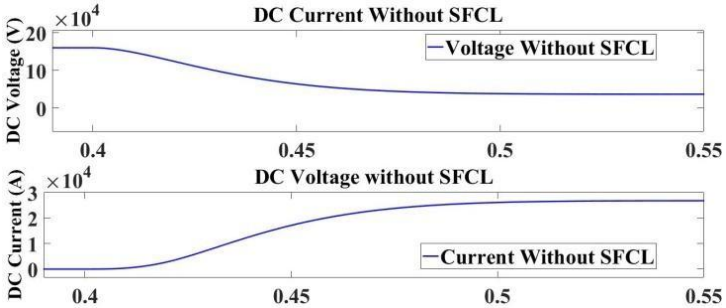

Fig 7: DC Current and Voltage without SFCL

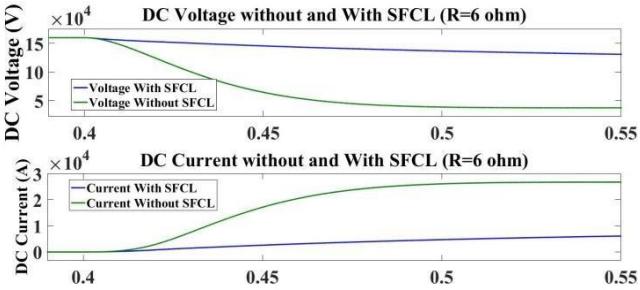

Fig 8: DC Current and Voltage Without and With SFCL R=6ohm

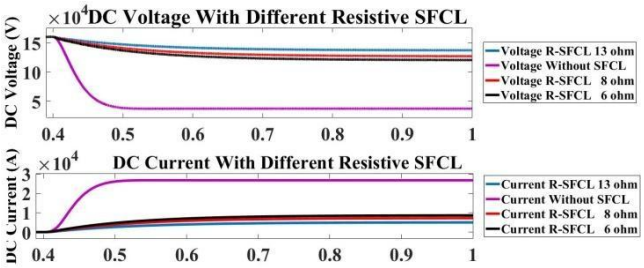

Fig 9: Comparison of DC Current and Voltage with different value of SFCL

From fig. 7 It is clearly shown in result the fault voltage goes to 1.5KV and the fault current increases very rapidly upto 25KA which is very high value, So in fig. 8 the by inserting the value of R-SFCL 6ohm the current is brought down to 8400A which is approximately 34% of fault current and voltage is increases up to 122KV so that by implementing resistive SFCL the voltage follows an overdamping decay so it has effect on AC-side of voltage source converter. In fig. 9 comparison of voltage and current is done during different values of SFCL. When R=13ohm the voltage is increases upto 137.5KV and current is decreases to 4975A. When R=8ohm the voltage is increases upto 127.5KV and current is decreases to 7200A. When R=6ohm the voltage is increases upto 122KV and current is decreases to 8400A. So by varying the value of resistance in a SFCL the current is decreased and voltage is made increases so that overdamping decay nature is followed. From the above result the R-SFCL application is verified in VSC-H VDC system.

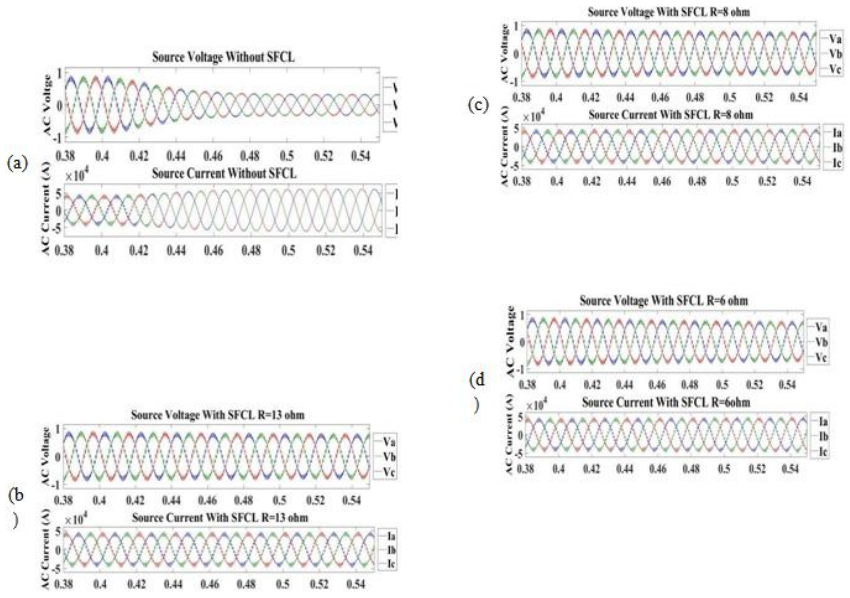

Fig 10: Three-phase AC fault current flowing through the rectifier-side under the fault. (a) With no SFCL. (b) With the resistive SFCL (RSFCL = 13 ohm). (c) With the resistive SFCL (RSFCL = 8 ohm) .(d) With the resistive SFCL (RSFCL = 6 ohm)

As the fault occur its impact can be seen in the AC-Side of the system at t=.4 sec as shown in Fig. 10. (a) the current is increasing and voltage is decreasing in ac side without SFCL, but as the SFCL of value 13ohm is implemented the magnitude of current is increases by very less value and voltage also decreases by less value similar results are shown in case of R-SFCL in case of 8 ohm and 6 ohm, so in this way by maintaining the resistance value overdamping nature its impact can also be verified in AC-Side of VSC and AC voltage and current is in secure level.

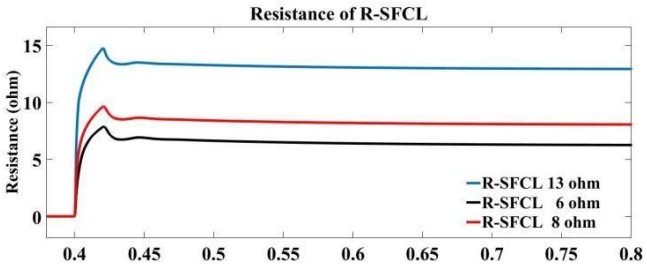

Fig 11: Comparison of different value R-SFCL

From fig. 11. It is clear that the at fault time t=.4sec the resistance of R-SFCL is build up 13,6 and 8 for suppressing the fault current. The above simulation analysis can be used as the basis for parameter selection of the R-SFCL in practical application.

IV. Conclusion

As per the working principles and performance characteristics, the SFCL offers best possible solutions to suppress the dc fault current. Based on the electromagnetic transient characteristics of the dc fault in the VSC-based dc system the resistive SFCL is suggested to be applied in the VSC-based dc system. And it should be fast to develop an enough quenching resistance and ensure the variation of the dc voltage is an overdamping decay process after a dc fault. Besides, the influence of the SFCL parameters on the current limiting capability is discussed by different simulation cases, providing the theoretical reference for designing the dc-system used resistive SFCL. In the near future, a prototype of the R-SFCL will be fabricated and its practical application in a VSC-based system will be assessed.

References

[1]. D. Jovcic, D. van Hertem, K. Linden, J. P. Taisne and W. Grieshaber, "Feasibility of DC transmission networks," *Innovative Smart Grid Technologies (ISGT Europe), 2011 2nd IEEE PES International Conference and Exhibition on*, Manchester, 2011, pp. 1-8.

[2]. J. Yang, J. O'Reilly and J. E. Fletcher, "An overview of DC cable modelling for fault analysis of VSC-HVDC transmission systems,"

[3]. *Universities Power Engineering Conference (AUPEC), 2010 20th Australasian*, Christchurch, 2010, pp. 1-5.

[4]. A. A. Elserougi, A. S. Abdel-Khalik, A. M. Massoud and S. Ahmed, "A new protection scheme for HVDC converters against DC-side faults with current suppression capability," *IEEE Trans. Power Del.*, vol. 29, no. 4, pp. 1569-1577, Aug. 2014.

[5]. C. M. Franck, "HVDC circuit breakers: a review identifying future research needs," in *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 998- 1007, Apr. 2011.

[6]. L. Chen, H. Pan, C. Deng, F. Zheng, Z. Li and F. Guo, "Study on the application of a flux-coupling-type superconducting fault current Limiter for decreasing HVDC commutation failure," *Can. J. Elect. Comput. Eng.*, vol. 38, no. 1, pp. 10-19, Winter 2015.

[7]. B. Li, F. Jing, J. Jia and B. Li, "Research on saturated iron-core superconductive fault current limiters applied in VSC-HVDC systems,"

[8]. *IEEE Trans. Appl. Supercond.*, vol. 26, no. 7, pp. 1-5, Oct. 2016.

[9]. L. Chen, H. Chen, Z. Shu, G. Zhang, T. Xia and L. Ren, "Comparison of inductive and resistive SFCL to robustness improvement of a VSC-HVDC system with wind plants against DC fault," *IEEE Trans. Appl. Supercond.*, vol. 26, no. 7, pp. 1-8, Oct.2016.

[10]. J. Yang, J. E. Fletcher, and J. O'Reilly., "Short-circuit and ground fault analyses and location in VSC-based DC network cables." *IEEE Trans. Ind. Electron.*, vol. 59, no.10, pp. 3827-3837, Oct. 2012.

[11]. Bin Liand JiaweiHe," Studies on the Application of R-SFCL in the VSC-Based DC Distribution System" *IEEE Trans ON Appl Supercond*, vol. 26, no. 3, april 2016