"Design and Implementation of High Throughput Vlsi Architecture For Ldpc Decoder"

Shraddha Pawankar[1], Prof. Nilesh Mehta[2]

[1]*M.Tech student Department of Electronics, JD College of Engineering and Management, Nagpur, India.*
[2]*Assistant professor Department of Electronics, JD College of Engineering and Management ,Nagpur, India.*

Abstract: *In the present era, more powerful error correcting tools is a Low-density parity-check code among the other error correcting tools. In this paper, the target device is a Field Programmable Gate Array (FPGA) implementation of LDPC. Here used Min-Sum (MS) algorithm for decoding structure minimize the complexity of the variable node unit (VNU) and check node unit (CNU) to achieving less slice resources. To get results in less slice resources a multiplexed storage structure is used for the storage of node messages. It encodes 324 message bit and creates 648 bit encoded message. This message passes through Additive white Gaussian noise AWGN channel. Hardware resources act as a very important factor in many applications like deep space communications and its efficient utilization area. The high performance is expected from LDPC decoders used in space data systems. In space data system used LDPC decoder to achieve high performance and low complexity. This low-complexity implementation is an efficient method to the requirements put forward by many and wireless communication systems.*
Index Terms: *LDPC decoder, Low-complexity implementation minus algorithm, FPGA and Quartus-II.*

I. Introduction

In wireless communication, it is important that the communication systems must be substantial in order to transmit the information from the source to the destination using a communication channel with high reliability. This in fact is a difficult task since in the physical world there exist many error causing factors as a result detecting and correcting errors is very important while transmitting information. If errors occur and we cannot detect and correct them, the received information at the receiver will be of no use, as it will differ considerably from the original source information. In the past few years, some practical code classes which can achieve transmission at rates very close to the channel capacity have been introduced. Two major representatives of this class of codes are LDPC and Turbo codes.

Low Density Parity Check (LDPC) codes were first introduced by Gallager in 1962, and after being rediscovered in 1996, these error correction codes have been constantly in the center of attention for researchers. Their superior correction performance and highly parallelizable decoding algorithms have resulted in adoption in many recent communication standards. LDPC codes are block codes with parity check matrices that contain only a very small number of non-zero entries. The linear increase in decoding complexity and minimum distance of LDPC decoders is attributed to this sparseness of H matrix. Graphically, the parity check matrix can be represented in the form of a Tanner Graph.

Throughput and power requirements of emerging communication systems have been constantly growing. For instance, recent wireless communication standards have increased their throughput to beyond 1 Gbps. These factors have resulted in high demand for innovative and adequate methods to tackle design challenges for LDPC codes.

II. Objective

Convertible LDPC decoders because of Large bit stream of encoded bits result in low through put and lower decoding bit rate. Our proposed architecture uses the minus algorithm for decoding the encoded bit stream. The throughput by the use of minus algorithm.

International Conference on Innovations in Engineering, Technology, Science & Management –   75 | Page
2019 (ICI-ETSM-2019)
Jhulelal Institute of Technology (JIT) is governed by Samridhi Sarwajanik Charitable Trust (SSCT), Koradi Road, Village Lonara, Nagpur-441111.

III. Work Related

1. ZhiqiangCui1 ,Zhongfeng Wang1 , Xinmiao Zhang2 , and Qingwei Jia3 1 Oregon State University, Corvallis. 'Efficient Decoder Design for High-Throughput LDPC Decoding'

In this paper, a matrix permutation scheme is proposed to convert a generic QC-LDPC code to a shift-structured LDPC code.Thus, efficient VLSI architectures can be developed to achieve very high decoding throughput with low hardware complexity.

2. Junho Cho, Member, IEEE, Jonghong Kim, and Wonyong Sung, Senior Member, IEEE 'VLSI Implementation of a High-Throughput Soft-Bit-Flipping Decoder for Geometric LDPC Codes' May 21, 2010

In this paper, a low-complexity high-performance algorithm is introduced for decoding of such high-weight LDPC codes. The developed soft-bit-flipping (SBF) algorithm operates in a similar way to the bit-flipping (BF) algorithm but further utilizes reliability of estimates to improve error performance. A hybrid decoding scheme comprised of the BF and SBF algorithms is also proposed to shorten the decoding time. Parallel and pipelined VLSI architecture is developed to increase the throughput without consuming much chip area.

3. Thien Truong Nguyen-Ly, ValentinSavin, Khoa Le, 'Analysis and Design of Cost-Effective, High-Throughput LDPC Decoders' 23 Aug 2017

In this paper introduces a new approach to cost-effective, high-throughput hardware designs for Low Density Parity Check (LDPC) decoders. The proposed approach, called Non-Surjective Finite Alphabet Iterative Decoders (NS-FAIDs), exploits the robustness of message-passing LDPC decoders to inaccuracies in the calculation of exchanged messages, and it is shown to provide a unified framework for several designs previously proposed in the literature.
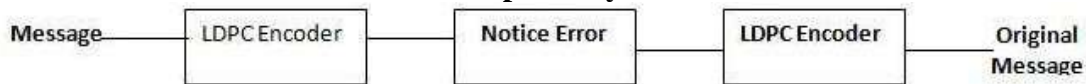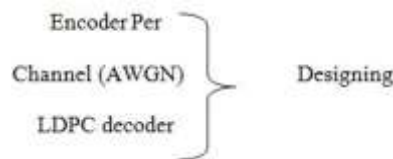
IV. Proposed System

Fig.1. digramatic representation for LDPC Encoder

This is the purposed system what we are going to use in high throughput VLSI architecture for LDPC decoder

LDPC decoder decodes the encoded message by using minus algorithm where it produces the exact message bits by using row & column processing

V. Simulation Results

In this section, the performance of LDPC codes with different decoding algorithms is simulated with MS-based simplified algorithms and NMS algorithm as a standard. The (648,324) and (648,540) QC-LDPC code in Verizon 5G standard are utilized for evaluating the bit-error-rate (BER) performance of all the decoding algorithms with different signal-noise-rate (SNR). Additive white Gaussian channel (AWGN) noise is considered as the channel model. The maximum number of iterations is set to 10 in all simulations. QPSK is used as the modulation scheme. The scaling coefficient is set to 4/5 in all the simulations.

Figure 1 compares the simulation results of the proposed algorithm compared with standard NMS algorithm. With the same number of iterations, the performance loss is nearly

dB when the code rate is 1/2. When the code rate goes up to 5/6 , the performance loss is nearly 0.15dB.

*International Conference on Innovations in Engineering, Technology, Science & Management –
2019 (ICI-ETSM-2019)*   76 | Page

Jhulelal Institute of Technology (JIT) is governed by Samridhi Sarwajanik Charitable Trust (SSCT), Koradi Road, Village Lonara, Nagpur-441111.
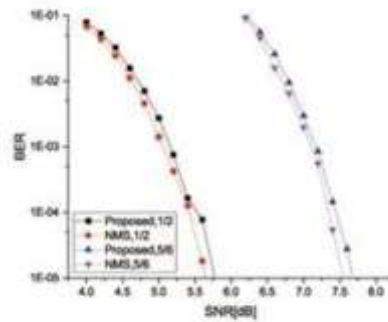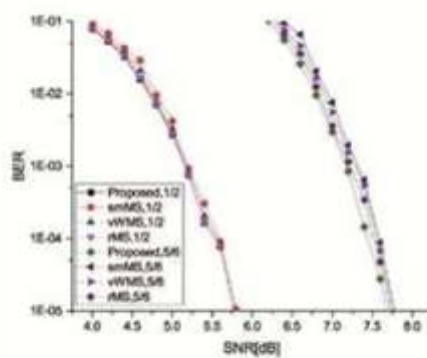
Figure 1. BER perfomance of proposed and NMS algorithms

gure 2. BER perfomance of proposed and existing simplified algorithms

Solution Techniques:-
1. We address the problem of LDPC code construction, analysis, and VLSI implementation from a different and significantly broader perspective.
2. The crux of the proposed approach is that VLSI implementation-aware code design can lead to an exceptional increase in data throughput and overall code performance by means of careful choices of VLSI implementation and circuit design techniques.
3. In this context, a joint optimization of code-related and hardware-imposed code constraints is performed.
4. The first set of constraints includes characteristics such as large girth and minimum distance of the codes; the second set of constraints is related to VLSI issues such as routing congestion, cross-talk minimization, and uniform processing delay in one iteration, power conservation, and chip size reduction.
5. For the purpose of fast prototyping, FPGA implementations of the proposed coding scheme can be devised, relying only on the structure of the code graphs and not on the actual VLSI layout.

VI. Results

Our objective that the architecture uses the minus algorithm for decoding the encoded bit stream. The throughput by the use of minus algorithm is achieved.

VII. Conclusion

Thus we have designed and implemented high throughput VLSI architecture for LDPC decoder.In future, for the purpose of fast prototyping, FPGA0 implementations of the proposed coding scheme can be devised.

International Conference on Innovations in Engineering, Technology, Science & Management – 77 | Page
2019 (ICI-ETSM-2019)
Jhulelal Institute of Technology (JIT) is governed by Samridhi Sarwajanik Charitable Trust (SSCT), Koradi Road, Village Lonara, Nagpur-441111.

References

[1]. A. J. Blanksby and C. J. Howland, "A 690-mW 1-Gb/s 1024-b, rate-1/2 low-density parity check code decoder," IEEE Journal of Solid- State Circuits, vol. 37, pp. 404-412, March 2002.

[2]. R. M. Tanner, "A recursive approach to low complexity codes," IEEE Trans. Inf. Theory, vol. IT-27, no. 5, pp. 533–547, Sep. 1981.

[3]. F. R. Kschischang, B. J. Frey, and H.-A. Loeliger, "Factor graphs and the sum–product algorithm," IEEE Trans. Inf. Theory, vol. 47, no. 2, pp. 498–519, Feb. 2001.

[4]. J. Barry, A. Kavcic, S. McLaughlin, A. Nayak, and W. Zeng, BIterative Timing Recovery,^ IEEE Signal Process. Mag., vol. 21, 2004, pp. 89–102.

[5]. A. J. Blanksby and C. J. Howland, BA 690-mW 1024-b, Rate 1/2 Low-density Parity-check Code Decoder,^ IEEE J. Solidstate Circuits, vol. 37, no. 3, 2002, pp. 404–412.

[6]. Y. Kou, S. Lin, and M. P. C. Fossorier, "Low-density parity-check codes based on finite geometries: A rediscovery and new results," IEEE Trans. Inf. Theory, vol. 47, no. 7, pp. 2711–2736, Nov. 2001.

[7]. J. Cho and W. Sung, "High-performance and low-complexity decoding of high-weight LDPC codes," (in Korean) J. Korea Inf. Commun. Soc., vol. 34, no. 5, pp. 498–504, May 2009.

[8]. J. Cho and W. Sung, "High-performance and low-complexity decoding of high-weight LDPC codes," (in Korean) J. Korea Inf. Commun. Soc., vol. 34, no. 5, pp. 498–504, May 2009.

[9]. M. P. C. Fossorier, M. Mihaljevic, and H. Imai, "Reduced complexity iterative decoding of low-density parity check codes based on belief propagation," IEEE Trans. Commun., vol. 47, no. 5, pp. 673–680, May 1999.

[10]. J. Chen, A. Dholakia, E. Eleftheriou, M. P. C. Fossorier, and X.-Y. Hu, "Reduced-complexity decoding of LDPC codes," IEEE Trans. Commun., vol. 53, no. 8, pp. 1288–1299, Aug. 2005.

[11]. J. Zhang and M. P. C. Fossorier, "A modified weighted bit-flipping decoding of low-density parity-check codes," IEEE Commun. Lett., vol. 8, no. 3, pp. 165–167, Mar. 2004.