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Reconfigurable Cache Memory Architecture Design Based On VHDL

Ms. Amber Shaikh[1], Prof. Mayuri Chawla[2]
[1](Department of M.Tech (VLSI Design),Jhulelal Institute of Technology, Lonara.Nagpur, India.)
[2](Department of M.Tech (VLSI Design),Jhulelal Institute of Technology, Lonara.Nagpur, India)

Abstract: *Advances of microprocessor design has been putting multiple cores on a single chip giving ways to internal parallel computing an exodus from increase in single clock frequency to provide remarkable growth in speed. What's significant is that each configuration presents itself to developer as a set of two or more cores capable of executing multiple tasks concurrently. Current advancements in industry highlight reconfigurable architectures as the new trend capable of conquering complexity of design, computational time and cost the primary research aspect of our paper. This research highlights the amendments/advancements in the chache memory for multi-core processor and its architecture for demonstrating its capability via reconfigurability. Due to abundant amount of data, many applications impose heavy resource requirements on the hardware platform. So our main purpose is to provide a simulation environment to applications demanding such heavy resource requirements.*

Keywords: *Multi-core, Optimization, Reconfiguration, VHDL*

I. Introduction

The modern microprocessors performance depends on the processing speed and energy saving feature. High processors speed require an equivalent speed for memory system .

Cache memory represents an important part because it reduces the speed gap between CPU (Central Processor Unit) and RAM (Random Access Memory). Cache memory prefetching the data from the main memory before the processor request for it with phenomenon known as locality of reference. Several parameters related to the cache performance are cache size, degree of associativity, number of words per block, access time and amount of energy consumption.

Power consumption has become a major design consideration. The cache memory occupies about 45%-55% of total chip area and consumes about 50% of a microprocessor's energy, a large amount of active energy is consumed as static power due to leakage currents without any operation, and consumes a dynamic power in read/write operations.

The performance of cache memory is determined by specific applications. Better energy performance is achieved by different applications with different configuration of the cache memory. The amount of consumed energy and memory access time has a direct correlation with cache parameters, bigger cache size and higher associativity require more energy consumptions and longest access time and most times increase the amount of hit rate, at the same time the smallest size of cache memory and less degree of associativity might cause a poor hit rate and this consuming more energy in each main memory access.

This complex relation between the hit rate, cache access time and amount of energy consumption of cache memory for different applications gives the importance for making reconfigurable cache memory. Several solutions have been proposed to reduce the energy consumption of the cache memory.

II. Literature Survey

In the paper by "Ibrahim A. Amory" VHDL is used to design and implement a 2D Reconfigurable Cache memory using FPGA (Field-Programmable Gate Array). In this design the cache memory architecture allows to change the organization of memory and the memory size with the use of a cache size controller unit and a way controller unit, to improve the processor performance and reduces the energy consumption, and using all available memory size for all possible organization that can be selected [1].

In the paper by "A.D. Santana Gil and J.I. Benavides Benitez," Cache memory is a common structure in computer system and has an important role in microprocessor performance. The relation between the performance of algorithm and main cache parameters such as number of words per block, associativity, and cache size has been demonstrated. In this paper, we propose a reconfigurable cache with several working modes [2].

In the paper by "Po-Hao Hsu and Shao-Yi Chien, " the main objective of this paper is the development of reading skills in Machines. After reading the text and understanding the meaning, it would self-program itself and would implement the instructions. This investigation presents an algorithm which recognizes text and character with specific protocol in a live streaming video and programs itself [3].

III. Propose Methodology

In this paper a three dimensional reconfigurable cache memory is designed with new controller units and programmed using hardware description language. The design allows reconfiguration in cache size, cache associativity and cache block size. Memory size can be (64K Byte, 128K Byte, 256K Byte and 512K byte), the associativity can be (Direct mapped (DM), 2 way, 4 way and 8 way set associative) and cache block size can be (4 words, 8 words and 16 words per block).

Memory size of 512 Kbytes is designed with eight sets of cache memory each with size 64K byte, for DM the maximum size is 512K byte and the CPU is dealing with the eight sets as one set with size 512K byte and for set associative organization the maximum cache size is 512K byte too, hence, the maximum cache memory size for each organization is equal to the already occupied cache memory size, then there is no waste in cache memory size, this is the contribution of this design as well as the (VHDL) hardware description language which used to implementing the design on FPGA.

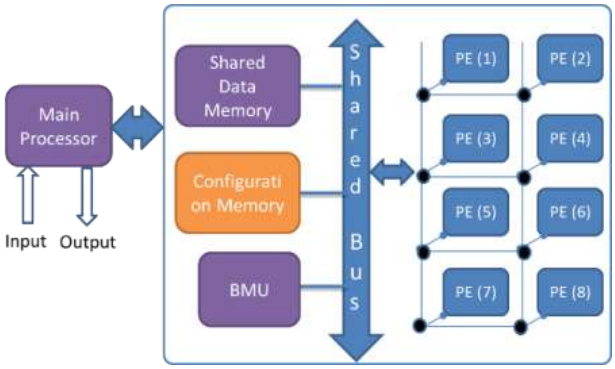

Figure 1: Block architecture Modified.

IV. Applications

1. A It will be used in media processing.
2. I/O intensive applications.
3. In many applications for improving the lifetime of SSDs up to 33%.
4. they can be added to ReCA to maintain its workload generality.
5. eDRAM (embedded DRAM) .
6. NVRAM (non-volatile RAM) .

V. Challenges

The cache architecture has been studied using simulation in the last years and chip-multiprocessor has also been addressed. We follow this traditional approach, but conduct an investigation by studying the adaptivity between cache performance and cache organization.

VI. Conclusion

The highlights of the research can be seen that due to different applications the utilization of the reconfigurable fabric plays a crucial role that depends on the type of reconfigurable structure deployed. The switch over from custom instruction to a fine grain system provides for reconfigurable area on the same core along with memory bandwidth but the reconfiguration is scheduling specific where ideal state cannot be utilized to balance out the hardwired kernel programs. As the application becomes dynamic larger share of resources can be conquered by the shared resource reconfigurable approach where the core fabric can be utilized to the maximum because of sharing and a soft deadline preemptive algorithm. The goal was to reduce the underutilization which we have achieved by custom instruction being implemented by inherent parallelism provided by MMU controlling the cache.

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