IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
Vol. 09, Issue 5 (May. 2019), ||S (IX) || PP 010-14

Design and Analysis of 6T, 8T, 10T SRAMS

Shamal Mahalle[1], Prof. Anil Bawaskar[2], Prof. Parinay Lavatre[3],
(PG Student, Department of Electronics and Telecomm Engg ,VLSI ,JIT ,Nagpur)
(Project Guide, Assistant Professor ,Dept of E&TC Engg ,VLSI , JIT ,Nagpur)
(Co-Guide,Assistant Professor ,Dept of E&TC Engg , VLSI , JIT ,Nagpur)

***Abstract*:** *In modern era, the demand for memory has been increases tremendously. Due to reduction in SRAM operating voltage, cell stability degradation and the increase in process variation with process scaling. The main issue in VLSI design are optimizing speed, scaling in silicon technology and increased packing density. These issues account for increased power dissipation in SoC (System on Chips) making them unsuitable for portable operations. Since SRAM consist of almost 60% of VLSI circuits, hence, it is needed that a low power SRAM design to maximize the run time with minimum requirements on size, battery life and weight allotted to batteries. In this paper the basic operation of SRAM along with techniques to reduce total power dissipation are discussed.*

Keywords: *SRAM , 6T , 8T , 10T .*

I. Introduction

POWER dissipation has become a first class design constraint as we have hit the utilization wall, and the low power circuit, architecture, and system level techniques are sought out. In addition, the static random access memory (SRAM) is the most important digital macro and its portion on a system-on-chip(SoC) is ever increasing .Decreasing the power dissipation of SRAM will not only lower the overall system power dissipation, but will also increase the yield and improve the SoC reliability. Although the six transistor (6T) SRAM cell is a widely used standard in industry, it has its own limitations. 6T SRAM not only has conflicting read and write requirements, it also has read static noise margin (RSNM) degradation. The most important factors to consider in the design of SRAM in Modern nanometer technologies are the: 1) read stability;2)write stability; 3) cell supply reduction;4) power dissipation;5) leakage currents; 6) bitline (BL) *I*ON to *I*OFF ratio; and7) variability [6].With increasing process variations, achieving specific yield is getting difficult, and novel designs and techniques, including read and write assist circuits, are adopted at the cost of area, power dissipation, or speed to improve the read/write stability and increase the number of cells in a single column . Reduction of the supply voltage is the most straightforward technique to reduce the active power dissipation. However, 6T SRAM power supply cannot be reduced aggressively due to its RSNM degradation. Many SRAM cell have been proposed that improve RSNM, including single ended (SE) 8T ,9T, 10T, and differential 7T ,8T , 9T , and 10T . Also, numerous SRAM assist techniques have been described in the literature as a cost-effective method to increase the write margin, and lower the leakage power dissipation compared to bit cell transistor upsizing or operating the memory array at a higher supply voltage.

II. Literature survey

Static random access memory (SRAM) is a static memory cell which is widely used in various electronic systems. It is faster and consumes less power as compared to other memory cells . It does not require refreshing periodically. Because of this, SRAM is the most popular memory cell among VLSI designers. Hence continuous evolution goes on for higher performance of SRAM cells. Due to this, different types of SRAM cells are available in the literature like 6T SRAM cell, 7T SRAM cell, 8T SRAM cell, 9T SRAM cell etc. Most common SRAM cells used in digital system is the 6T SRAM cell. This cell can store 1-bit of data. The bit remains within the cell as long as power is equipped. In this paper, design and performance analysis of a 6T SRAM cell is discussed. Recently, Static random access memory (SRAM) is used in a large variety of consumer electronics, such as computers and cellular phones. SRAM needs no refreshing and can maintain its data as long because it has adequate power equipped. This is thanks to the actual fact that the SRAM cell includes flip-flop electronic equipment internally that doesn't need refreshing. However, it's apparent that SRAM suffers from the disadvantage of counting on too several transistors. Accordingly, there is an important need to have an SRAM cell that requires fewer than six transistors. An SRAM cell has 3 modes of operation, namely read, write and standby . The data stored in the cells may be corrupted when the cells are read. This drawback arises from the actual fact that the next voltage on the bit line is coupled to a lower voltage within the cell, inflicting the bit line

voltage to drop and the cell voltage to rise. Further, a priority related to the write operation is that it's comparatively tough to jot down a logic '1' to the cell if the cell presently stores a logic '0'. Accordingly, the SRAM cell ought to offer less doubtless to be corrupted once the cell is browse and additional reliable once the cell is written. As integrated circuits become smaller and denser and as power consumption specifications for battery powered integrated circuits decrease, along with power supply voltages, the present SRAM cell designs are increasingly inefficient in each element space used and power consumed. Memories take up eightieth of the die space in high performance processors. Therefore, there's an important would like for a coffee run and extremely strong SRAM style. Leakage current from a memory cell will cause supererogatory power consumption, especially during a standby mode. Recent analysis has shown that the run current can become even larger than the dynamic current within the overall power consumption . Typically, there area unit 3 major sources of run in a very MOS semiconductor device, namely subthreshold leakage, gate leakage, and reverse bias junction leakage . Amongst them, Gate-Induced drain leakage (GIDL) is an unwanted short-channel effect that occurs at higher drain biases in an overdriven off state of a MOS transistor. The GIDL is the result of a deep depletion region that forms in the drain at high drain-to-gate biases. However, Drain induced barrier lowering (DIBL) may be a short-channel impact in MOS semiconductor devices referring originally to a discount of threshold voltage of the transistor at higher drain voltages. With lowering of the MOS semiconductor device, each of the leakage sources may increase accordingly, thus resulting in the increase of the total leakage current. As CMOS technology scales right down to ninety nm and below, the power consumption caused by leakage currents is becoming a significant part of the global power consumption . Therefore, it'd clearly be fascinating to produce a style for AN SRAM cell that has less run current than ancient styles once the cell in standby.

III. Proposed Circuit Digrams

3.1 6T SRAM

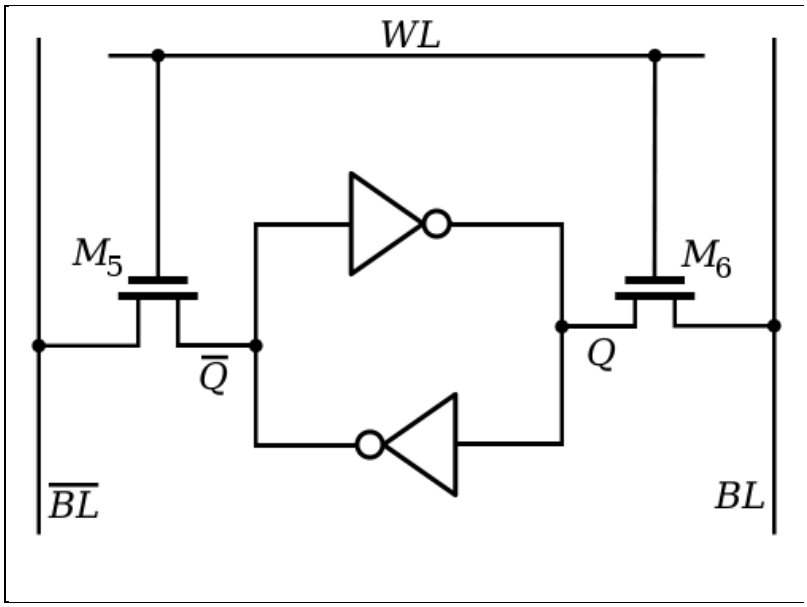

Fig.1. 6T SRAM

3.2 8T SRAM

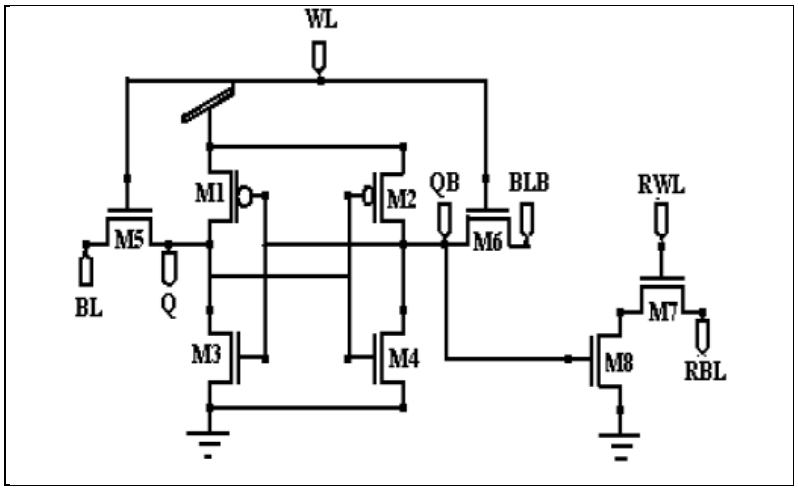

Fig.2. 8T SRAM

3.3 10T SRAM

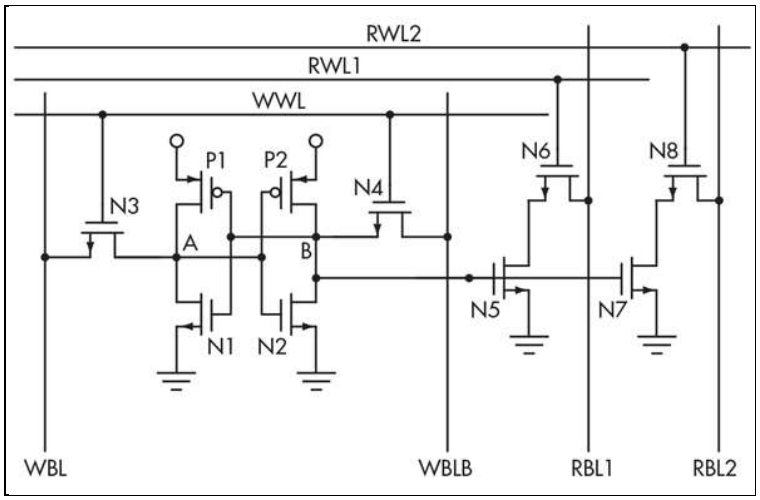

Fig.3. 10T SRAM

IV. Design Of Srams

Various SRAM are design and their waveform are observed. 6T,8T,10T SRAM are design in TANNER S-edit tool ,Where as the waveform are analyse .All SRAM are perform their operation during read and write mode.

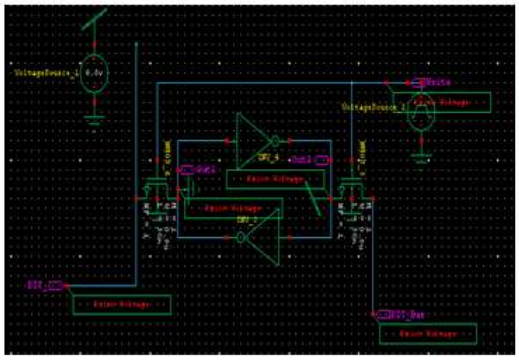

Fig .4 .6T SRAM schematic during read mode

Fig.5 . 6T SRAM read operation waveform

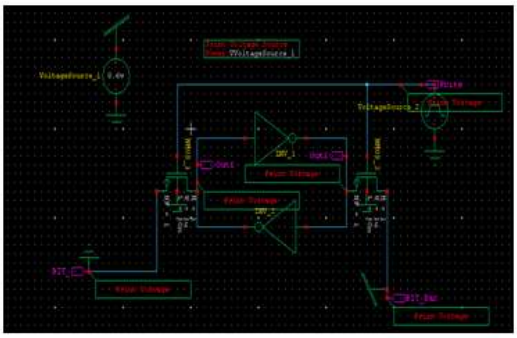

Fig 6 .6T SRAM schematic during write mode

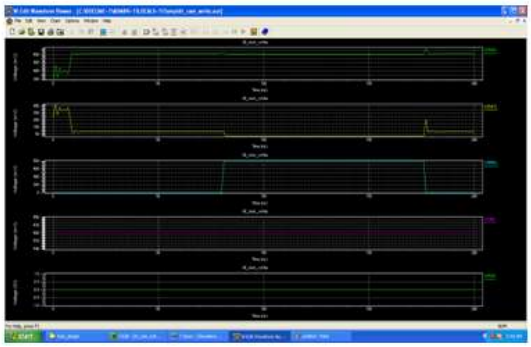

Fig.7. 6T SRAM write operation waveform

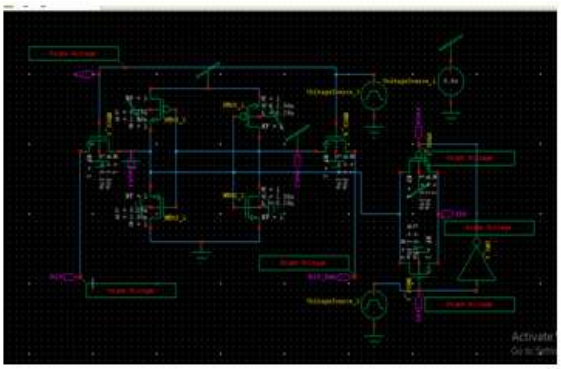

Fig 8 .8T SRAM Schematic during read mode

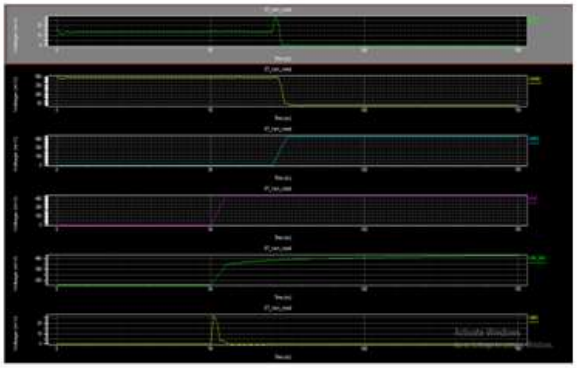

Fig.9 . 8T SRAM read operation Waveform

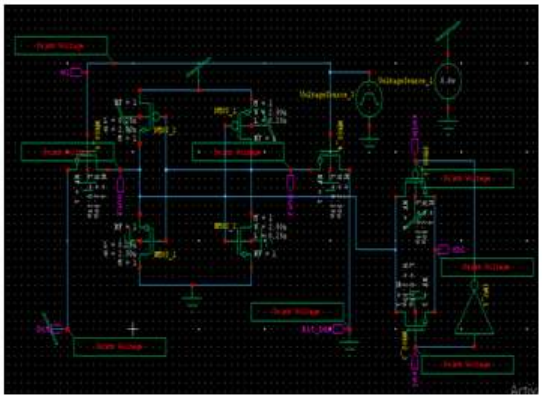

Fig.10. 8T SRAM Write Schematic

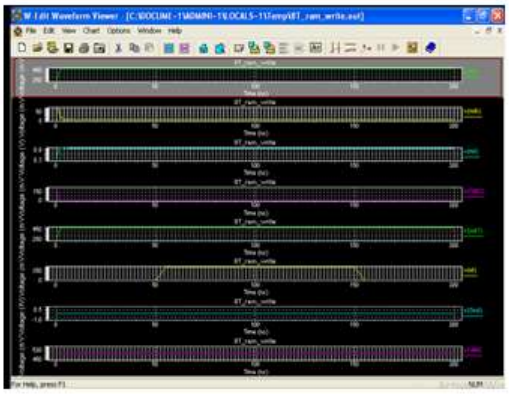

Fig.11. 8T SRAM Write operation Waveform

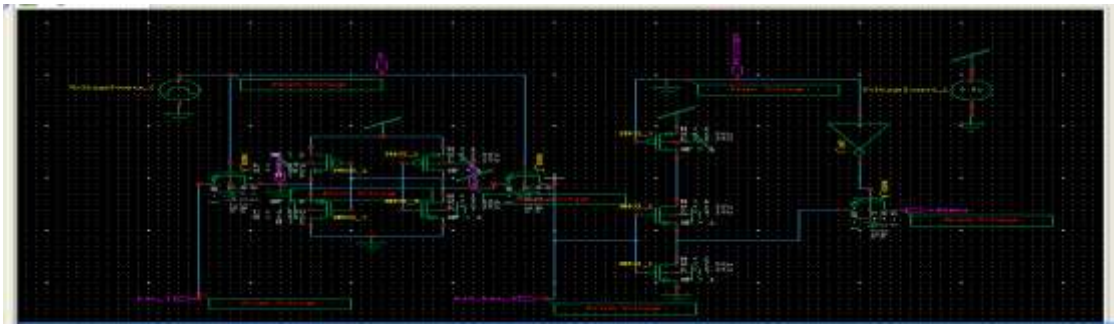

Fig 12 10T SRAM schematic of read operation

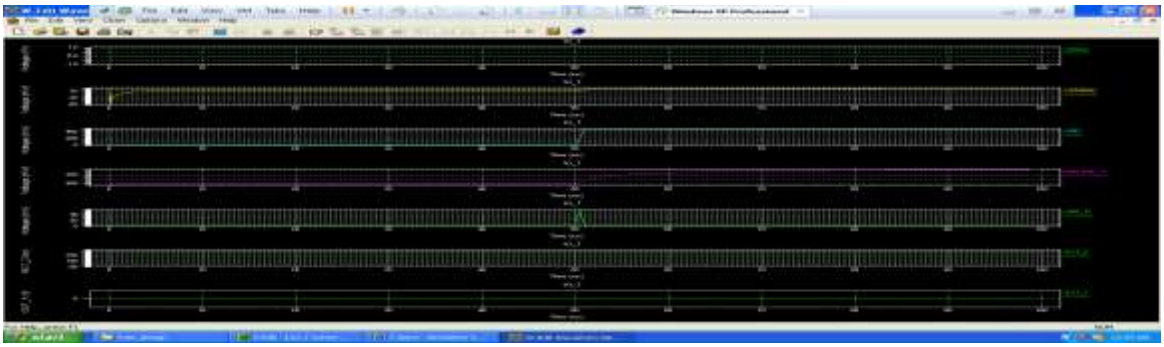

Fig 13 10T SRAM read operation waveform.

V. Results

Sr. No.	RAM	Average Power(Watt)	Average Current(Amp)
1	6T Read	15.70112n	31.40224n
2	6T Write	2.49962u	4.99924u
3	8T Read	20.32869n	40.65738n
4	8T Write	2.90857u	5.81713u
5	10T Read	259.75172n	519.50344n
6	10T Write	3.55760u	7.11520u

TABLE: I DEPICTS THE AVERAGE POWER AND AVERAGE CURRENT OF VARIOUS SRAM.

VI. Conclusion

Average power and average current of different SRAM are calculated and studied .The 10 T SRAM during write operation consumes less power as 3.5576uW compared to the other SRAM during write operation .During read operation 8T SRAM consumes less power as 2.90uW.The performance of each SRAM are studied and obtained their waveform.

References

[1]. 1.Chien-Cheng Yu and Ming-ChuenShiau, "*SINGLE-PORT FIVE-TRANSISTOR SRAM CELL WITH REDUCED LEAKAGE CURRENT IN STANDBY*" International Journal of VLSI design & Communication Systems (VLSICS) Vol.7, No.4, August 2016.

[2]. Arash Azizi Mazreaht, Mohammad TaghiManzuriShalmani , Reza Noormande, Ali Mehrparvar, "*A Novel Zero-Aware Read-Static-Noise-Margin-Free SRAM Cell for High Density and High Speed Cache Application"* ©2008 IEEE

[3]. Michael Wieckowski, Martin Margala,"*A NOVEL FIVE-TRANSISTOR (5T) SRAM CELL FOR HIGH PERFORMANCE CACHE*" ©2005 IEEE.

[4]. Shyam Akashe, Sushi I Bhushan "*High Density and Low Leakage Current Based 5T SRAM Cell Using 45 nrn Technology*" @2011 IEEE

[5]. Satyanand Nalam and Benton H. Calhoun, "*Asymmetric Sizing in a 45nm 5T SRAM to Improve Read Stability over 6T*" ©2009 IEEE.

[6]. M. C. Shiau and E. G. Chang, "5T single port SRAM", TW pat. I436359 B, May 1, 2014.

[7]. M. C. Shiau, C. C. Yu, and K. T. Chen, "Single port SRAM with reducing standby current", TW pat. I425510 B, Feb. 1, 2014.

[8]. M. C. Shiau and W. C. Tsai, "Single port SRAM having a discharging path", TW pat. I41916 B, Dec.11, 2013

[9]. Carlson, S. Andersson, S. Natarajan, and A. lvandpour, "A high density, low leakage, 5T SRAM for embedded caches," in Proc. ESSCIRC 2004, Sept. 2004, pp. 215-218.