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An Overview: Design and Analysis of SRAMS

Shamal Mahalle[1], Prof. Anil Bawaskar[2], Prof. Parinay Lavatre[3],
(PG Student, Department of Electronics and Telecomm Engg ,VLSI ,JIT ,Nagpur)
(Project Guide, Assistant Professor ,Dept of E&TC Engg ,VLSI , JIT ,Nagpur)
(Co-Guide,Assistant Professor ,Dept of E&TC Engg , VLSI , JIT ,Nagpur)

Abstract**:** *In modern era, the demand for memory has been increases tremendously. Due to reduction in SRAM operating voltage, cell stability degradation and the increase in process variation with process scaling. The main issue in VLSI design are optimizing speed, scaling in silicon technology and increased packing density. These issues account for increased power dissipation in SoC (System on Chips) making them unsuitable for portable operations. Since SRAM consist of almost 60% of VLSI circuits, hence, it is needed that a low power SRAM design to maximize the run time with minimum requirements on size, battery life and weight allotted to batteries. In this paper the basic operation of SRAM along with techniques to reduce total power dissipation are discussed.*

Keywords: *SoC , SRAM ,VLSI,CMOS.*

I. Introduction

POWER dissipation has become a first class design constraint as we have hit the utilization wall, and the low power circuit, architecture, and system level techniques are sought out. In addition, the static random access memory (SRAM) is the most important digital macro and its portion on a system-on-chip(SoC) is ever increasing.Decreasing the power dissipation of SRAM will not only lower the overall system power dissipation, but will also increase the yield and improve the SoC reliability. Although the six transistor (6T) SRAM cell is a widely usedstandard in industry, it has its own limitations. 6T SRAMnot only has conflicting read and write requirements, it alsohas read static noise margin (RSNM) degradation. The mostimportant factors to consider in the design of SRAM in Modern nanometer technologies are the: 1) read stability;2)writestability; 3) cell supply reduction;4) power dissipation;5) leakage currents; 6) bitline (BL) *I*ON to *I*OFF ratio; and7) variability [6].With increasing process variations, achieving specific yield is getting difficult, and novel designs and techniques, including read and write assist circuits, are adopted at the cost of area, power dissipation, or speed to improve the read/write stability and increase the number of cells in a single column .Reduction of the supply voltage is the most straight forward technique to reduce the active power dissipation. However, 6T SRAM power supply cannot be reduced aggressively due to its RSNM degradation. Many SRAM cell have been proposed that improve RSNM, including single ended (SE) 8T ,9T, 10T, and differential 7T ,8T , 9T , and 10T . Also, numerous SRAM assist techniques have been described in the literature as acost-effective method to increase the write margin, and lower the leakage power dissipation compared to bitcell transistorupsizing or operating the memory array at a higher supply voltage .

II. Literature Survey

[Paper 1]*Chien-Cheng Yu and Ming-ChuenShiau, "SINGLE-PORT FIVE-TRANSISTOR SRAM CELL WITH REDUCED LEAKAGE CURRENT IN STANDBY" International Journal of VLSI design & Communication Systems (VLSICS) Vol.7, No.4, August 2016*

A new single-port five-transistor (5T) Static Random Access Memory (SRAM) cell with integrated read/write assist is proposed. Amongst the assist circuitry, a voltage control circuit is coupled to the sources corresponding to driver transistors of each row memory cells. This configuration is aimed to control the source voltages of driver transistors under different operating modes.

[Paper 2]*ArashAziziMazreaht, Mohammad TaghiManzuriShalmani , Reza Noormande, Ali Mehrparvar, "A NOVEL ZERO-AWARE READ-STATIC-NOISE-MARGIN-FREE SRAM CELL FORHIGH DENSITY AND HIGH SPEE*D CACHE APPLICATION" ©2008 IEEE

The newly developed CMOS five-transistor SRAM cell uses one word-line and one bit-line during read/write operation. This cell retains its data with leakage current and positive feedback without refresh cycle. The new cell size is 18% smaller than a conventional six-transistor SRAM cell using same design rules. Simulation result in standard 0.25J.1m CMOS technology shows purposed cell has correct operation during read/write and idle mode. The average delay of new cell is 20% smaller than a six-transistor SRAM cell.

[Paper 3] *Michael Wieckowski, Martin Margala,"A NOVEL FIVE-TRANSISTOR (5T) SRAM CELL FOR HIGH PERFORMANCE CACHE" ©2005 IEEE*

A novel five-transistor (5T) static memory cell is presented for applications in high-speed, low-power cache. The 5T design in 0.18pm bulk CMOS exhibits 57% faster operation speed, a 12% reduction in power, and a 6% reduction in area with respect to the standard 6T cell design.

[Paper 4]*ShyamAkashe, Sushi I Bhushan "HIGH DENSITY AND LOW LEAKAGE CURRENT BASED 10T SRAM CELL USING 45 NRN TECHNOLOGY" @2011 IEEE*

This paper is based on the observation of a CMOS five-transistor SRAM cell (5T SRAM cell) for very high density and low power applications. This cell retains its data with leakage current and positive feedback without refresh cycle. This 5T SRAM cell uses one word-line and one bit-line and extra redline control. The new cell size is 21.66% smaller than a conventional six-transistor SRAM cell using same design rules with no performance degradation.

[Paper 5]*NaeemMaroof and Bai-Sun Kong, IEEE, "10T SRAM USING HALF-VDD PRECHARGE AND ROW-WISE DYNAMICALLY POWERED READ PORT FOR LOW SWITCHING POWER AND ULTRALOW RBL LEAKAGE" ©2017 IEEE.*

In this paper a new 10T staticrandom access memory cell having single ended decoupled RBL with a 4T read port for low power operationand leakage reduction is proposed. RBLincreases toward the *V*DD level for a read-1, and dischargestoward the ground level for a read-0. The proposed 10T cellin a commercial 65 nm technology is 2.47× the size of 6T with

$\beta = 2$, provides 2.3× read static noise margin, and reduces theread power dissipation by 50% than that of 6T.

III. Proposed Methadology

3.1 6T SRAM CELL

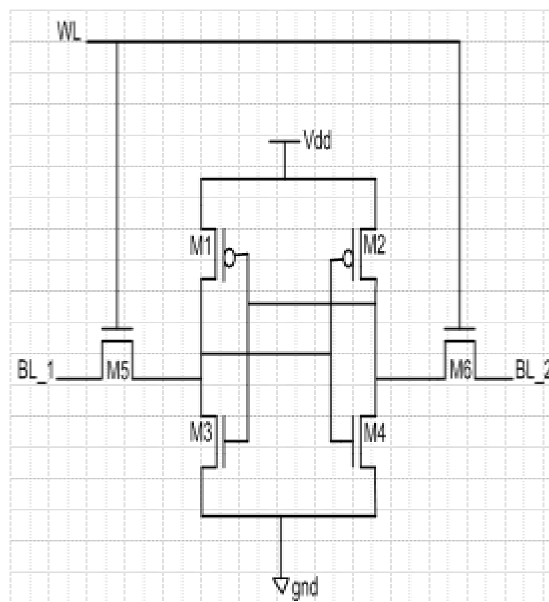

Figure 1 Conventional 6T SRAM cell

The SRAM cell is the key component for storing the binary information. By the employment of 2 cross-coupled inverters, a typical SRAM cell forms a latch and access transistors. The access transistors modify access to the cell throughout browse and write operations and supply cell isolation throughout the not-accessed state. SRAM cell is intended to produce write capability, non-destructive read access and data storage (or data retention) for as long as cell is powered. The design and analysis of different SRAM cells are: Conventional 6T, 7T, 8T, 9T and improved 6T. They are compared with respect to power, delay and speed. Generally, the cell design must strike a balance between cell area, speed, robustness, leakage and yield. One of the most important design objectives is power reduction. However, power cannot be reduced indefinitely without compromising the other parameters. As an example, low-power can compromise the cell area and also the speed of operations. The thought six-transistor (6T) CMOS SRAM cell is shown in Figure -1, here four transistors (M1−M4) comprise cross-coupled CMOS inverters and two NMOS transistors M5 and M6 provide read and write access to the cell.

The most well-liked SRAM cell may be a 6T CMOS SRAM cell because of its superior hardiness, low-voltage and low power operation

3.2 8T SRAM CELL

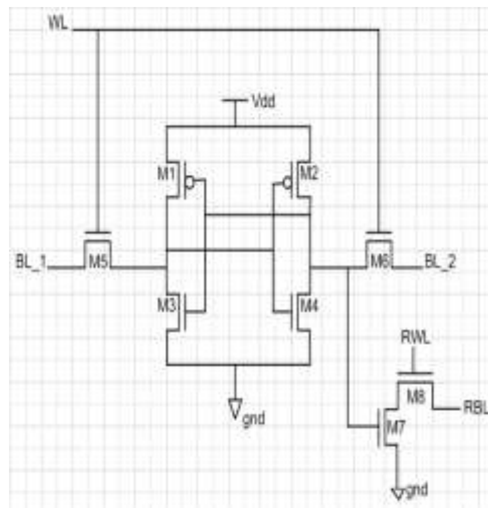

Figure 2 8T SRAM cell

The 8T SRAM circuit is presented in this section. The schematic of the 8T SRAM cell sized for associate degree 180nm CMOS technology is shown in Figure five. The left sub-circuit of the 8T memory cell is a conventional 6T SRAM cell with minimum sized devices (composed of M1, M2, M3, M4, M5, and M6). Two data access transistors (M5 and M6) andtwo bit lines (BL_1 and BL_2) are used for writing to the SRAM cell. An alternative communication channel (composed of a separate read bit line RBL and the transistor stack formed byM7 and M8) is used for reading the data from the cell. Two separate control signals RWL and WL are used for controlling the read and the write operations, respectively, with the 8T SRAM circuit as shown in Figure 5. During a read operation, the read signal RWL transitions to VDD while the write signal WL is maintained at VGND. The browse bit line (RBL) is not absolutely discharged supported the information keep within the SRAM cell. The storage nodes (Node1 and Node2) are completely isolated from the bit lines during a read operation. The data stability is thereby significantly enhanced as compared to the conventional 6T SRAM cells.

3.3 10T SRAM CELL

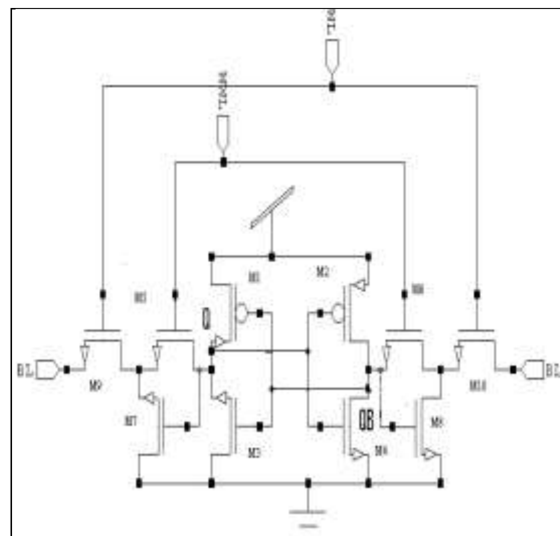

Figure 3 . 10T SRAM cell

IV. Parameters For Simulation And Results

The Simulation and results of the improved 8T SRAM cell is given in Table one. In the following subsections, three important metrics of an SRAM design: Static noise margins, power, and delays are explaining.

4.1 STATIC-NOISE-MARGIN (SNM)

The stability of SRAM circuit depends on the Static Noise Margin. The basic SNM is obtained by drawing and mirroring the electrical converter characteristics and finding the most attainable sq. between them. It is a graphical technique of estimating the SNM

4.2- POWER CONSUMPTION

The power consumption of Static Random Access Memory cell depends on consumption of the power which used to perform the operation of the transistor. Dynamic power consumption in SRAMs is consumed due to the charging and discharging capacitances during read and write operation and during each cycle of SRAM particular amount of Energy is drawn from the power supply and dissipated. For each cycle the power consumption is depended on the type of operation (read or write). Also, when the capacitor charged from GND to VDD and then discharged VDD to GND, the amount of energy drawn from the power supply and dissipated equals CLVDD2. The stored energy on the capacitor CL with voltage VC equals ½ CLVC2. Therefore, each time the capacitor CL is charged from VC to VDD and then discharged VDD to VC .A average power dissipation of any device over one period can be obtained by following expression

. Pav = [(1/T) 0∫T I dt] × V

V. Applications

Memory is a necessary part of soo many devices .They are widely used in so many devices .SRAM most common use is in the cache memory .SRAMS are used in various categories such as industrial and scientific subsystems, automotive electronics, and similar systems. SRAMS are used in defence equipments as well.SRAMS are used in medical field.

References

[1]. Chien-Cheng Yu and Ming-ChuenShiau, "*SINGLE-PORT FIVE-TRANSISTOR SRAM CELL WITH REDUCED LEAKAGE CURRENT IN STANDBY*" International Journal of VLSI design & Communication Systems (VLSICS) Vol.7, No.4, August 2016.

[2]. Arash Azizi Mazreaht, Mohammad TaghiManzuriShalmani , Reza Noormande, Ali Mehrparvar, "*A Novel Zero-Aware Read-Static-Noise-Margin-Free SRAM Cell for High Density and High Speed Cache Application"* ©2008 IEEE

[3]. Michael Wieckowski, Martin Margala,"*A NOVEL FIVE-TRANSISTOR (5T) SRAM CELL FOR HIGH PERFORMANCE CACHE*" ©2005 IEEE.

[4]. Shyam Akashe, Sushi I Bhushan "*High Density and Low Leakage Current Based 5T SRAM Cell Using 45 nrn Technology*" @2011 IEEE

[5]. Satyanand Nalam and Benton H. Calhoun, "*Asymmetric Sizing in a 45nm 5T SRAM to Improve Read Stability over 6T*" ©2009 IEEE.

[6]. M. C. Shiau and E. G. Chang, "5T single port SRAM", TW pat. I436359 B, May 1, 2014.

[7]. M. C. Shiau, C. C. Yu, and K. T. Chen, "Single port SRAM with reducing standby current", TW pat. I425510 B, Feb. 1, 2014.

[8]. M. C. Shiau and W. C. Tsai, "Single port SRAM having a discharging path", TW pat. I41916 B, Dec.11, 2013

[9]. Carlson, S. Andersson, S. Natarajan, and A. lvandpour, "A high density, low leakage, 5T SRAM for embedded caches," in Proc. ESSCIRC 2004, Sept. 2004, pp. 215-218.