IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
Vol. 09, Issue 7 (July. 2019), ||S (I) || PP 59-64

Study of variability issues on CMOS inverter

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Abstract*:* This paper studies the impact of performance and variability effects on CMOS inverter circuits. Device mismatches, the small random variations in the characteristics of identically designed devices, occur during the manufacturing of integrated circuits. These mismatches result in behavioral variations of analog and digital integrated circuits. The impact of these random parameter variations on circuit behavior can be studied with Monte Carlo simulation by analyzing a large set of circuit instantiations with randomly varied devices and process parameters.

Keywords: process; mismatch; MOSFET; Monte-Carlo simulation

Date of Submission: 03-07-2019 Date of acceptance: 18-07-2019

I. INTRODUCTION

The basic CMOS inverter is the nucleus of all digital designs. Complex structures such as NAND gates, adders, multipliers, and processors can be easily designed if the operation of an inverter is well understood. The electrical behavior obtained from a CMOS inverter can be extrapolated to obtain the characteristics of these complex circuits. The analysis of inverters can be extended to explain the behavior of more complex gates such as NAND, NOR, or XOR, which in turn form the building blocks for modules such as multipliers and processors. Therefore this paper focuses on study of inverter and its performance and variability effects.

The paper is organized as follows. Section II describes the methodology adopted. Section III discuss about the variability effects and various obtained results and section IV concludes the paper.

II. METHODOLOGY

This study involves analysis of CMOS inverter circuit and obtaining the transient and DC characteristics. The inverter output signal rise time, fall time and delay calculation also performed. The CMOS circuit shown in figure 1 is simulated using Cadence Virtuoso tool, using the gpdk 180nm technology.

The static CMOS inverter offers almost ideal VTC— symmetrical shape, full logic swing, superior noise margins and high robustness, which makes the circuit a major attraction in the design process. Also the static CMOS consumes no power in the steady-state operation. It is this combination of robustness and low static power that has made static CMOS the technology of choice of most contemporary digital designs. The power dissipation of a CMOS circuit is instead dominated by the dynamic dissipation resulting from charging and discharging capacitances.

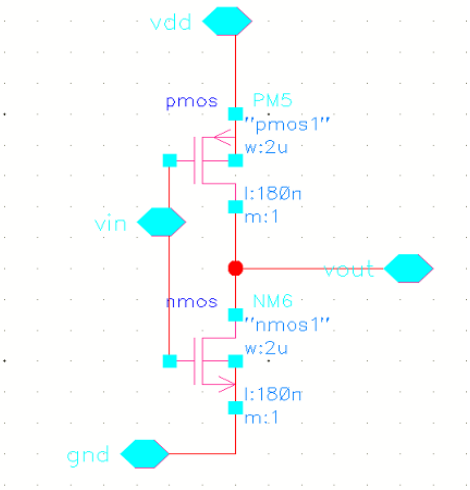

Figure 1: Schematic of CMOS inverter

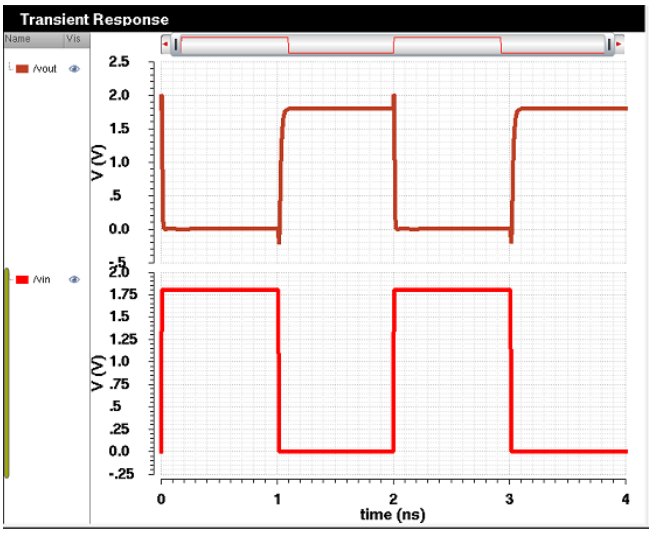

Figure 2: Transient response of CMOS inverter

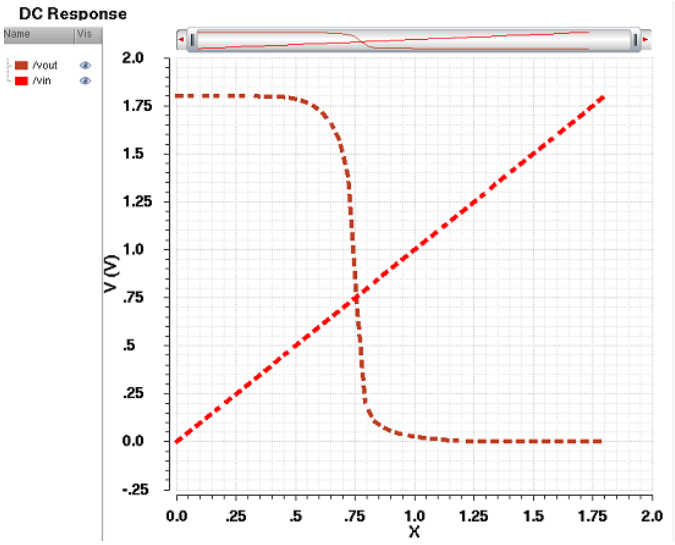

Figure 3: CMOS Inverter DC response

Table Of Outputs

	Name/Signal/Expr	Value	Plot	Save
1	vout		yes	allv
2	vin		yes	allv
3	risetime	19.5599p		
4	falltime	19.5599p		
5	delay	9.20812p		

Figure 4: Inverter parameter calculations

The figures 2 and 3 shows the near ideal characteristics of CMOS inverter as expected. The switching threshold of the inverter can be varied by changing the Wp/Wn ratio of the transistors. The rise time, fall time and delay calculations are carried out using the calculator tool in Cadence and are shown in figure 4.

III. VARIABILTY STUDY

Another important design consideration in digital circuit is the process variability. Here the basic inverter circuit is considered to study the effect of process and device mismatches on the inverter circuit. Mismatch means the difference in the value of a device parameter among identically designed devices. The

methodology involves, performing Monte-Carlo simulations on the CMOS circuit for various operating conditions. Monte Carlo analysis is based on statistical distributions and it simulates the effect of device mismatches and process variation in a more realistic way. Here the study considered 20 samples.

A) EFFECT OF PROCESS VARIATION

The study involves the analysis of the variation in the rise time, fall time and delay of CMOS inverter and the obtained histograms are shown in figures 5 to 8.

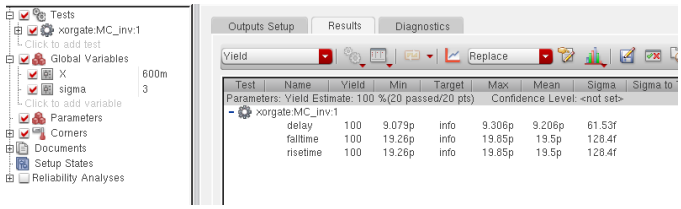

Figure 5: Monte Carlo result for process variation

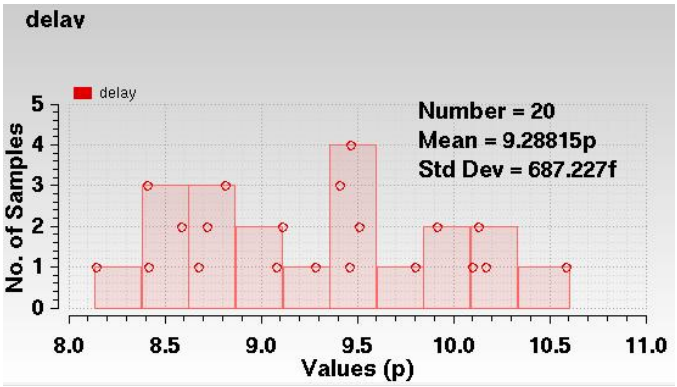

Figure 6: Delay variations due to process

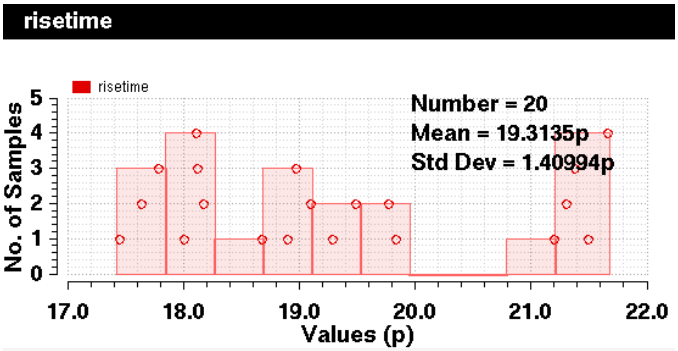

Figure 7: Rise time variations due to process

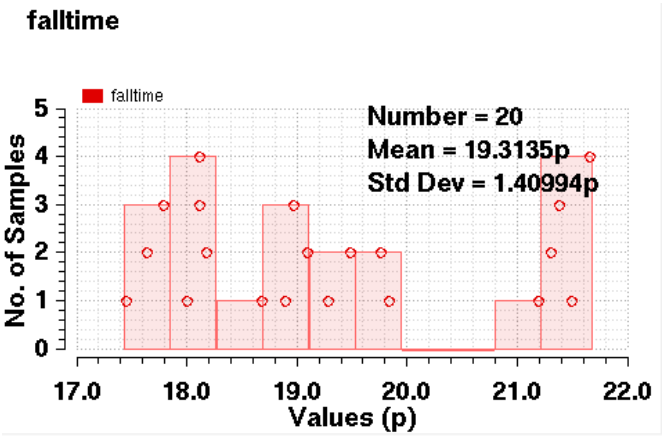

Figure 8: Fall time variations due to process

B) EFFCET OF DEVICE MISMATCHES

Here the variations in the rise time, fall time and delay of CMOS inverter due to mismatch between the transistors are obtained and shown in figures 9 to 12.

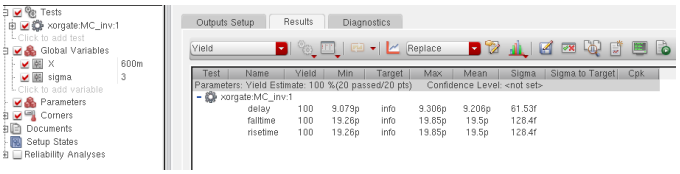

Figure 9: Monte Carlo result for device mismatch

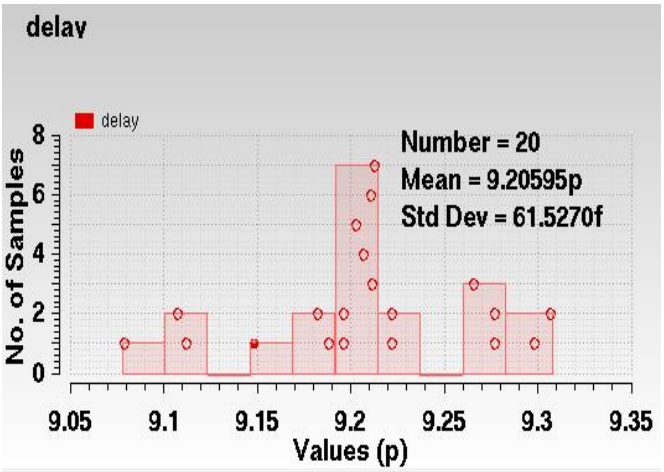

Figure 10: Delay variations due to mismatch

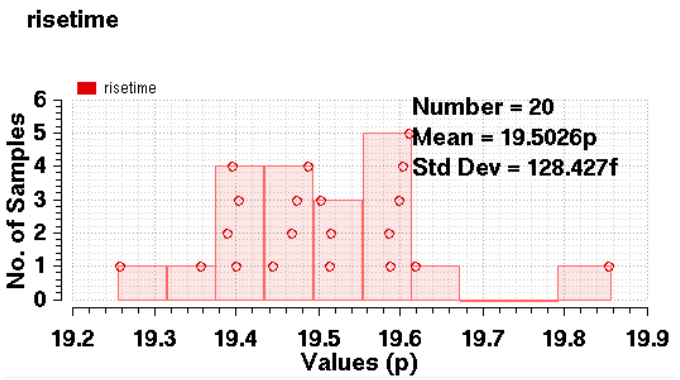

Figure 11: Risetime variations due to mismatch

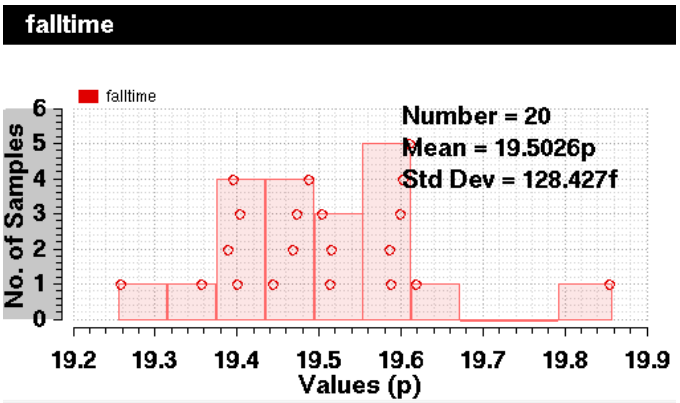

Figure 12: Fall time variations due to mismatch

C) COMBINED EFFECT OF PROCESS AND MISMATCH

The following figures 13 to 15 show the effect on CMOS inverter parameters due to mismatch between the transistors and process considered together.

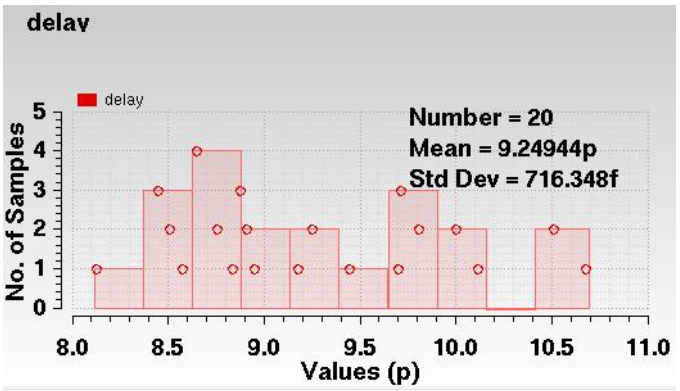

Figure 13: Delay variation due to both process and mismatch

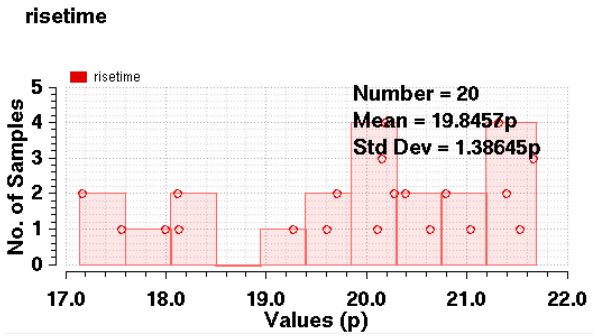

Figure 14: Rise time variation due to both process and mismatch

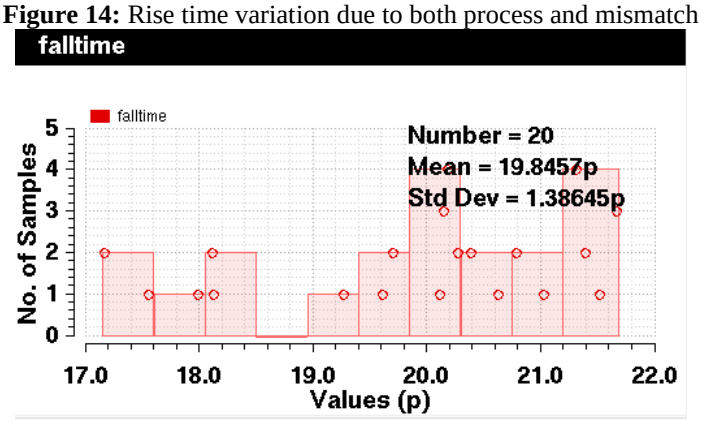

Figure 15: Fall time variation due to both process and mismatch

IV. RESULTS AND CONCLUSION

The study carried out reinstates the fact that variations of process and mismatch is affecting the circuit parameters. This affects the performance of CMOS digital circuits. But process varaition

As the amount of process variation becomes more pronounced at smaller process nodes, there is an increasing demand for extensive study on variabilty effects in the advanced technology nodes. Therefore the future work involves study of process variabity effects on FINFET devices using Monte-Carlo analysis.

REFERENCES

[1]. A. Islam, A. Imran, M. Hasan, "Variability Analysis and FinFET-based Design of XOR and XNOR Circuit", in Int. Conf. on Computer & Communication Technology, 2011, pp. (239- 245).

[2]. M. J. Pelgrom et al, "Matching Properties of MOS Transistors", IEEE JSSC,Vol.24,No.5,pp.1433-1439,Oct.1989.

[3]. K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," IEEE Journal of Solid-State Circuits 21, no. 6 (1986):1057–1066.
[4]. A. Asenov, "Simulation of statistical variability in nano MOSFETs," IEEE Symp. VLSI Technol., Dig. Tech. Papers, Jun. 2007, pp. 86–87.
[5]. C. G. Dieseldorff, C. Tseng, "Technology Node Transitions Slowing Below 32nm," Industry Research & Statistics, SEMI.org, June 2014.

Neethu Johny. "Study of variability issues on CMOS inverter." IOSR Journal of Engineering (IOSRJEN), vol. 09, no. 07, 2019, pp. 59-64.