

# DESIGN OF DDS WITH OPTIMIZATION TECHNIQUES AND IMPLEMENTATION IN FPGA

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**Abstract**—This paper presents an analysis of a Direct Digital Synthesizer (DDS) using various optimization techniques to achieve high-frequency waveform generation. Enhanced waveforms with multiple parameters are simulated in MATLAB SIMULINK and implemented on an FPGA board. The principles of DDS, along with its structural schematic model, are outlined. This approach enables the synthesis of signals with precise frequency generation and phase modulation across a frequency range of up to 200 MHz, making it suitable for diverse applications. Additionally, a PN sequence method is introduced to improve model accuracy by adjusting phase values. The DDS system, incorporating various optimization techniques, undergoes parameter analysis to ensure accurate signal generation. Fast Fourier Transform (FFT) analysis of the signals reveals low total harmonic distortion, achieved through these optimization methods. This work highlights the significance of advancements in DDS technology in enhancing signal processing efficiency across multiple fields.

**Index Terms**—direct digital synthesis; direct digital synthesizers; digital frequency synthesizers; DAC; low-pass filter; function generator code-sine; digital frequency accumulator; digital phase accumulator; level of amplitude noises; phase noise, total harmonic distortion.

## I. INTRODUCTION

Direct Digital Frequency Synthesizers (DDFS) have been used in digital communication systems to create wave signals. DDS have several characteristics that make them preferable over analog Phase-Locked Loops (PLLs), including fast continuous switching, fine frequency resolution, the ability to operate over a large frequency range, and high spectral purity [1]. Most Direct Digital Synthesizers are based on a structure first proposed by Tierney, Rader, and Gold in 1971. The structure of a DDS consists of two primary components: a phase accumulator and a sine or cosine mapping function (SCMF). The phase accumulator consists of an N-bit adder and a register. The frequency tuning word, M, controls the sampling of data at a given constant value, which determines the output frequency. The N-bit output of the phase accumulator is truncated to generate data, which serves as input to the SCMF. The size of the lookup table grows exponentially with the number of bits N. The number of data points in the lookup table is (2 power

18) +1. The internal prioritization of the lookup table relies primarily on precision. Consequently, significant research has been conducted over the last 40 years to reduce the size of lookup tables. FPGAs are increasingly popular for implementing digital circuits, despite the significant clock speed reduction and power overhead compared to ASIC designs in the same process. FPGA-based DDS technology is used to generate wave signals with specified frequency and phase. The feasibility and simulation results of the designed signal generator were produced using VIVADO simulation software. Signal generators have evolved significantly with the rapid advancement of modern technology in electronics, from simple signals to high-speed arbitrary signals. With the adoption of digital technology in instruments and communication systems, direct digital frequency synthesizers were developed [2] [3]. Direct digital frequency synthesis is a type of frequency synthesis in which the target waveform is synthesized directly from the phase angle. To improve spur reduction and reduce memory usage, dithering techniques are applied, implemented in MATLAB SIMULINK using a PN Sequence Generator. In telecommunications, aerospace, instrumentation, and other fields, frequency synthesis technology is widely used. Today, direct, phase-locked, and direct digital methods are primarily used to synthesize frequency [4]. Direct digital frequency synthesis is a modern frequency synthesis technique that allows for waveforms to be synthesized directly from the phase of signals using fast frequency tuning [5] [6].

## II. DIRECT DIGITAL SYNTHESIZER

### A. Principle of Direct Digital Synthesizer

The main part of a DDS is a digital phase accumulator. This accumulator determines the phase information of the signal being generated. At a particular clock signal the phase of the signal is incremented intermediately. The increment of the phase is based on the constant value. The constant value is given manually which helps to determine the needed intervals to collect the data, regenerate and resample. The output is continuous digital signal of the desired output frequency. The phase accumulator consists of an N-bit adder and register. The

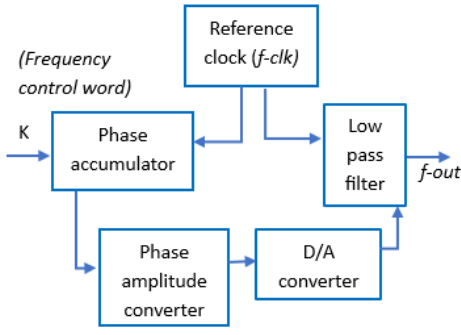


Fig. 1. Structure of direct digital synthesizer

frequency control word which is also known as frequency tuning word  $M$  controls the sampling of data at a given constant value that are given manually and hence the output frequency.

### B. Structure of DDS Signal Generator

The Structure of DDS Signal Generator includes a phase accumulator with a phase amplitude converter and a Digital or analog converter including a low-pass filter as illustrated in [Fig.1]. The phase accumulator is consisting of an adder and a register. The main function is to complete phase accumulation and waveform data output. The phase or amplitude converter is mainly to convert the output signal on the basis of the needed output form. The function of the Digital or Analog converter is mainly to convert the digital phase amplitude into analog quantity. The low pass filter that filters the signal to the needed form. It reduces the unwanted signal that obtained through the quantization. The signal is smoothened by the low pass filter by the filtering. The components of a Direct Digital Synthesizer (DDS) involve a phase generator also known as accumulator, phase to waveform convertor, low pass filter. To generate precise and adjust able output frequencies digital signal processing and analog components can be included.

## III. DDS WITH OPTIMIZATION TECHNIQUES

### A. Dither Generator

The Dither Generator Approach In another method to spread the spurs throughout the available bandwidth. The dither signal from the Dither Generator can add a dither signal to the Accumulator phase value. The model of DDS with Dither generated as illustrated in [Fig.2] The dither generator is mainly a pseudo-random noise sequence (generated, for example, with binary shift registers and exclusive-or gates, and having a repetition period much greater than the output signal period) whose word width is  $B$  bits providing noise values in the range of  $0$  and  $2B$ . it is mainly a sprinkles of noise particles or sequence which added to the signal to increase the accuracy with less spur. The Total Harmonic Distortion can be also reduced through it. The DDS with dither generator is modified using PN sequence.

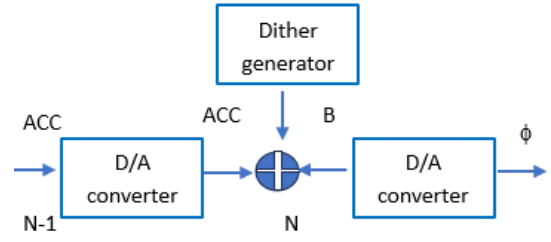


Fig. 2. Structure of DDS with Dither generator

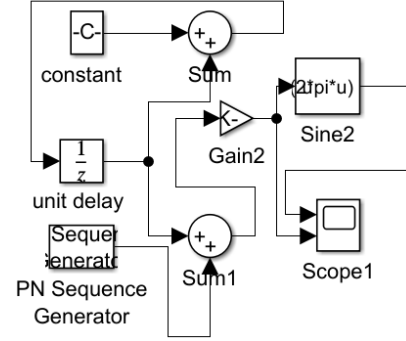


Fig. 3. Structure of DDS with Dither generator in MATLAB

### B. Odd Number Approach

The Odd Number Approach enhance the performance of DDS system and reduce the unwanted spur in the signal frequencies in the output waveform. In Direct Digital Synthesizer, a phase accumulator is typically used to produce the phase information of the output waveform. This phase information can be changed on the basis of the optimization technique. The information of the phase is then used to address a lookup table. The look up table contains the digital samples of the waveform. The output frequency of the DDS is identified by the value at which the phase accumulator is increased. Parameters such as the clock frequency and the number of bits in the phase accumulator. In that method the spurious frequencies produced by the DDS are odd multiples of the output frequency. It helps to reduce the spectral components in the output waveform. That are typically easier to filter the unwanted signal.

### C. Noise Shaping Approach

Noise shaping is also most significant technique used in direct digital synthesizer to enhance the signal-to-noise ratio (SNR) of a system. The effect of noise which can degrade the quality of the synthesized waveform. Quantization noise occurs mainly by the effect of limited precision of the digital samples. The digital samples are stored in the waveform lookup table and the finite resolution of the phase accumulator. That noise content leading to distortion and reduced signal stability. Noise shaping contains the use of digital filters to shape the spectral distribution of the quantization noise. It is pushed to frequencies where it is less perceptible or

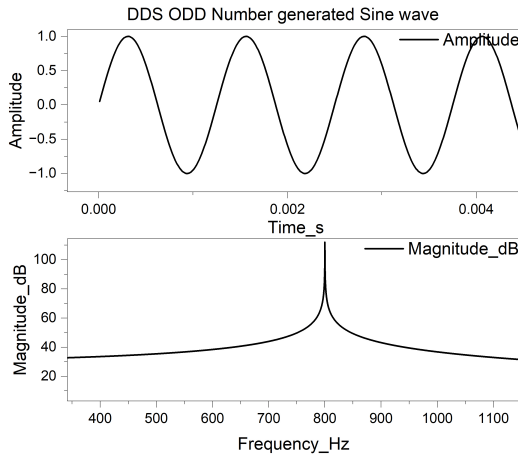


Fig. 4. FFT analysis of DDS with Odd Number Approach

easier to filter out. This is typically made by adding feedback of the quantization error into the DDS system, effectively shaping the noise spectrum. The DDS system generates a digital representation of the desired waveform by quantizing the output of the waveform lookup table. The quantized output is compared to the desired output, resulting in an error. The quantization error is processed by a digital filter, it is often a high-order filter. The filtered quantization error is fed back into the DDS system. By shaping the quantization noise spectrum to concentrate energy at higher frequencies or frequencies where it is less perceptible, noise shaping allows for a more efficient use of the available quantization levels, effectively increasing the SNR of the DDS system and improving the quality of the synthesized waveform.

#### IV. RESULT ANALYSIS

##### A. DDS with Odd Number Approach

The Odd Number Approach is one of the optimization techniques used in DDS to get more précised output signal. It helps to enhance the performance of DDS systems as illustrated in [Fig.3]. It is used mainly to reduce the unwanted spur in the signal frequencies in the output waveform. The output frequency of the DDS identified by the value at which the phase accumulator is increased. It helps to reduce the spectral components in the output waveform. It is mainly due to the odd multiples of the output frequency. That are typically easier to filter the unwanted signal. The sine wave of DDS with dither Odd number 1000 frequency generated and analysed. Total Harmonic Distortion (THD): 0.0023621.

##### B. DDS with Noise Shaping Approach

Noise shaping is applied by dithering and quantization such that the noise power. In the noise power is at a lower level in frequency bands. Noise is considered to be less desirable. By using noise shaping the quantization error can be effectively spread around so that more of it is focused on frequencies that can't be heard as well and less of it is focused on frequencies that can. In the result main quantization error can be reduced

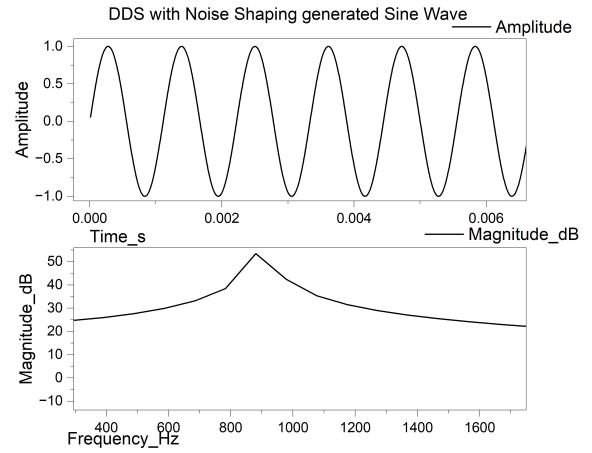


Fig. 5. FFT analysis of DDS with Noise Shaping Approach

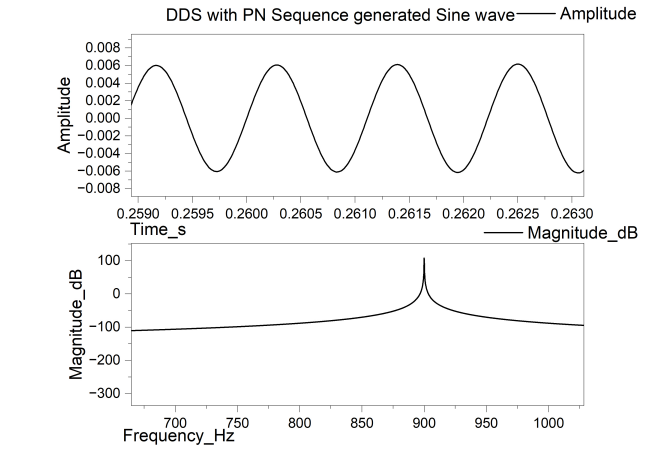


Fig. 6. FFT analysis of DDS with PN Sequence

greatly. It can be less sensitive the noise is much greater. as shown in [Fig.4]. the sine wave with 1000 frequency are obtained and fft analysed. Total Harmonic Distortion (THD): 0.0016899.

##### C. DDS with Dither Generator (PN Sequence)

Direct digital frequency synthesis technology which can convert a continuous digital signal into analog signals through a digital or analog converter.

The reference clock signal frequency is  $f_{clk}$ , the number of bits of the phase accumulator is  $N$ . The frequency control word also known as frequency tuning word. By changing the size of the frequency control word  $k$ , the output frequency can be changed. Total Harmonic Distortion (THD): 0.00048383. The DDS with Dither generated also known as PN Sequence output sine wave form of 1000 frequency are generated as shown in [Fig.5]. The obtained wave form are then compared with the other optimization techniques as shown in [Table.1].

The proposed DDS model incorporates various optimization techniques, including the Odd Number Approach, Noise Shaping Approach, and Dither Generator, which are thoroughly

TABLE I  
COMPARISON OF DDS WITH OPTIMIZATION TECHNIQUES

Optimization techniques	parameters	
	Target Frequency (Hz)	THD
PN Sequence Approach No of bits: - 1024 Sample Frequency=100000 Hz	1000	0.001972
	900	0.0010726
	800	0.0004838
	700	0.00040897
	600	0.0001283
Odd Number Approach Sample Frequency=100000 Hz	1000	0.0026202
	900	0.0022824
	800	0.0029022
	700	0.0005292
	600	0.0002924
Noise shaping approach copy No of bits: - 1024 Sample Frequency=100000 Hz	1000	0.080333
	900	0.080795
	800	0.080133
	700	0.078261
	600	0.080333

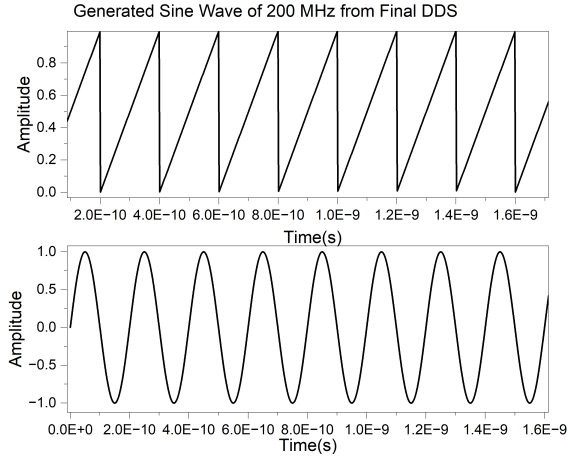


Fig. 7. Wave form of DDS with Dither generator (200 Mhz)

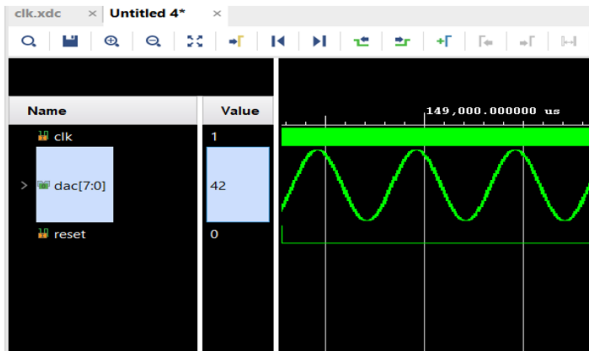


Fig. 8. Output sine wave of 200Mhz

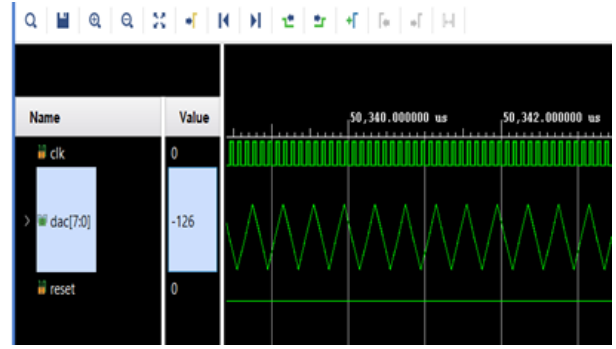


Fig. 9. Output sine wave of 200Mhz

analyzed. A constant value of 10,000 is maintained for the target frequency, with 1,024 samples used for analysis. After comparing the three techniques in MATLAB, the model demonstrates excellent high-frequency waveform generation up to 200 MHz as shown in [Fig.6]. The FFT and THD of the signals are evaluated, with the Dither Generator technique showing significantly lower THD than the other two, resulting in a more accurate output. A novel DDS design using a PN Sequence and configurations with or without the Dither Generator is developed. The output signals are compared, and a new DDS block design featuring the Dither Generator is created in Xilinx Vivado as shown in [Fig.7] and [Fig.8]. Simulation results obtained within Vivado show that this design can generate a sine wave by manually adjusting parameters for enhanced accuracy. Waveforms at different frequencies, including sine waves up to 200 MHz and triangular waves, are successfully generated. This enhanced model produces a more accurate sine wave with reduced THD, indicating improved signal quality.

## V. CONCLUSION

This paper presents a Direct Digital Synthesizer (DDS) incorporating various optimization techniques. Different parameters are analyzed to enhance signal accuracy and performance. The DDS model, designed with a PN sequence approach, achieves more accurate and precise signal generation. By adjusting the input parameters on the board, waveforms at different frequencies can be manually generated. This work addresses the limitations of DDS at frequencies around the 200 MHz range, implementing improvements that enhance signal quality and stability.

## REFERENCES

- [1] I. I. V. Strelnikov, I. V. Ryabov and E. S. Klyuzhev, "Direct Digital Synthesizer of Phase-Manipulated Signals, Based on the Direct Digital Synthesis Method," 2020 Systems of Signal Synchronization, Generating and Processing in Telecommunications (SYNCHROINFO), Svetlogorsk, Russia, 2020, pp. 1-3, doi: 10.1109/SYNCHROINFO49631.2020.9166040.
- [2] I. I. V. Ryabov, I. V. Strelnikov, S. V. Tolmachev and E. S. Klyuzhev, "Direct Digital Synthesizers of Complex Broadband Signals," 2019 Systems of Signals Generating and Processing in the Field of on Board Communications, Moscow, Russia, 2019, pp. 1-4, doi: 10.1109/SOSG.2019.8706776.

- [3] 4. D. N. Bochkarev, I. V. Ryabov, I. V. Strelnikov and N. V. Degtyarev, "Direct Digital Synthesizers of Frequency and Phase-Modulated Signals," 2019 Systems of Signal Synchronization, Generating and Processing in Telecommunications (SYNCHROINFO), Russia, 2019, pp. 1-4, doi: 10.1109/SYNCHROINFO.2019.8814244.
- [4] I. V. Ryabov, S. V. Tolmachev and P. M. Yuriev, "DIRECT DIGITAL SYNTHESIZER WITH FAST FREQUENCY TUNING," 2018 Systems of Signal Synchronization, Generating and Processing in Telecommunications (SYNCHROINFO), Minsk, Belarus, 2018, pp. 1-3, doi: 10.1109/SYNCHROINFO.2018.8456988.
- [5] S. Saad, M. Mhiri, A. B. Hammadi and K. Besbes, "An Enhanced Variable Phase Accumulator with Minimal Hardware Complexity Dedicated to ADPLL Applications," 2018 15th International Multi-Conference on Systems, Signals and Devices (SSD), Yasmine Hammamet, Tunisia, 2018, pp. 1447-1452, doi: 10.1109/SSD.2018.8570405.
- [6] S. Narayan Sinha, S. Chatterjee and R. K. Palani, "A 2-GHz Two-Tone Direct Digital Frequency Synthesizer," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 12, pp. 5109-5113, Dec. 2022, doi: 10.1109/TCSII.2022.3202903.
- [7] Bochcarev, "Formation of Frequency-Modulated Signals Using the Direct Digital Synthesis Method," 2021 Wave Electronics and its Application in Information and Telecommunication Systems (WECONF), St. Petersburg, Russia, 2021, pp. 1-4, doi: 10.1109/WECONF51603.2021.9470536.
- [8] 9. Yan, J. Sun and W. Liu, "An Efficient High SFDR PDDS Using High-Pass-Shaped Phase Dithering," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 29, no. 11, pp. 2003-2007, Nov. 2021, doi: 10.1109/TVLSI.2021.3114680.
- [9] 10. V. Strelnikov, I. V. Ryabov and E. S. Klyuzhev, "Direct Digital Synthesizer of Phase-Manipulated Signals, Based on the Direct Digital Synthesis Method," 2020 Systems of Signal Synchronization, Generating and Processing in Telecommunications (SYNCHROINFO), Svetlogorsk, Russia, 2020, pp. 1-3, doi: 10.1109/SYNCHROINFO49631.2020.9166040.
- [10] 11. I. V. Ryabov, N. V. Degtyarev and D. N. Bochcarev, "Formation of Frequency-Modulated Signals Using the Direct Digital Synthesis Method," 2021 Wave Electronics and its Application in Information and Telecommunication Systems (WECONF), St. Petersburg, Russia, 2021, pp. 1-4, doi: 10.1109/WECONF51603.2021.9470536.
- [11] 12. Yan, J. Sun and W. Liu, "An Efficient High SFDR PDDS Using High-Pass-Shaped Phase Dithering," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 29, no. 11, pp. 2003-2007, Nov. 2021, doi: 10.1109/TVLSI.2021.3114680.
- [12] K. Galanopoulos and P. P. Sotiriadis, "Modulation techniques for all-digital transmitters based on Pulse Direct Digital synthesizers," 2012 IEEE International Frequency Control Symposium Proceedings, Baltimore, MD, USA, 2012, pp. 1-4, doi: 10.1109/FCS.2012.6243662.
- [13] 14. J. -M. Choi et al., "Design and Analysis of Low Power and High SFDR Direct Digital Frequency Synthesizer," in IEEE Access, vol. 8, pp. 67581-67590, 2020, doi: 10.1109/ACCESS.2020.2986016.
- [14] 15. H. Liu, Z. Fu, S. Qi, D. Kong and H. Wang, "A Waveform Distortion Correction Method Based on Jitter Injection and FIR Digital Filter Using Farrow Structure," 2023 IEEE AUTOTESTCON, National Harbor, MD, USA, 2023, pp. 1-8, doi: 10.1109/AUTOTESTCON47464.2023.10296391.
- [15] 16. J. Muñoz, J. Arbustini, E. Elzenheimer, M. Höft and A. Bahr, "Digital Approaches on Frequency Tuning for Magnetoelectric Sensors," 2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Glasgow, United Kingdom, 2022, pp. 1-4, doi: 10.1109/ICECS202256217.2022.9970919.
- [16] 17. G. D'Amato, G. Avitabile, G. Coviello and C. Talarico, "DDS-PLL Phase Shifter Architectures for Phased Arrays: Theory and Techniques," in IEEE Access, vol. 7, pp. 19461-19470, 2019, doi: 10.1109/ACCESS.2019.2895388.
- [17] 18. C. Yan, J. Sun and W. Liu, "An Efficient High SFDR PDDS Using High-Pass-Shaped Phase Dithering," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 29, no. 11, pp. 2003-2007, Nov. 2021, doi: 10.1109/TVLSI.2021.3114680.
- [18] J. -M. Choi et al., "Design and Analysis of Low Power and High SFDR Direct Digital Frequency Synthesizer," in IEEE Access, vol. 8, pp. 67581-67590, 2020, doi: 10.1109/ACCESS.2020.2986016.
- [19] T. Guo, K. Tang and Y. Zheng, "A 1GHz Configurable Chirp Modulation Direct Digital Frequency Synthesizer in 65nm CMOS," 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea, 2021, pp. 1-4, doi: 10.1109/ISCAS51556.2021.9401736.
- [20] K. Yousef, "A low phase noise, high figure of merit, 3.1 GHz-3.5 GHz ring oscillator using edge injection technique," 2017 Japan-Africa Conference on Electronics, Communications and Computers (JAC-ECC), Alexandria, Egypt, 2017, pp. 37-40, doi: 10.1109/JEC-ECC.2017.8305773.
- [21] S. M. Schober and J. Choma, "A capacitively phase-coupled low noise, low power 0.8-to-28.2GHz quadrature ring VCO in 40nm CMOS," 2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS), Grenoble, France, 2015, pp. 1-4, doi: 10.1109/NEWCAS.2015.7181985.
- [22] A. Homayoun and B. Razavi, "Relation Between Delay Line Phase Noise and Ring Oscillator Phase Noise," in IEEE Journal of Solid-State Circuits, vol. 49, no. 2, pp. 384-391, Feb. 2014, doi: 10.1109/JSSC.2013.2289893.
- [23] W. Bae, H. Ju, K. Park, S. -Y. Cho and D. -K. Jeong, "A 7.6 mW, 214-fs RMS jitter 10-GHz phase-locked loop for 40-Gb/s serial link transmitter based on two-stage ring oscillator in 65-nm CMOS," 2015 IEEE Asian Solid-State Circuits Conference (A-SSCC), Xiamen, China, 2015, pp. 1-4, doi: 10.1109/ASSCC.2015.7387448.
- [24] P. Mostafa, S. Karmakar and S. Chatterjee, "A Multiphase Low Phase-Noise DCO based on Self-Timed Ring Oscillator," 2023 International Symposium on Devices, Circuits and Systems (IS-DCS), Higashihiroshima, Japan, 2023, pp. 1-4, doi: 10.1109/IS-DCS58735.2023.10153557.
- [25] S. Robson, B. Leung and G. Gong, "Truly Random Number Generator Based on a Ring Oscillator Utilizing Last Passage Time," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 61, no. 12, pp. 937-941, Dec. 2014, doi: 10.1109/TCSII.2014.2362715.
- [26] G. von Bueren, D. Barras, H. Jaeckel, A. Huber, C. Kromer and M. Kossel, "Design and phase noise analysis of a multiphase 6 to 11 GHz PLL," 2009 Proceedings of ESSCIRC, Athens, Greece, 2009, pp. 384-387, doi: 10.1109/ESSCIRC.2009.5326023.
- [27] S. -N. Hsieh and T. -H. Chu, "A linear retro- and reflecto-nulling antenna array with an odd element number," 2009 Asia Pacific Microwave Conference, Singapore, 2009, pp. 2664-2667, doi: 10.1109/APMC.2009.5385354.
- [28] H. Xingui, "Harmonic analysis of three-phase fractional-slot concentrated windings based on number theory," 2019 22nd International Conference on Electrical Machines and Systems (ICEMS), Harbin, China, 2019, pp. 1-6, doi: 10.1109/ICEMS.2019.8921525.
- [29] G. D'Amato, G. Avitabile, G. Coviello and C. Talarico, "DDS-PLL Phase Shifter Architectures for Phased Arrays: Theory and Techniques," in IEEE Access, vol. 7, pp. 19461-19470, 2019, doi: 10.1109/ACCESS.2019.2895388.
- [30] D. Panda and V. Ramanarayanan, "Mutual Coupling and Its Effect on Steady-State Performance and Position Estimation of Even and Odd Number Phase Switched Reluctance Motor Drive," in IEEE Transactions on Magnetics, vol. 43, no. 8, pp. 3445-3456, Aug. 2007, doi: 10.1109/TMAG.2007.898101.