IOSR Journal of Engineering
May. 2012, Vol. 2(5) pp: 1000-1006

Power Factor Improvement With High Efficiency Converters

P. YOHAN BABU, P.SURENDRA BABU, K. Ravi Chandrudu, G.V.P. Anjaneyulu

***Abstract*—**New recommendations and future standards have increased the interest in power factor improvement circuits. There are multiple solutions in which line current is sinusoidal. In addition, in the recent years, a great number of circuits have been proposed with non sinusoidal line current. In the proposed circuit, the power factor is improved by using an auxiliary winding coupled to the transformer of a cascade DC/DC fly back converter. The auxiliary winding is placed between the input rectifier and the low-frequency filter capacitor to serve as a magnetic switch to drive an input inductor. The proposed approach is primarily based on the concept of inductive effect, from which PFC cells composed of energy buffers and high-frequency signals are introduced. Since the DC/DC fly back converter is operated at high-switching frequency, the auxiliary windings produce a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced. Properly selecting an eligible PFC cell and inserting it in between input rectifier and dc-link capacitor can yield an SSC which can improve the input power factor significantly.

Key Words—PFC, DC/DC converter, SSC, THD

I. INTRODUCTION

In modern electronic products, including personal computers, computer peripherals, and test instruments, AC/DC Converters have become the primary power supplies. The AC/DC converters use switching circuits to achieve high-power transfer efficiency and ac/dc converter controllers can be designed flexibly. Improving power quality considerations requires two things: achieving high power factor and low high-frequency harmonics. Many studies have examined the relevant issues and numerous topologies have been proposed. The proposed solutions of these studies can be classified into two groups: those designed such that the input line current is sinusoidal and those designed such that it is non sinusoidal [23], [24]. The group of topologies with the sinusoidal line current almost achieves the requirement of unity power factor but requires a complex topology or control circuit [25], [26]. Thus, the sinusoidal line current topologies are more costly to implement. Fig. 1 shows the block diagram of the ac/dc converter with sinusoidal input line current. The AC/DC converter with non sinusoidal line current employs a simple topology, such as single-stage–single-switch, and costs less in practical applications [28]–[31]. Although the circuits [29]–[31] lack a unity power factor, they comply with IEC 61000-3-2 [26]. A family of such circuits was described in [23] and [24]. In this family a boost circuit accompanied by a DC/DC converter was introduced to form the so-called single-stage single-switch AC/DC converters. The family circuits have PFC function, as illustrated in Fig. 2. This concept successfully simplifies a conventional power-factor corrector by changing it from two stages to one stage. However, this concept employs a bulk inductor in the boost section, which occupies significant volume and weight. The new converter satisfies the input harmonic current limits required by IEC 61000-3-2 and also has fast output response. A multi winding transformer is employed in the proposed converter. The additional winding in the primary side is known as a reset winding in the forward-type converter. The reset winding of the transformer replaces the boost inductor presented in [28]–[31]. Moreover, the proposed converter design reduces the volume and weight of the magnetic material by almost half compared to existing boost-based single-stage PFC converters. Furthermore, the voltage across the bulk capacitor can be reduced to a reasonable value by adjusting the turn's ratio of the windings and, therefore, this design can adapt to significant line voltage variation. Generally, single-stage PFC converters meet the regulatory requirements regarding the input current harmonics, but they do not improve the power factor and reduce the THD as much as their conventional two-stage counterpart. The power factor could be as low as 0.8, however, they still meet the regulation. In addition, although the single-stage scheme is especially attractive in low cost and low power applications due to its simplified power stage and control circuit, major issues still exist, such as low efficiency and high as well as wide-range intermediate DC bus voltage stress [2], [3]. Another technique based on parallel connection of this dither signal is presented in [8]; however, the harmonic content can meet the regulatory standard by a small margin. In [14], a new concept of PFC is proposed to improve the efficiency of a single-stage converter by preventing the input current or voltage stress due the PFC cell from being added to the active switch. In this circuit, the dc/dc cell operates in DCM so that a series of discontinuous pulses is used to shape the input inductor current and the PFC is achieved. As the circuit uses resonance of circuit parameters to achieve PFC, the control of the power factor will be very sensitive to the variation of components values. In this letter, a new technique of PFC is proposed. The PFC cell is formed by connecting the energy buffer (*LB*) and an auxiliary winding (*L*3) coupled to the transformer of the dc/dc cell, between the input rectifier and the low-frequency filter capacitor used in conventional power converter. Since the dc/dc cell is operated at high frequency, the auxiliary winding produces a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input

current harmonics is reduced. The input inductor *LB* operates in DCM such that a lower THD of the input current can be achieved.

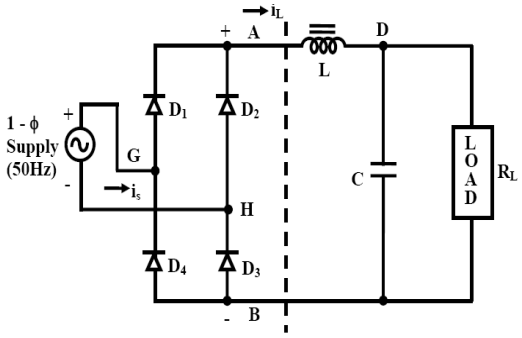

Fig 1: Full bridge diode rectifier

II. REVIEW OF SINGLE STAGE PFC TOPOLOGIES

Concept for single-state PFC can be traced back to some early work presented in [1], [2]. In article [1], a single power stage with dual outputs produces both the desired DC output and a boosting supply in series with the input. Without active control of the boost supply, a reasonably good input current shape results due to the natural gain characteristics of the boost resonant circuit. This circuit is original but the component count is high. Another way to realize single stage PFC is by cascading a boost ICS with a dc–dc converter using one switch as shown in [2]. Both pulse width modulation (PWM) and frequency modulation (FM) were applied in the control circuitry. The rectifier has very high power factor. However, the circuit suffers wide frequency variation and high voltage stress. Nevertheless, this circuit presents an early form of the single stage PFC method that integrates a boost ICS with a dc–dc converter in a cascade fashion. A very systematic synthesis of single stage PFC using cascade method was initiated in article [3] in 1992, in which some new PFC rectifiers, BIFRED and BIBRED, were resulted from integrating a boost input current shaper with a converter as shown in Fig. 1. The characteristic marker of these rectifiers is that the energy storage capacitor is in the series path of the energy flow. Synthesis of single stage PFC by inserting a diode in front of the Cuk and Sepic converters have resulted in the same topologies [4], [5]. The dc-bus capacitor voltage has a strong dependency on the output load. For universal input applications, it will suffer high voltage stress at light load. Articles [4], [6] use frequency modulation method to keep the dc-bus voltage under control during light load. Article [5] shows a new operation mode for the Sepic converter that operates both the boost like ICS and the DC/DC converter in DCM, which has effectively reduced the DC-bus voltage and significantly improved the input current waveform.

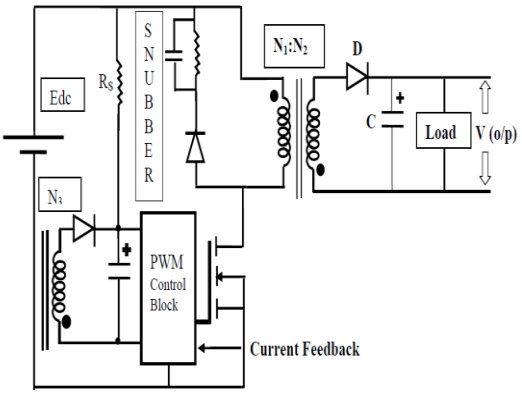

Fig 2: General circuit diagram of rectifier with PFC cells

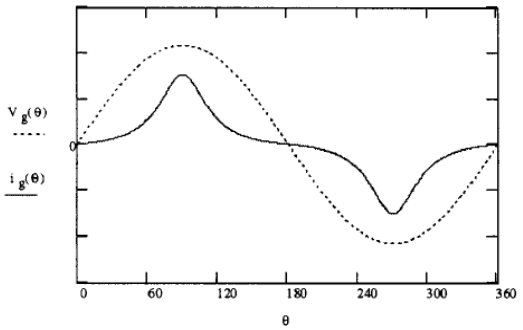

Fig.3. Typical input voltage waveforms for single-stage PFC.

Topological variations are also found in many other forms. A parallel PFC concept was reported in [9], while three switch-states were used to provide two-dimensional (2-D) control for the PFC function and fast output regulation. The performance is commendable but the implementation is very complicated. In article [10], [11], a converter is used as ICS, which results in better input current waveform but higher current stress. An interesting method of combining a boost ICS with a forward converter with two energy storage capacitors was shown in [12]. With two capacitors, the spike due to the leakage inductance during switch turn off is subdued. Very good performance was demonstrated. Article [13] shows a new single stage PFC rectifier that uses an ac side inductor and additional two diodes to directly connect the ac voltage to the switch. This circuit has similar operational principle as the one proposed in [7], but with less conduction loss. The rectifier proposed in [8] uses a boost bridge rectifier that shares its switches with the following dc–dc converter with the intention to increase the power level. Since both the boost bridge rectifier and the converter operate in DCM, the conduction loss is high. In addition, this circuit may suffer high common mode noise. Article [14] presented a rectifier that integrates a boost ICS and a half bridge dc–dc converter. Synchronized rectifiers are used to achieve high efficiency for low voltage applications. Article [15] proposed a regenerative clamping circuit for single-stage PFC to reduce the turn-off losses and stress of the switch. In addition, the power factor is also improved. Article [16] reported a single stage high power

factor converter using the Sheppard–Taylor topology. Two possible operation regimes are described. Compared to the usual boost-buck cascade operating in the first regime, the proposed converter has a wider operating range. When operating in the second regime, the modified boost stage has the ability of producing a harmonic free input current, unlike the standard boost PFC whose current always suffers a cusp distortion. A new parallel approach for single stage PFC was reported in [17]–[20] that employ an auxiliary dc/dc converter to supplement energy to the load when the direct power from the line is low. This method improves overall efficiency because only partial energy is processed twice. An additional switch is required. Extensive syntheses were performed in [21], [22] that yielded many families of single stage PFC rectifiers based on dither effect [21] and partial energy processing [22]. These two papers present interesting teaching from the principle of synthesis as well as analysis to the implementation of the new circuits, thus are valuable to researchers in the power factor correction area.

A. Steady-State Analysis

The voltage conversion ratio of the proposed converter can be estimated from the volt-second balance on the inductors and the input–output power balance as explained in the following. From the volt-second balance on *LB*

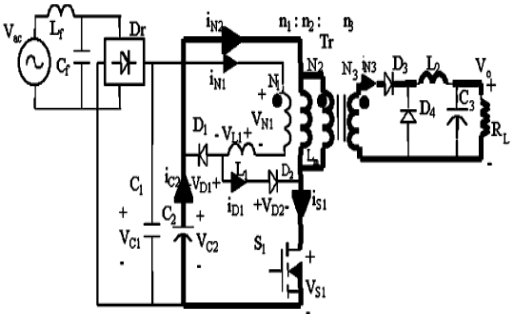

Fig:4 Family circuits have PFC function

$$\left(V_{in}+\frac{N_3}{N_1}V_{CB}-V_{Ca}\right)dT_s=(V_{CB}-V_{in})d_1T_s \qquad (1)$$

Where d_1 is the OFF-time of the switch (SW).

Therefore, $d_1$could be given by

$$d_1=\frac{V_{in}+(N_3/N_1)V_{CB}-V_{Ca}}{V_{CB}-V_{in}}d \qquad (2)$$

From Fig. 2, the average current of the boost inductor in a switching cycle is given by

$$I_{in}=I_{LB,av}=\frac{i_{LB,peak}}{2}(d+d_1)T_s \qquad (3)$$

Substituting for $i_{LB,peak}$ given in (2) and using (2), the average input current is given by

$$I_{in}=\frac{V_{in}+(N_3/N_1)V_{CB}-V_{Ca}}{2L_B}d^2T_s \times\left(\frac{(1+N_3/N_1)V_{CB}-V_{Ca}}{V_{CB}-V_{in}}\right) \qquad (4)$$

Based on (4) for a given input voltage, the normalized input current waveform in a half cycle for a change in the turns ratio *N3*/*N*1. It can be seen that to reduce the dead time and improve the power factor of the input current the turn's ratio must be ≥0.5. The normalized input current waveform for a change in dc bus capacitor voltage is *VCB*. As it can be seen that the higher the *VCB* the better quality of the input current waveform (lower THD). However, higher *VCB* means higher voltage stress on the power switch (SW), which can reduce the efficiency of the converter. Therefore, a tradeoff between THD and efficiency must be made. The energy absorbed by the circuit from the source during a half switching cycle is given by

$$P_{in}=\frac{1}{\pi}\int_0^{\pi}V_m\sin(t)I_{in}dt \qquad (5)$$

Substitution for I_{in} in given (4) yields

(6)

Where

$$P_{in}=\frac{1}{\pi}\frac{V_m}{2L_B}d^2T_s(A)\int_0^{\pi}\sin(t)Bdt$$

$$A=\left[\left(1+\frac{N_3}{N_1}\right)V_{CB}-V_{Ca}\right],$$

$$B=\frac{V_m\sin(t)+(N_3/N_1)V_{CB}-V_{Ca}}{V_{CB}-V_m\sin(t)} \qquad (7)$$

The average output power for a DCM converter is given by

$$P_o=\frac{V_{CB}^2}{2L_m}d^2T_s \qquad (8)$$

Assume 100% efficiency, $P_{in}=P_0$, yields

$$V_{CB}^2=\frac{V_m}{\pi}\frac{L_m}{L_B}(A)\int_0^{\pi}\sin(t)Bdt \qquad (9)$$

Equation (8) shows that the dc bus capacitor is independent of load variation; *VCB* is determined by the input voltage and circuit parameters L_m/L_B, N_3/N_1 Note that, (8) is transcendental and can only be solved by numerical method using specific circuit parameters.

III. HARMONICS IN POWER SYSTEM

One of the biggest problems in power quality aspects is the harmonic content in the electrical system. Generally, harmonics may be divided into two types: 1) voltage harmonics 2) current harmonics. Current harmonics is usually generated by harmonics contained in voltage supply and depends on the type of load such as resistive load, capacitive load and inductive load. Both harmonics can be generated by either the source or the load side. Harmonics generated by load are caused by nonlinear operation of devices, including power converters, arc-furnaces, gas

discharge lighting devices, etc. Load harmonics can cause the overheating of the magnetic cores of transformer and motors. On the other hand, source harmonics are mainly generated by power supply with non-sinusoidal voltage waveform. Voltage and current source harmonics imply power losses, Electromagnetic Interference (EMI) and pulsating torque in AC motor drives. Any periodic waveform can be shown to be the superposition of a fundamental and a set of harmonic components. By applying Fourier transformation, these components can be extracted. The frequency of each harmonic component is an integral multiple of its fundamental. There are several methods to indicate of the quantity of harmonics contents. The most widely used measure in North America is the total harmonics distortion (THD), which is defined in terms of the amplitudes of the harmonics, Hn, at frequency nw_0, where w_0 is frequency of the fundamental component whose amplitude of *H1* and *n* is integer. The THD is mathematically given by

$$THD = \frac{\sqrt{\sum_{n=2}^{m} H(n)^2}}{H1} \qquad (10)$$

IV. LINEAR AND NON-LINEAR LOADS

A linear element in a power system is a component in which the current is proportional to the voltage. In general, this means that the current wave shape will be the same as the voltage (See Figure 5, 6, 7). Typical examples of linear loads include motors, heaters and incandescent lamps

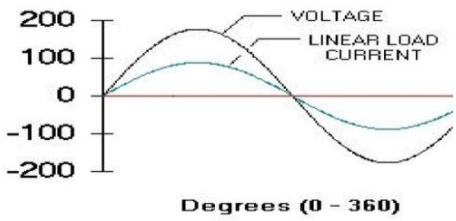

Fig 5: Voltage and current waveforms for linear loads

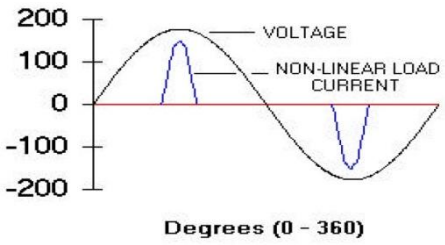

Fig 6: – Voltage and current waveforms for non-linear loads

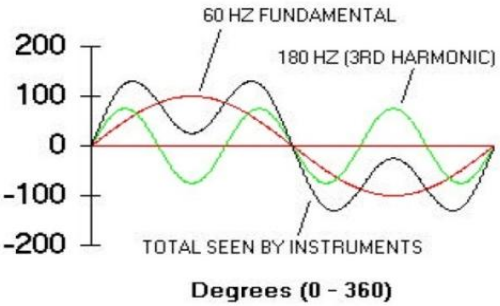

Fig 7: Waveform with symmetrical harmonic component

V. CIRCUIT EQUATIONS UNDER CONTINUOUS-FLUX OPERATION

The waveforms in correspond to steady state operation under continuous magnetic flux. 't_{ON}' denotes the time for which the fly-back switch is ON during each switching cycle. 'T' stands for the time period of the switching cycle. The ratio (t_{ON} /T) is known as the duty cycle (δ) of the switch. As can be seen from the primary winding current rises from I_0 to $I_p$in 'δT' time. In terms of input supply voltage (E_{dc}) and the primary winding inductance
The following relation holds:

$$Pri L\ (I_P - I_0) = (E_{dc}/)\ \delta T$$

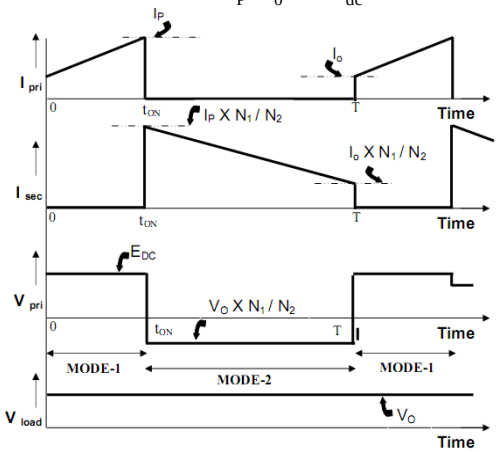

Fig 8: Wave forms for Fly-back circuit waveforms under continuous magnetic flux

Under steady state the energy input to primary winding during each ON duration equals: $0.5E_{dc}$ (I_P +I_0) δT and similarly the output energy in each cycle equalsV_0I_{Load} T, where V_0 is the output voltage magnitude and I_{Load} denotes the load current. Equating energy input and energy output of the converter (the converter was assumed loss-less) in each supply cycle, one gets

$$0.5E_{dc}\ (I_p + I_0)\ \delta = V_0I_{Load} \qquad (11)$$

The mean (dc) voltage across both primary and secondary windings must be zero under every steady state. When the switch is ON, the primary winding voltage equals input supply voltage and when the switch is OFF the

reflected secondary voltage appears across the primary winding. Under the assumption of ideal switch and diode.

$$E_{dc}\delta = (N_1 / N_2)\, V_1\, (1-\delta) \qquad (12)$$

Where N_1 and N_2 are the number of turns in primary and secondary windings and $(N_1 / N_2)\, V_0$ is the reflected secondary voltage across the primary winding (dotted end of the windings at lower potential) during mode-2 of circuit operation. One needs to know the required ratings for the switch and the diode used in the converter. When the switch is OFF, it has to block a voltage (V_{SWITCH}) that equals to the sum of input voltage and the reflected secondary voltage during mode-2. Thus,

$$V_{Switch} = E_{dc} + (N_1 / N_2)\, V_0 \qquad (13)$$

When the switch in ON, the diode has to block a voltage (**V_{diode}**) that equals to the sum of output voltage and reflected primary voltage during mode-1, i.e.,

$$V_{diode} = V_0 + E_{dc}\,(N_2 / N_1) \qquad (14)$$

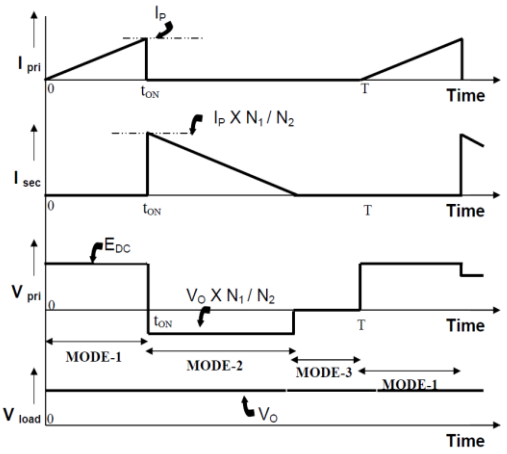

Fig 9: Fly-back circuit waveforms under discontinuous magnetic flux

With the turning ON of the switch, the primary winding current starts building up linearly from zero and at the end of mode-1 the magnetic field energy due to primary winding current rises to 212*priPLI*. This entire energy is transferred to the output at the end of mode-2 of circuit operation. Under the assumption of loss-less operation the output power (P_o) can be expressed as

$$P_0 = 21/2 priPLI_{switch} \qquad (15)$$

Where F_{switch}=1/T is the switching frequency of the converter. It may be noted that output power $\mathbf{P_0}$ is same as $V_0 I_{Load}$ used in Equation (11). The volt-time area equation as given in Eqn.(12) gets modified under discontinuous flux mode of operation as follows

$$E_{dc}\,\delta \leq (N_1 / N_2)\, V_0\, (1-\delta) \qquad (16)$$

Average voltage across windings over a switching cycle is still zero. The inequality sign of Eqn.16 is due to the fact that during part of the OFF period of the switch [= (1-δ)T], the winding voltages are zero. This zero voltage duration had been identified earlier as mode-3 of the circuit operation.

VI. RESULT ANALYSIS

In order to verify the proposed concept, a prototype of the converter shown in Fig. 2 was constructed and experimentally tested. To ensure proper operation of the converter, the dc bus voltage (*VCB*) must be higher than the input voltage, such that the diode *D*1 is OFF and the inductor *LB* stores energy when the switch (SW) is ON. Therefore, from (15) the inductor *Lm* must be higher than the input inductor *LB*. The DCM converter was designed and implemented for 50 V/80 W output, *V*in,rms (100–240 V) universal line voltage, and overall efficiency of 86% is assumed. The switching frequency is selected to be 100 kHz and the maximum duty cycle of is 0.45.

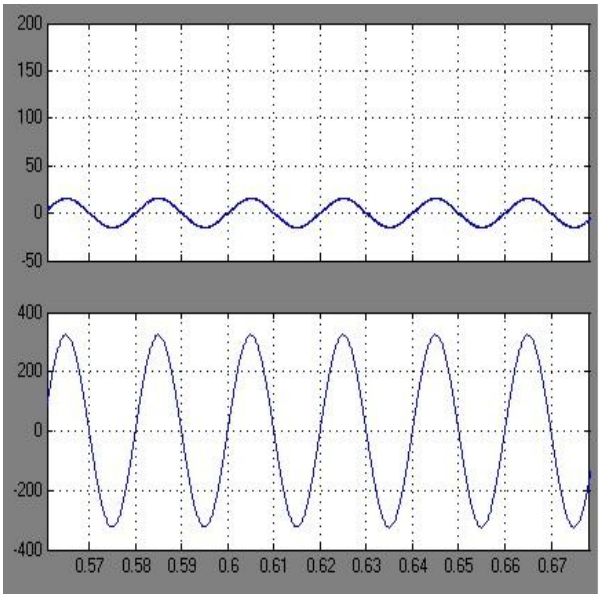

Fig 10: input current& input voltage measurement at diode rectifier

Fig.10 shows the measured input voltage and filtered input current waveforms for a 100 V_{ac} input voltage at full load.

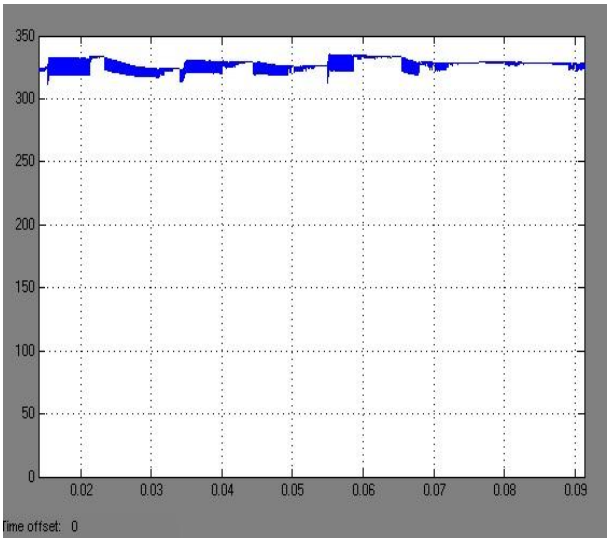

Fig 11: DC Capacitor voltage

As it may be seen from Figs. 4, 5 and 6, that selecting the turn's ratio *N*3/*N*1 and the dc bus voltage V_{CB} can be optimized in order to reduce the dead time and improve the quality of the input current. The measured harmonic content of the input current compared to the Classes A and D regulation standards. Note that, in order to improve the visibility of the higher order harmonics, class A limits are scaled down by a factor of 5 (class A limits/5). The measured THD = 7% and the power factor is 0.997. Obviously, the input current is much closer to the sinusoidal waveform and it meets the regulation standards. Fig. 11 & 12 shows the transient response of the converter for a step change of load between 50% and 100%. It may be seen that a fast dynamic response has been obtained. Fig. 13 shows the input current of inductor- transformer and Fig 14 shows the measured dc bus voltage *VCB* and efficiency of the converter for range of load and input voltage variation. It may be seen that the capacitor voltage can be maintained below 450 V by properly designing the turn's ratio *N*3/*N*1 and the inductors ratio *Lm/LB*. Furthermore, the proposed converter can maintains 90% efficiency or above at high load.

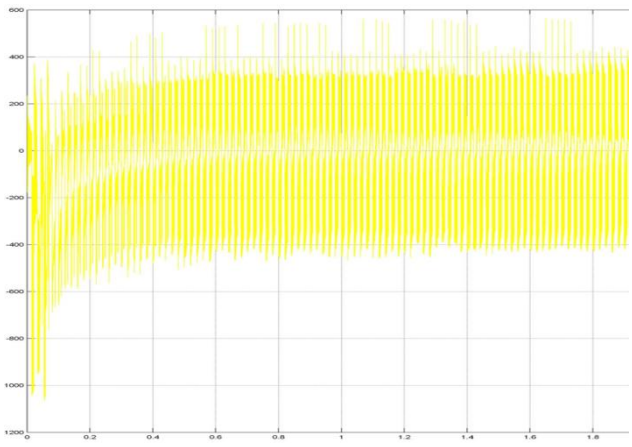

Fig12. Response between 50% and 100% of load.

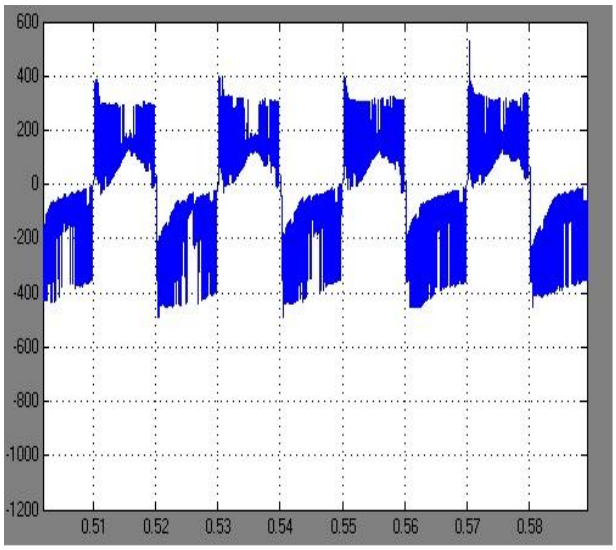

Fig 13: input current of inductor-transformer

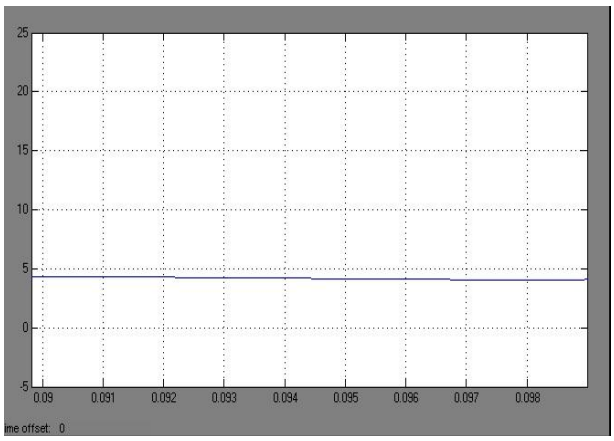

Fig 14: response of dc voltage

VII. CONCLUSION & FUTURE SCOPE

In this paper, a new AC/DC converter based on a PFC scheme has been presented. The proposed method produces a current with low harmonic content to meet the standard specifications as well as high efficiency. This circuit is based on adding an auxiliary winding to the transformer of a DC/DC DCM fly back converter. The input inductor can operates in DCM to achieve lower THD and high power factor. By properly designing the converter components, a tradeoff between efficiency and harmonic content can be established to obtain compliance with the regulation and efficiency as high as possible. Operating principles, analysis, and experimental results of the proposed method are presented.

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