

Design of a Variable Structure Controller for Power Quality Enhancement of a Micro Grid Inverter

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Abstract: The paper develops a Variable Structure Controller (VSC) to reduce the total harmonic distortion of the output voltage of the micro grid inverter fed from a solar source. It involves the use of a Single Ended Primary Inductor Converter (SEPIC) structure to form the basic inverter module and ensure that the control mechanism regulates the output voltage across a range of operating loads. The theory of VSC arbitrates to imbibe a structural modification to the inverter in an effort to resurrect the trajectory along the load line and accomplish a compliance of delivery of power to the load. The philosophy orients to arrive at a reference for generating the Pulse Width Modulation (PWM) pulses for the switches in order that it serves to increase the fundamental component and lower the higher frequency components of the output voltage. The MATLAB based simulation results improved the ability of the controller to reject servo and regulatory disturbances and offer a better performance over that of the benchmark PI controller. The results obtained from a prototype validate the simulated response and espouse a new dimension to the use of such inverters in the field of renewable energy.

Keywords: Micro grid, SEPIC, VSC, THD

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I. INTRODUCTION

A power converter forms an essential component in the use of a renewable resource with a view to augment the imbalance between generation and demand besides engaging the emergence of the green energy. Among the three types that include the central, string and the micro inverters [1], the micro inverters find a wide scope for its use from the solar panels. The inverters generally occupy a significant space in industrial, commercial and air craft power supplies.

The PV inverters constitute to be a part of the power conversion system that convert the power available from the PV panels to an ac, that can either be fed to the grid or operate in a standalone manner. The size of the passive components decreases when the switching frequency of the inverter increases together with the decrease in the weight and size of the inverter [2-4].

However the switching losses increase due to the increase in switching frequency and in turn affect the efficiency of the converter. The switch mode dc-to-ac inverters using the dc-to-dc converter topology inherit a number of advantages over the traditional bridge type inverter where in the output voltage of the inverter can easily be stabilized [5-7].

A dc-dc boost converter has been designed to operate in the continuous conduction mode using PWM technique. The simulation results have been presented to show that the sliding mode control scheme provides good voltage regulation and suitable when changes in the line voltage and converter parameters [8].

A converter-per-module approach has been suggested to reap the advantages including individual module maximum power point tracking, which offers a greater flexibility in module layout, replacement and insensitivity to shading. The simple non-isolated per-module dc-dc converter has been series connected to create a high voltage string connected to a simplified dc-ac inverter. The buck converter has been projected as the most efficient topology using investigative exercises [9].

A novel single-phase flyback inverter for photovoltaic applications has been proposed to achieve low-frequency ripple current reduction on the dc bus bar and to deliver sinusoidal current into the ac grid. The

topology has been derived from a SEPIC and two-switch flyback inverter to obtain soft switching operation for the active switches and operates based on capacitive idling techniques. The peak-current mode control method has been employed in the control schemes to ensure pure sinusoidal current with unity power factor on the ac grid and laboratory experimental results using a 500 W prototype included to verify the effectiveness of the inverter [10].

Two three-phase buck-boost current source inverters (CSIs) have been designed for use in general energy conversion applications where the input source voltage varies widely. The inverters have been developed by first identifying characteristic modular features of a traditional CSI before integrating with a buck-boost converter and a SEPIC to develop a two extended single-stage dc-ac inverters with bidirectional power conversion ability. The resulting digitally controlled inverters have been tested in simulation using PSIM with Matlab/Simulink coupler and experimentally using two laboratory prototypes for demonstrating their smooth steady-state and transient operations [11].

A z- source has been employed with an LC impedance network between the main inverter bridge and the power source. The unique feature of the Zero Switching Inverter (ZSI) has been shown to allow it to operate either in the buck and boost mode with a wide range of obtainable output voltages from a given input voltage. A novel topology called switched boost inverter (SBI) which exhibits similar advantages of ZSI with lower number of passive components and more active components compared to ZSI has been brought out. The steady state and small signal analysis of SBI along with its PWM control strategies have been discussed to present a comparative study of SBI and ZSI with the same input and output parameters [12].

A transformerless grid-connected SEPIC converter has been proposed for photovoltaic generation system. The salient features of the converter has been that the two inductors in the topology can be used to store energy and the electromagnetic field allowed to produce an non-inverted continuous output voltage. It has been shown to operate at high switching frequency with any type of load [13].

The performance of a photovoltaic array fed three phase induction motor through a voltage source inverter (VSI) has been evaluated using MATLAB based simulation. The experimental work has been carried out with a prototype and involves the use of a PIC microcontroller to generate the pulses for driving the switch of the SEPIC converter. The results have been presented to establish the viability of the scheme and portray a scope for its use in practice [14].

A novel half load-cycle worked dual SEPIC single-stage inverter has been developed based on the analysis of the relationship between input and output voltages of SEPIC converters operating in the discontinuous conduction mode. The output of the dual SEPIC converter has been connected in anti-parallel and half load-cycle control used to realize the boost and buck output directly The working principle, parameter selection and the control strategy of the inverters have been analyzed through simulation and experiment results [15].

II. PROBLEM FORMULATION

The objective of this paper owes to develop a VSC for a single phase SEPIC inverter suitable for use in the micro-grid with a view to reduce the Total Harmonic Distortion (THD) of the inverter output voltage, besides offering a regulated voltage over a range of operating loads. It becomes necessary on the theory of VSC to synthesize the output voltage owing to the attempt for allowing the inverter to receive power from the solar PV panel. The efforts require examining its performance from simulation and validating the results using an experimental prototype.

2.1 Power Circuit

An active switch (Q), two inductors (L_1 & L_2), two capacitors (C_1 & C_2) and two reverse connected transistors (T_1 & T_2) form the power module of the inverter seen in Fig-1 with a primary purpose of producing a sinusoidal output voltage. The turning on of the switch Q causes the input voltage to appear across L_1 and enables a linear increase of the current to charge the inductor. It simultaneously allows the initially charged capacitor C_2 to discharge through the inductor L_2 and the transistor T_1 does not conduct in this mode. However when the switch Q in the off state, the input voltage charges the capacitor C_1 in addition to maintaining the current through the inductor L_1 . The algebraic sum of currents through the inductors L_1 and L_2 constitute the output current to flow through the load and produce the positive voltage at the output.

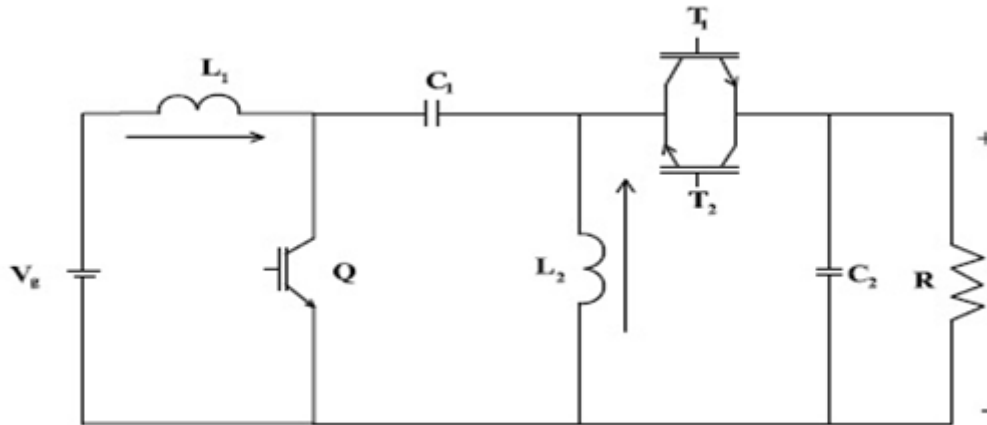


Fig 1. Power circuit of Micro grid inverter

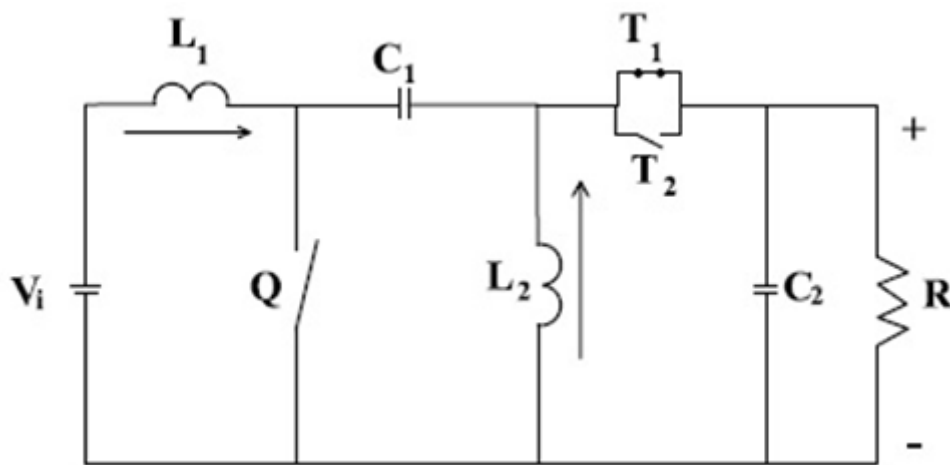


Fig 2. Mode I : positive peak Q and T1 are synchronized Q :off T1: on

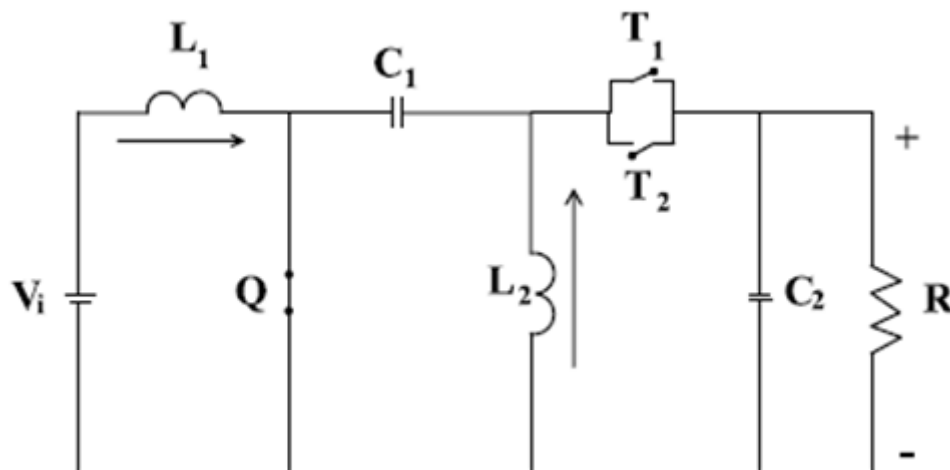


Fig 3. Mode II : positive peak Q and T1 are synchronized Q :on T1: off

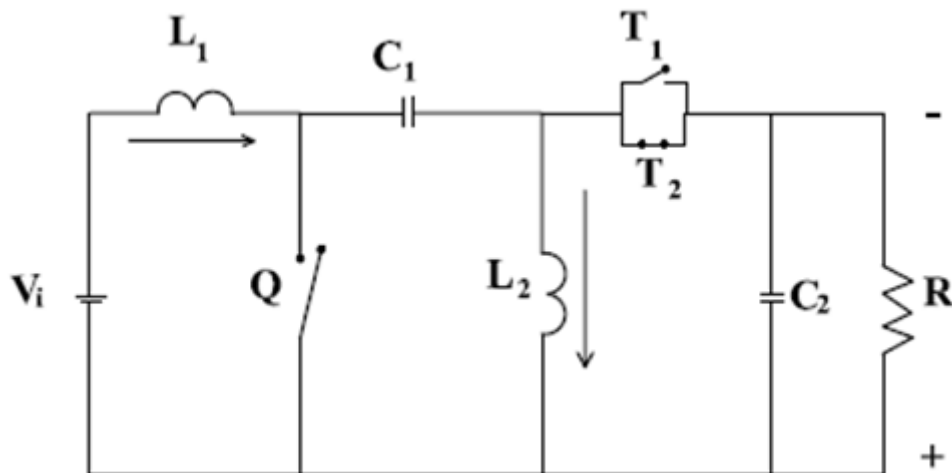


Fig 4. Mode III: Negative peak Q and T2 are synchronized Q :off T2: on

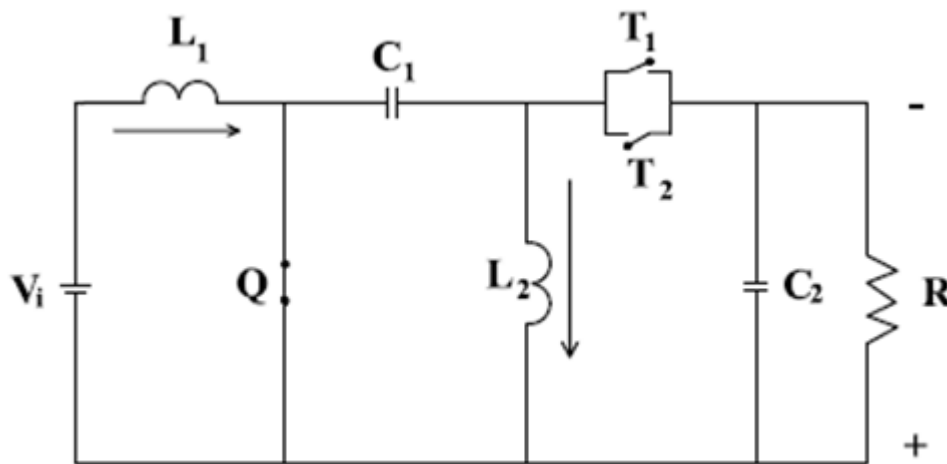


Fig 5. Mode IV: Negative peak Q and T2 are synchronized Q: on T2: off

Fig 2. through **Fig 5.** shows the different modes of operation and transition from positive to negative peak voltage

The turning on of the synchronizing switch T_2 assuages to reverse the direction of the load current and engage a transition mode to the operation of the system. With the switch Q turned on, the input voltage reappears across L_1 with the opposite polarity and allows a linear increase of current to charge the inductor in the reverse direction. It accompanies a discharge from the capacitor C_2 through L_2 and the transistor T_2 does not conduct in this mode.

When the switch Q turns off, the input voltage charges the capacitor C_1 besides maintaining the current through the inductor L_1 . The algebraic difference of the currents through the inductors L_1 and L_2 contribute to the output current and produce the negative load voltage.

III. MODELLING

The philosophy relies on the state space averaging to arrive at a dynamic modeling technique that allows mathematically representing the operation of the converters. It gives the state space representation of each mode of operation and requires taking the average over a cycle for elucidating the complete system. The first two modes give rise to the positive half cycle of output voltage and the remaining two modes to the negative half cycle of output voltage.

It necessitates four equations involving the state variables i_{L1} , i_{L2} , v_{C1} , v_{C2} to express the operation of the system. The switch Q remains off and T_1 on over the period $1-d$ where d represents the duty cycle of operation in the first mode.

The Eqns . (1) to (4) describe the mode I operation

$$\frac{di_{L1}}{dt} = -\frac{1}{L_1} v_{C1} + \frac{1}{L_1} v_{C2} + \frac{V_i}{L_1} \quad - \quad (1)$$

$$\frac{di_{L2}}{dt} = -\frac{1}{L_2} v_{C2} \quad - \quad (2)$$

$$\frac{dv_{C1}}{dt} = \frac{1}{C_1} i_{L1} \quad - \quad (3)$$

$$\frac{dv_{C2}}{dt} = \frac{1}{C_2} i_{L1} + \frac{1}{C_2} i_{L2} + \frac{1}{RC_2} v_{C2} \quad - \quad (4)$$

The switch Q turns ON and T1 remains on for the period of the chosen duty cycle d in the second mode.

The Eqns. 5 to 8 relate to the operation in the mode II

$$\frac{di_{L1}}{dt} = \frac{V_i}{L_1} \quad - \quad (5)$$

$$\frac{di_{L2}}{dt} = \frac{1}{L_2} v_{C1} \quad - \quad (6)$$

$$\frac{dv_{C1}}{dt} = -\frac{1}{C_1} i_{L2} \quad - \quad (7)$$

$$\frac{dv_{C2}}{dt} = -\frac{1}{RC_2} v_{C2} \quad - \quad (8)$$

The switch Q off and T2 on for the period of 1-d in the third mode of operation. The Eqns. (9) to (12) represent the behavior in the mode III

$$\frac{di_{L1}}{dt} = -\frac{1}{L_1} v_{C1} + \frac{1}{L_1} v_{C2} + \frac{V_i}{L_1} \quad - \quad (9)$$

$$\frac{di_{L2}}{dt} = -\frac{1}{L_2} v_{C2} \quad - \quad (10)$$

$$\frac{dv_{C1}}{dt} = \frac{1}{C_1} i_{L1} \quad - \quad (11)$$

$$\frac{dv_{C2}}{dt} = \frac{1}{C_2} i_{L1} + \frac{1}{C_2} i_{L2} - \frac{1}{RC_2} v_{C2} \quad - \quad (12)$$

The switch Q comes back into on state with T2 still on over the period of the duty cycle d to constitute the fourth mode of operation.

The Eqns. (13) to (16) explain the operation in the mode IV

$$\frac{di_{L1}}{dt} = \frac{V_i}{L_1} \quad - \quad (13)$$

$$\frac{di_{L2}}{dt} = -\frac{1}{L_2} v_{C1} \quad - \quad (14)$$

$$\frac{dv_{C1}}{dt} = \frac{1}{C_1} i_{L2} \quad - \quad (15)$$

$$\frac{dv_{C2}}{dt} = -\frac{1}{RC_2} v_{C2} \quad - \quad (16)$$

The averaged state space model of the inverter over a cycle can be obtained using Eqns. 17 and 18 and the corresponding state space matrices from Eqns. (19) to (22)

$$\dot{x} = A_{avg}x + B_{avg}u \quad - \quad (17)$$

$$V_O = C_{avg}x + C_{avg}u \quad - \quad (18)$$

$$A_{avg} = d_{positive}A_1 + (1-d_{positive})A_2 + d_{negative}A_3 + (1-d_{negative})A_4 \quad - \quad (19)$$

$$B_{avg} = d_{positive}B_1 + (1-d_{positive})B_2 + d_{negative}B_3 + (1-d_{negative})B_4 \quad - \quad (20)$$

$$C_{avg} = d_{positive}C_1 + (1-d_{positive})C_2 + d_{negative}C_3 + (1-d_{negative})C_4 \quad - \quad (21)$$

$$E_{avg} = d_{positive}E_1 + (1-d_{positive})E_2 + d_{negative}E_3 + (1-d_{negative})E_4 \quad - \quad (22)$$

The averaged state space matrices relate as:

$$A_{avg} = \begin{bmatrix} 0 & 0 & \frac{-(K_p(1-d_p)+K_n(1-d_n))}{L_1} & \frac{K_n(1-d_n)-K_p(1-d_p)}{L_1} \\ 0 & 0 & \frac{K_p d_p - K_n d_n}{L_2} & \frac{K_p(1-d_p)+K_n(1-d_n)}{L_2} \\ \frac{K_p(1-d_p)-K_n(1-d_n)}{C_1} & \frac{K_n d_n - K_p d_p}{C_1} & 0 & 0 \\ \frac{K_p(1-d_p)-K_n(1-d_n)}{C_2} & \frac{K_p(1-d_p)-K_n(1-d_n)}{C_2} & 0 & \frac{-(K_p+K_n)}{C_{2R}} \end{bmatrix}$$

$$B_{avg} = \begin{bmatrix} \frac{K_p+K_n}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$C_{avg} = [0 \quad 0 \quad 0 \quad K_p + K_n]$$

IV. CONTROL STRATEGY

The VSC alters the dynamics of a system by the application of a discontinuous control signal in the sense the state feedback control law appears to be a discontinuous function of time and thus allows the system to switch from one continuous structure to another. The discontinuous signal augurs the system to slide along cross section of the system's normal behavior.

The procedure evolves the design of multiple control structures so that the trajectories travel toward adjacent region with a different control structure in order that the ultimate trajectory does not exist entirely within one control structure and slides along the boundaries of the control structures. The motion of the system that slides along the boundaries forms the locus consisting of the boundaries termed as the switching surface [10].

The function of switching control law allows driving the state trajectory onto a pre-specified surface and maintains it for the subsequent time. It becomes appropriate to formulate a control law that adopts a switching function such as

$$U = 1 \text{ When } S > 0$$

$$U = 0 \text{ When } S < 0$$

Where S is the instantaneous state variable's trajectory and can be described as

$$S = \alpha_1 X_1 + \alpha_2 X_2 + \alpha_3 X_3$$

Where α_1 , α_2 and α_3 represent the control parameters usually referred to as the coefficients and X_1 , X_2 and X_3 denote the desired state feedback variables that require to be controlled.

The switching surface may be obtained by enforcing $S=0$.

The mapping for the equivalent control function in terms of the duty ratio control d is given in

$$0 < d = \frac{V_c}{V_{ramp}} < 1 \quad - \quad (23)$$

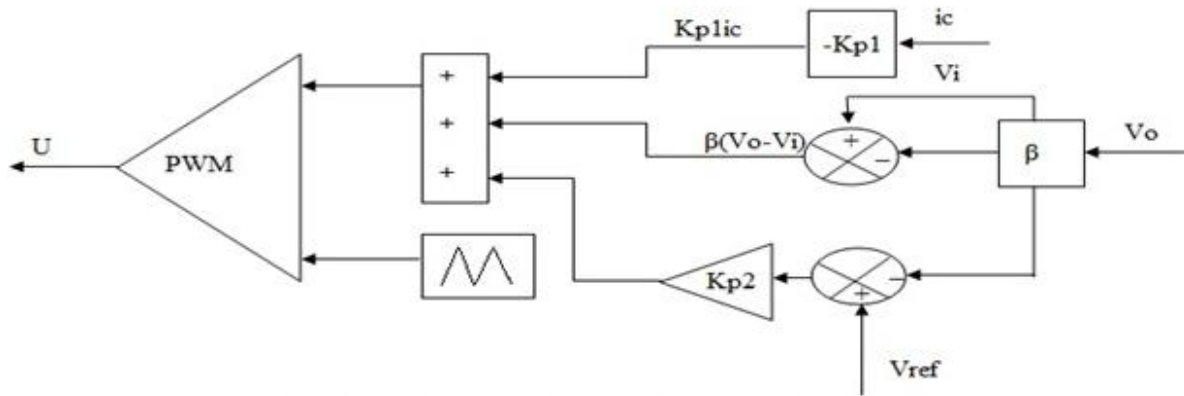


Fig 6. Sliding mode controller for Micro grid Inverter

$$U_{sequ} = d \quad d = \frac{V_C}{V_{ramp}} \quad V_C = d * V_{ramp} \quad V_{ramp} = \beta V_{in} \quad - \quad (24)$$

$$V_C = U_{sequ} = -\beta L \left[\left(\frac{\alpha_1}{\alpha_2} \right) - \left(\frac{1}{RC} \right) \right] i_C + LC \left(\frac{\alpha_3}{\alpha_2} \right) (V_{ref} - \beta V_o) + \beta (V_o - V_i) \quad - \quad (25)$$

$$V_C = -K_{p1} i_C + K_{p2} (V_{ref} - \beta V_o) + \beta (V_o - V_i) \quad - \quad (26)$$

$$K_{p1} = \beta L \left(\frac{\alpha_1}{\alpha_2} \right) - \left(\frac{1}{RC} \right) \quad \& \quad K_{p2} = LC \left(\frac{\alpha_3}{\alpha_2} \right) \quad - \quad (27)$$

V. SIMULATION RESULTS

The exercise endeavors to examine the performance of the inverter through simulation on a MATLAB – SIMULINK platform. The Tables 1 and 2 include the specifications of the PV panel and the parametric values of the elements in the inverter.

The study envisages arriving at a steady state sinusoidal output of 230V from a dc input supply of 140V acquired from the solar panel to support a resistive load of 2.5 kW, when the power switches operate at a switching frequency of 10 KHz.

Table 1. Specification for the PV Panel

PV Module	
Number of cells in a modules	36
Open circuits voltage	21 V
Short circuit current	6.4 A
Voltage at MPP, V_m	17 V
Current at MPP, I_m	5.4 A
PV Array	
Voltage at MPP, $V_{mpp} = V_{pv}$	140
Power at MPP, $P_{mpp} = P_{pv}$	2000W
Current at MPP, $I_{mpp} = I_{pv}$	13.3 A
No. of Series Modules N_s	$V_{amp}/V_{im}=9$
No. of Parallel Modules N_p	$I_{mp}/I_m=2$

Table 2. List of Parameters

Description	Parameter	Nominal Value
Input Voltage	V_{in}	140 V
Inductance	L_1 & L_2	165 μ H
Capacitance	C_1 & C_2	30 μ F
Switching Frequency	F	10KHz
Load Resistance	R	2.5KW
Output Voltage	V_o	230 V

The efforts relate to simulating the performance in an attempt to obtain 230 volts ac from a solar input of 140 volts. The graphs in Fig 7 and Fig 8 correspond to the input voltage, the output voltage and current corresponding to a load of 2.5 kW. It engages to introduce sudden changes in the load and supply at $t = 0.05$ s and $t = 1$ s respectively in order to evaluate the robustness of the controllers. Though the load current increases, still it retains the desired output voltage on account of the modification in the duty cycle. Similarly the VSC ensures to maintain the output voltage even in the case offset point changes as seen from the same figure.

The THD spectrum drawn in Fig 9 and Fig 10 for the same operating point and the bar diagram in Fig 11 elicits the merits of the VSC over the PI controller in terms of a much lower THD for the entire operating range.

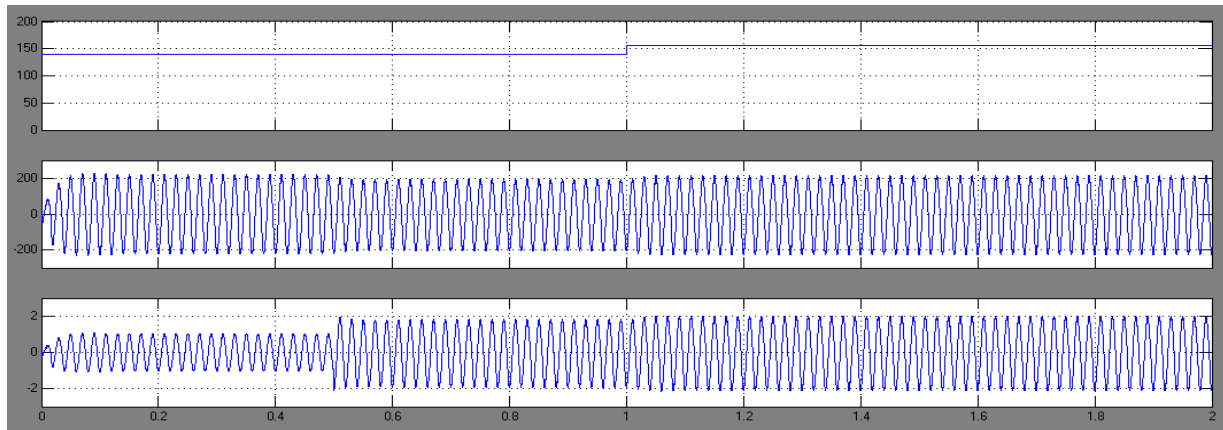


Fig 7. Output voltage and current from PI in Boost Mode

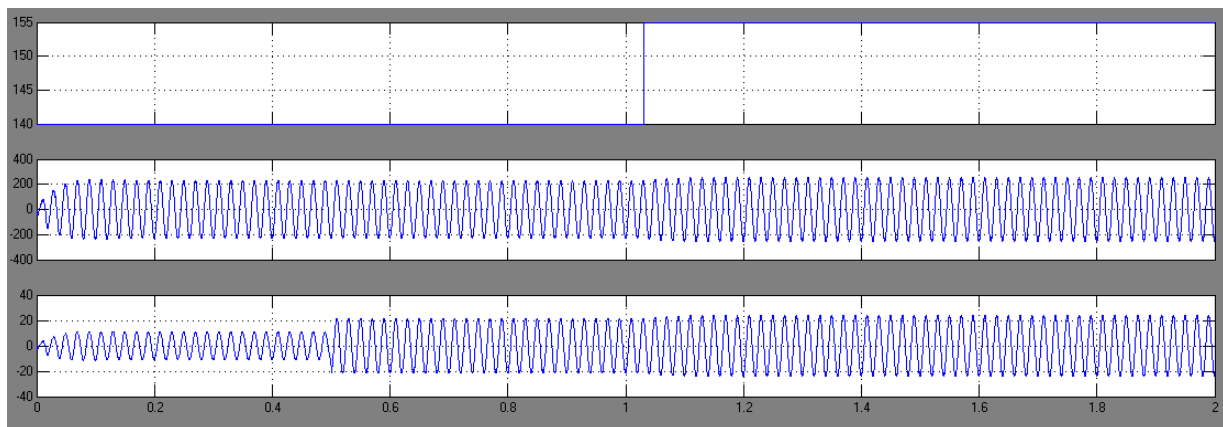


Fig 8. Output voltage and current from SMC in Boost Mode

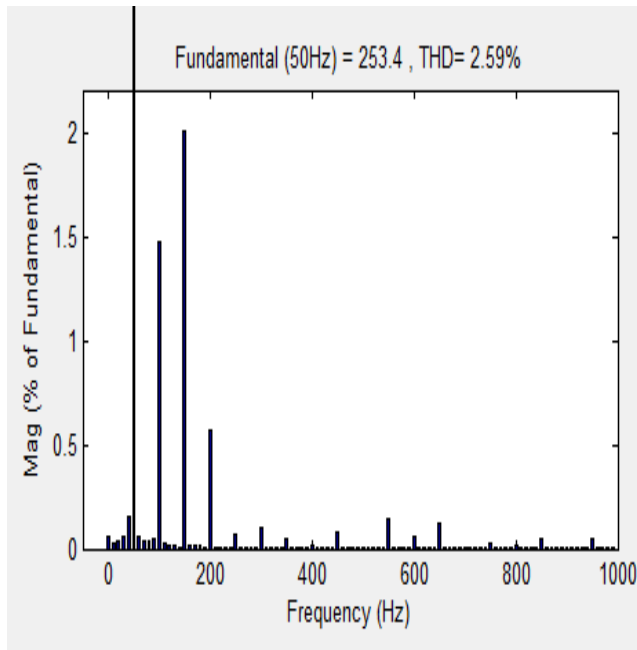


Fig 9. FET for PI in Boost Mode

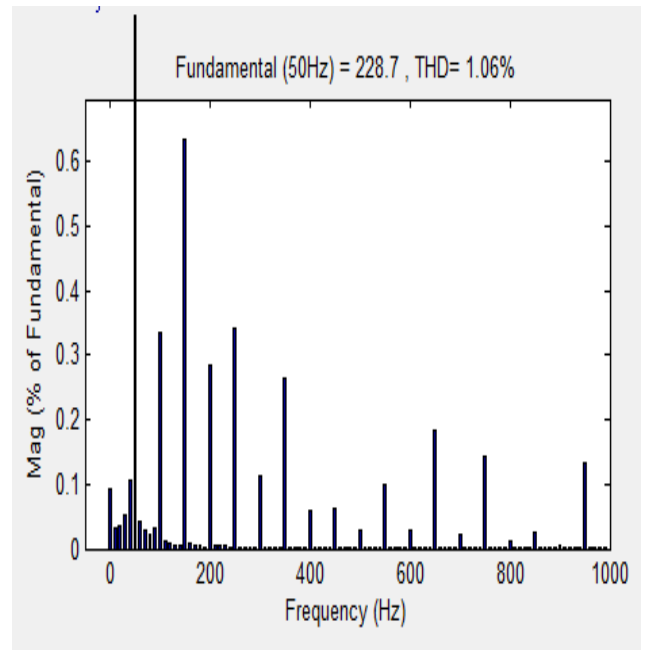


Fig 10. FET for SMC in Boost Mode

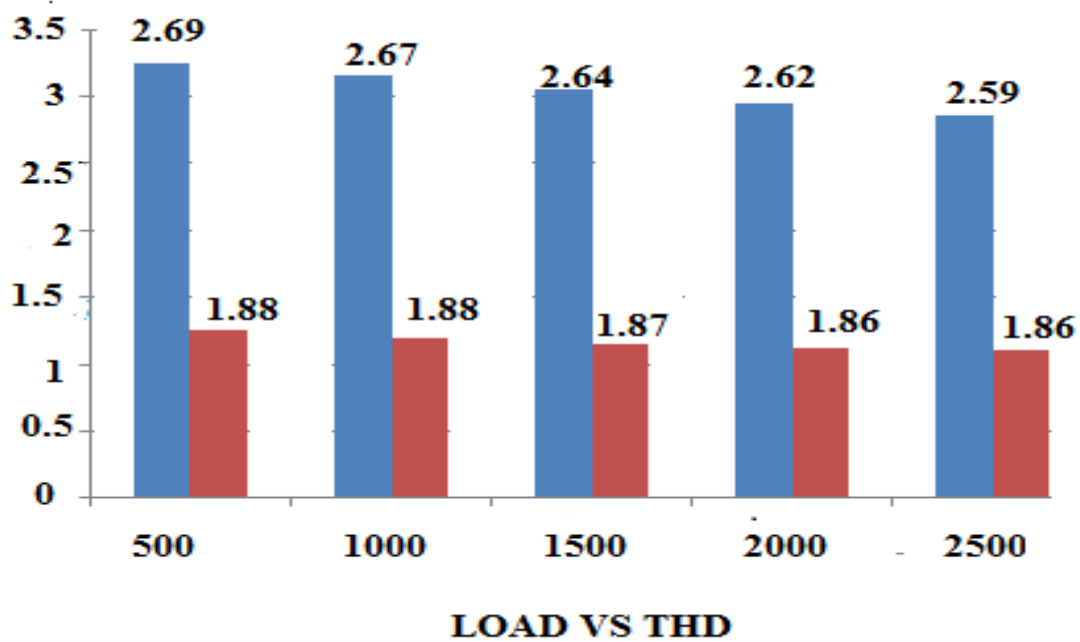


Fig 11. Bar Chart

VI. HARDWARE IMPLEMENTATION

The methodology involves constructing a hardware prototype with similar ratings as that used in simulation and investigating the performance through the same operating range. It features using a ATmega 8 processor to generate the PWM pulses for the MOSFET switches in accordance with the design of the control strategy.

The ATmega 8 belongs to a class of a low-power CMOS 8-bit microcontroller following the generics of the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega 8 achieves throughputs approaching 1 MIPS per MHz allowing the system design to optimize power consumption against the processing speed. The AVR core combines a rich instruction set with 32 general

purpose working registers. The registers remain directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle.



Fig 12. Solar Panel



Fig 13. Control section

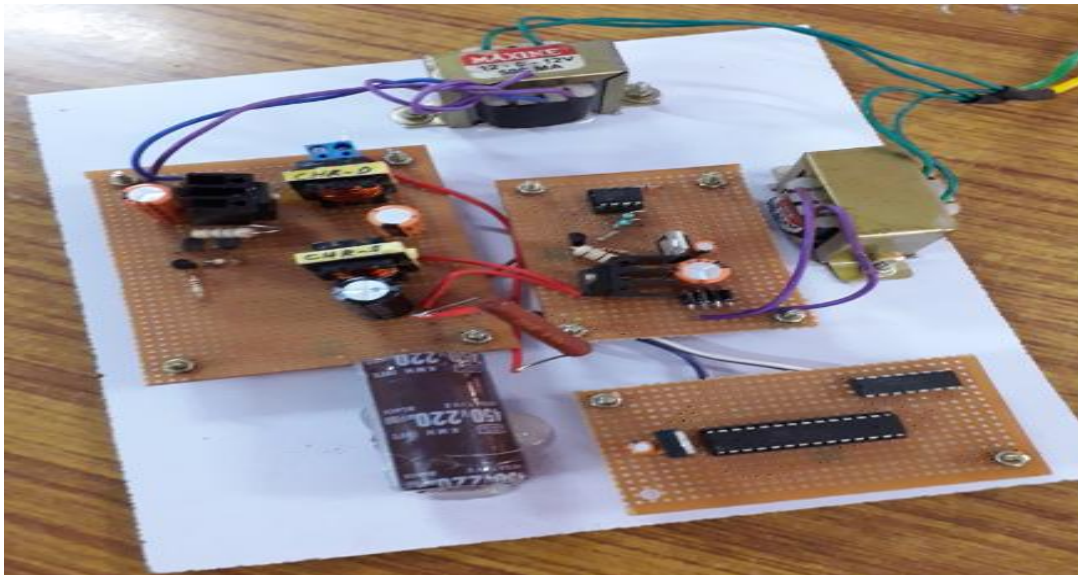


Fig 14. Experimental prototype

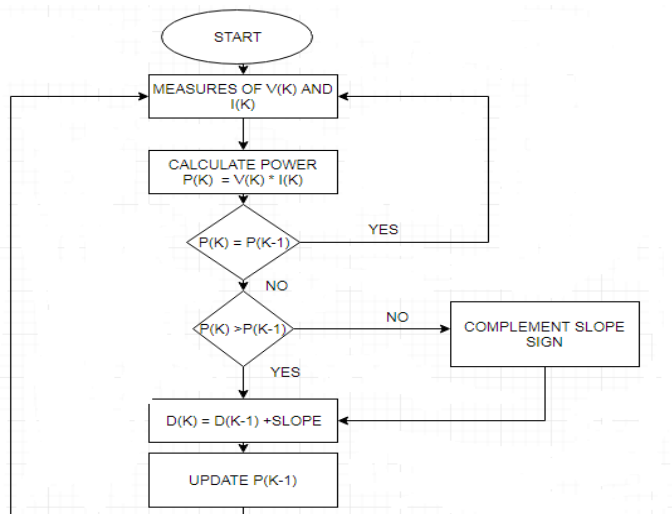


Fig 15. Flow chart of voltage algorithm

The photographs displayed in Fig 12 through Fig 14 shows the solar PV panel, control section from where the dc output enters the prototype and the hardware set up formed for testing the applicability of the scheme. The flow schematic in Fig 15 explains the process of generation of appropriate firing pulses for the MOSFET switches. The sinusoidal nature of the output voltage in Fig 16 captured using an attenuator probe of 1:10 at the operating point of 2.5kW along with its corresponding THD spectrum in Fig 17 orchestrate the benefits of the chosen inverter in terms of its suitability for being connected to the grid.

Besides the shape of the input current waveform and its THD spectrum in Fig 18 and 19 respectively, obtained at the same operating point bring out the merits of the control scheme in being able to contribute to the improvement in power quality. The close comparison of the readings in the Table 3 allows validating the simulated performance across the operating range.

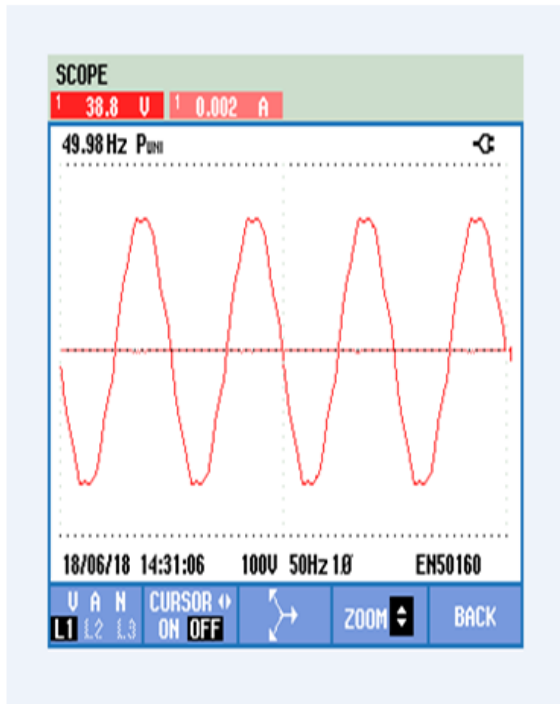


Fig 16. Output Voltage

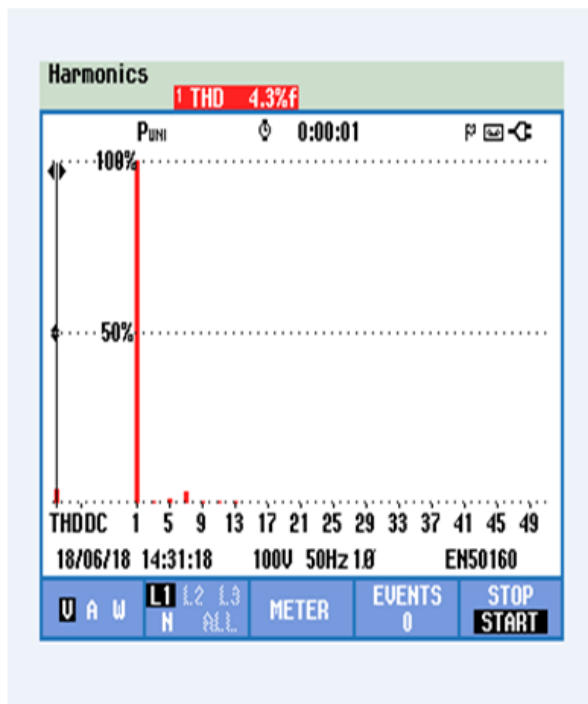


Fig 17. Output Voltage THD

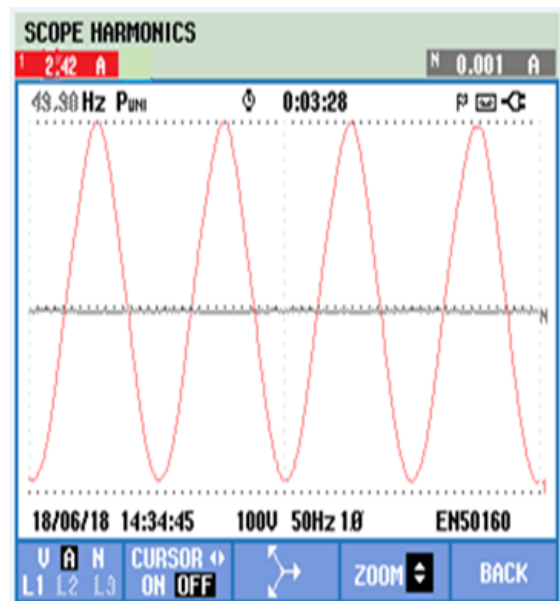


Fig 18. Input Current

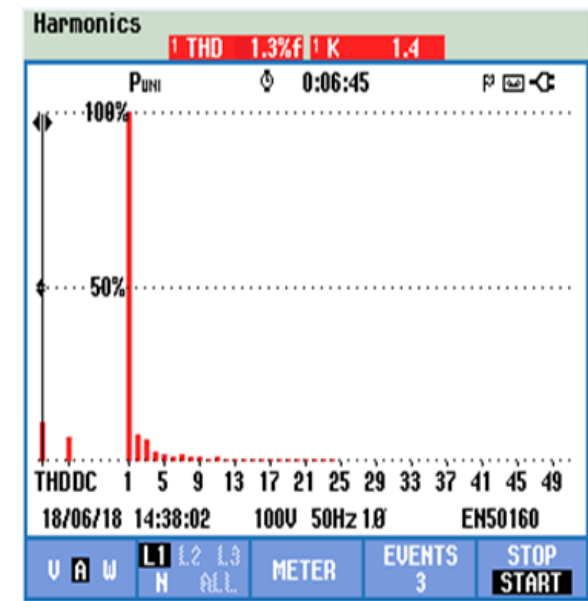


Fig 19. Output Current

Table 3. Comparison of Simulation and Hardware Results

LOAD (KW)	LOAD VOLTAGE (Volts)			LOAD CURRENT (Amps)			TOTAL HARMONIC DISTORTION(THD) %		
	SIMULATION		HARD WARE	SIMULATION		HARD WARE	SIMULATION		HARD WARE
	PI	SMC		PI	SMC		PI	SMC	
500	230.0	230.0	228	2.17	2.17	2.19	2.69	1.88	4.3
1000	229.5	229.9	228	4.35	4.35	4.38	2.67	1.88	4.1
1500	229.2	229.5	228.5	6.54	6.53	6.56	2.64	1.87	4.0
2000	229.1	229.2	230	8.72	8.71	8.69	2.62	1.86	3.8
2500	229.0	229.1	230	10.91	10.90	10.86	2.59	1.86	3.1

VII. CONCLUSION

A VSC based control strategy has been formulated for operating the micro-grid inverter from a solar source. The inverter has been modeled in the state space framework and the control theory incorporated to develop the methodology for generating the PWM pulses. The performance has been evaluated to regulate a regulated output voltage over a range of operating loads. The ability of the control scheme has been projected to reject both servo and regulatory disturbances and maintain the desired output voltage at the new operating point. The methodology has been tailored to lower the output voltage and the input current. The consequent increase in the fundamental component has been projected to facilitate the sinusoidal shape of the output voltage. The results have been obtained to enable the inverter claim an integral part of a renewable energy supported micro-grid.

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